Designing dependable systems through a test-in-the-loop method

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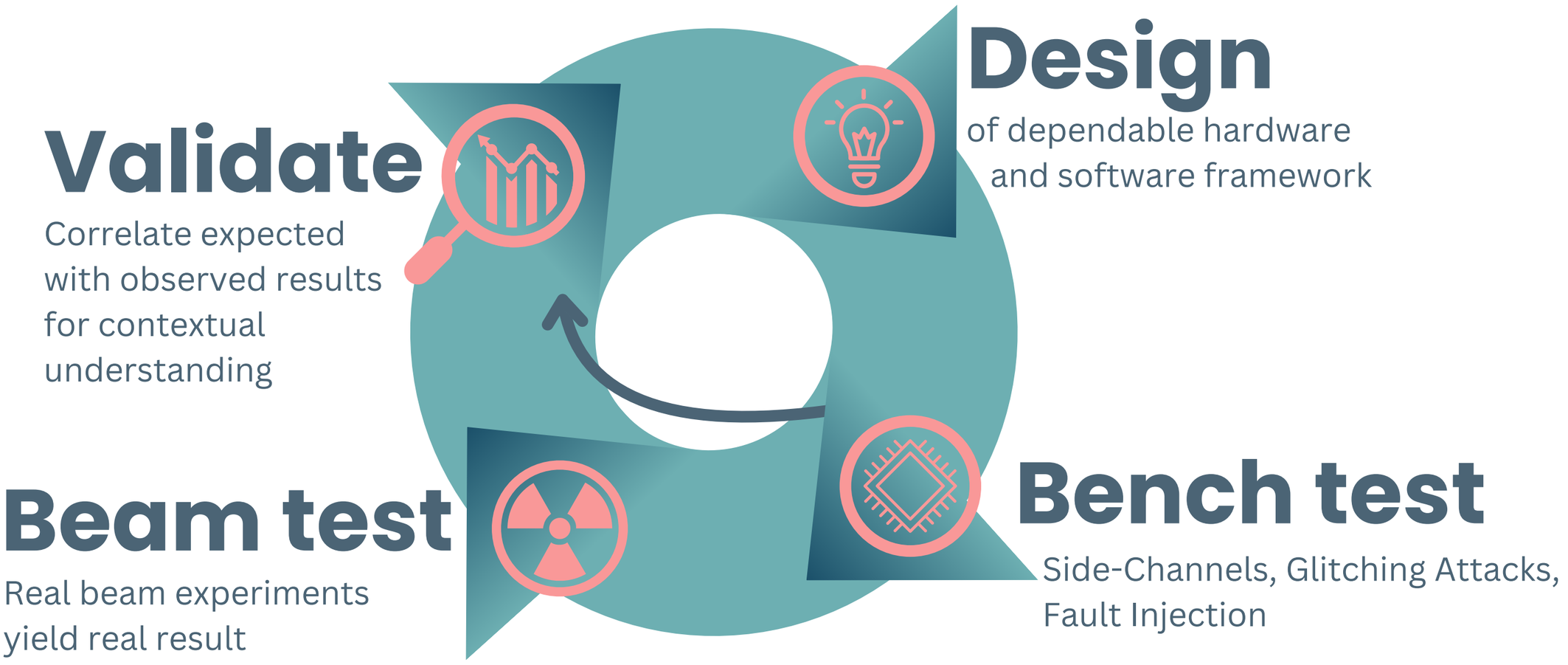


Introduction
As intelligent systems increasingly permeate various industries, the challenge of reducing implementation costs while ensuring high reliability and security becomes paramount, especially in critical domains like space applications. RISC-V has emerged as a flexible and cost-effective solution, promoting innovation through its open-source nature. However, the complexity introduced by its adaptability poses challenges for industries with stringent certification requirements. Traditional validation processes are often time-consuming and expensive, necessitating a more efficient approach to certification. This research presents a novel methodology for accelerated validation of RISC-V intellectual property (IP), utilizing rapid bench and beam testing to assess hardware reliability and security against radiation-induced errors and security threats. By integrating standard hardware components and automation, our approach aims to streamline certification efforts, making RISC-V a competitive architecture for high-reliability applications while minimizing engineering costs and complexity.

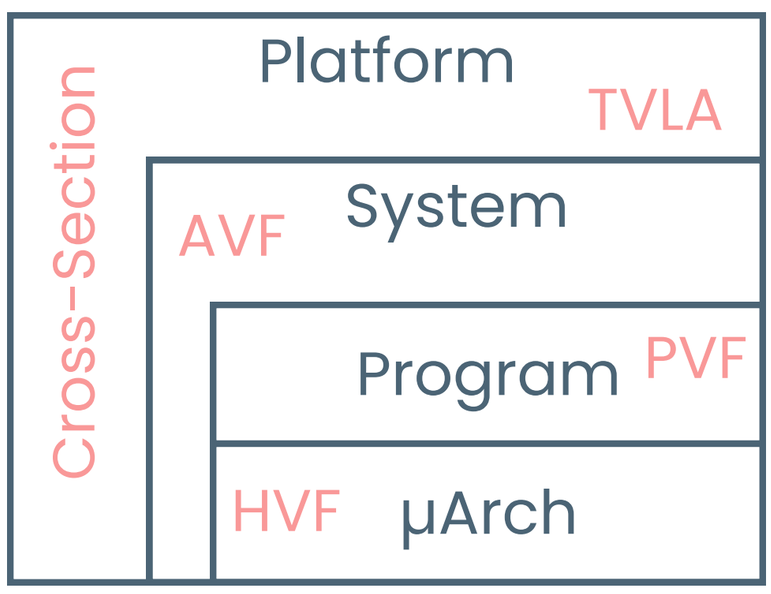
Design Phase
- Emphasis on co-design of dependable hardware and software frameworks. E.g. probabilistic instruction validators, resilient execution environments.
- Development of a hardware shell for streamlined I/O interfacing and adaptability across multiple devices.

Bench Testing Phase
- Serves as holistic validation of Software Under Test (SUT) and Hardware Under Test (DUT)
- Involves post-simulation work on the final implemented platform.
- Provides preliminary reliability estimations.
- Crucial for security evaluations; results are considered final.
- Assessment of vulnerabilities through: Side-channel analysis, Glitch attack methodologies, TVLA for detecting information leakage.
- Fault injection to quantify system resilience.

Beam Testing Phase
- Real beam experiments yield real results.
- Strong correlation with fault emulation techniques.
- Beam experiments explicitly included in the methodology.
- Ensure that the software as part of the fixture is protected to exclusively target the SUT.

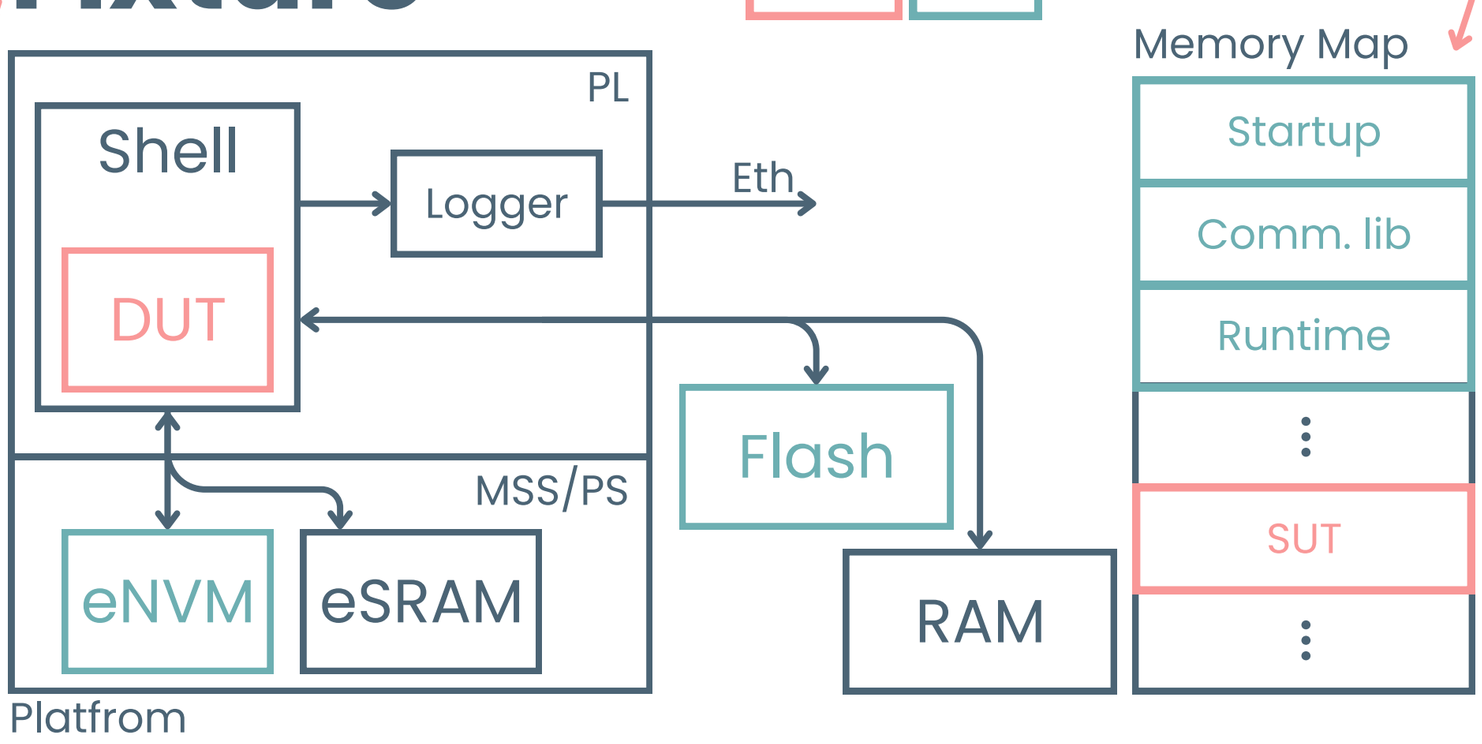
Validation Phase
- Validation of designs using results from bench and beam experiments.
- Create a contextual understanding of results.
- Side-channel analysis results correlated with specific instructions for targeted countermeasures.
- Vulnerabilities from glitching attacks addressed through enhanced countermeasures.
- Combining results from both testing stages deepens understanding of system behavior.

Metrics



Key Dependability Metrics: Cross-Section, Test Vector Leakage Assessment (TVLA), Signal-to-Noise Ratio (SNR), System Vulnerability Factor (AVF), Microarchitectural Vulnerability Factor (HVF), Program Vulnerability Factor (PVF).

Fixture



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