SEFUW 2025

A Roadmap for NanoXplore Platforms

LGM GROUP INTRODUCTION

MANAGEMENT AND ENGINEERING OF COMPLEX PROJECTS AND SUPPORT

- MAINTENANCE AND SUPPORT ENGINEERING
- SYSTEMS ENGINEERING & RAMST
- ORGANISATIONS AND PROGRAM PERFORMANCE
- DIGITALISATION, DATA & INFORMATION TECHNOLOGY

ELECTRONIC ENGINEERING AND PRODUCTION

- **CRITICAL ELECTRONICS** EQUIPMENT
- **RADIOFREQUENCY** AND **MICROWAVES**
- **FPGA** AND **SOFTWARE** SOLUTIONS
- MICROELECTRONICS
- EMBEDDED NETWORKS
- TEST BENCHES

LGM : A GROWING PLAYER IN THE SPACE INDUSTRY

2000
ILS studies for ground station

2003
ILS Studies for M51

2008
1st ESA contract

2009
LGM ISS ground segment A5

2016
EGSE :for SODERN IVV for TAS Belgium

2017
Opening for LGM In Guyana
Start R&T in electronics

2018
LGM is collaborating with AIRBUS and THALES to develop the system support for SYRACUSE 4 (S3000L / S1000D)

2019
International referencing for ILS and RAMS

2020
Start R&T for NX FPGA

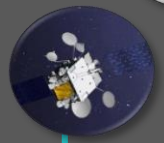
2021
RF test benches for THALES and AD&S

2022
Digitalisation of CSG







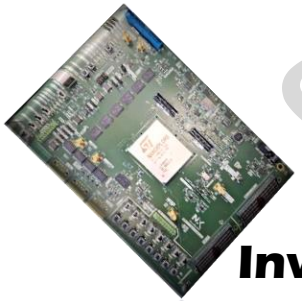




R&T STRATEGY ON NANOXPLORE SOLUTIONS

R&T roadmap

State of the art



Invest on HW platforms

ECOSYSTEM

of

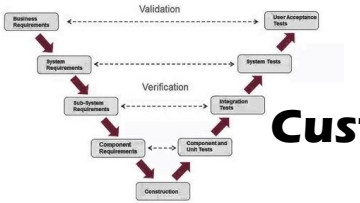
EXPERTISES & BUILDING BLOCKS to

HELP YOU

to **adopt NanoXplore**

solutions and **facilitate** their use

Train more FPGA/SoC specialists to NX

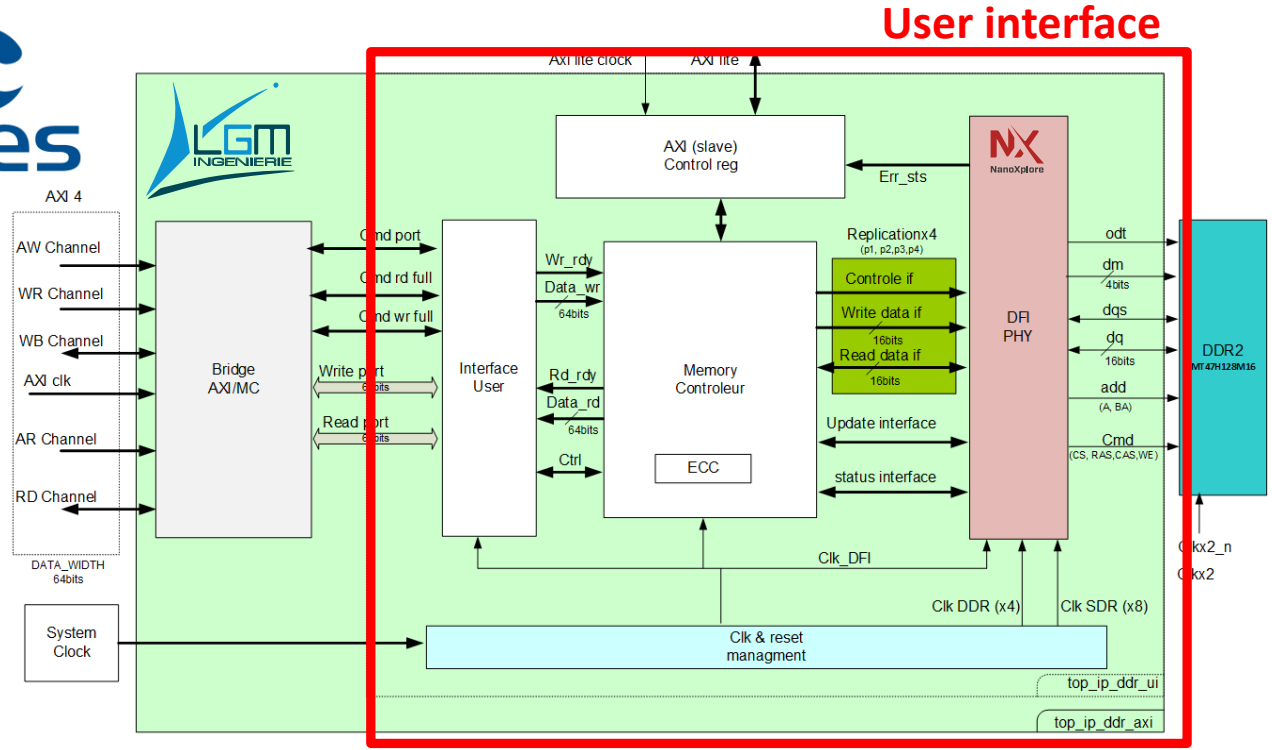


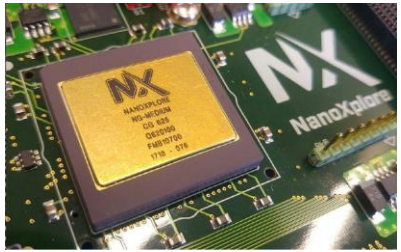
Custom solutions

Reinforce partnerships

DDR2 controller IP core

DDR2 IP CORE ALREADY AVAILABLE





- **Available for free** on NanoXplore Design Suite for **NG-MEDIUM**
- Stand alone "**User interface**" for light implementation => **available on request**

DDR2 IP CORE MAIN CHARACTERISTICS

- **AXI-4** interface for data path
- **AXI-Lite** interface for command and control
- **SECDED** with a 32/39 ECC implementation
- Generate **Error Correction statistics**
- Implements **JEDEC** parameters to support all standard memory chips
- **MR and EMR auto refresh** capabilities
- **Up to 64 bits** configuration
- **4 rank** support, **8 bank** support
- Supports **CAS** Latency between **2 and 6**
- Supports **Additive Latency** between **0 and 4**
- Total Write latency up to 8 (CAL+AL)

GENERIC & ADAPTATIVE

- **Compliant to** ECSS-Q-ST-60-02C adapted by CNES
- Fully tested on **Micron DDR2** **MT47H128M16RT**
- Fully simulated on **ISSI DDR2** **IS46DR16128C**
- Fully **automatized tests** (physical and simulation)
- **More than 50 tests scenarios**
- **UVVM methodology including OSVVM** library for **random** generation
- **100% code coverage** on branches and statements
- Tested at **250 MT/s**

DDR2 controller IP core

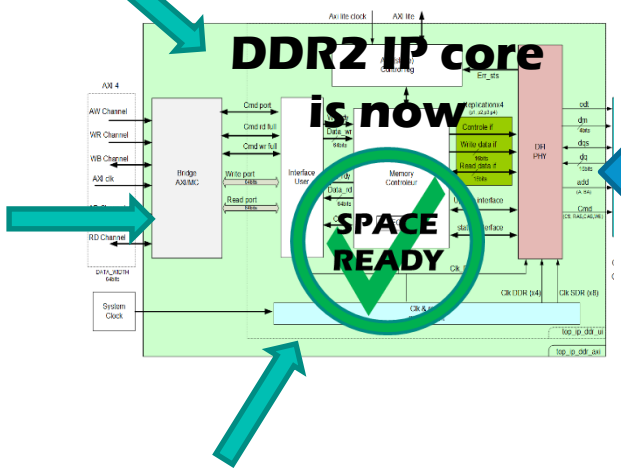
«SPACE READY»VERSION NOW AVAILABLE

Write back

Performs an automatic write command when a read error is detected

Scrubbing

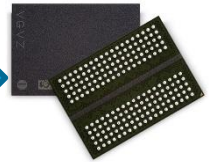
Performs automatic read and integrity checks at programmable intervals

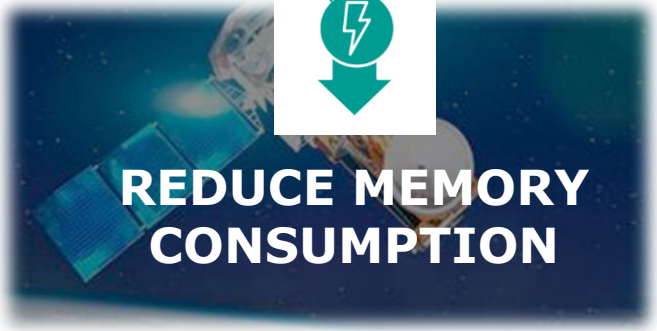


Power-down

Reduce the static power **from 30%** compare to standby mode

Contact us !

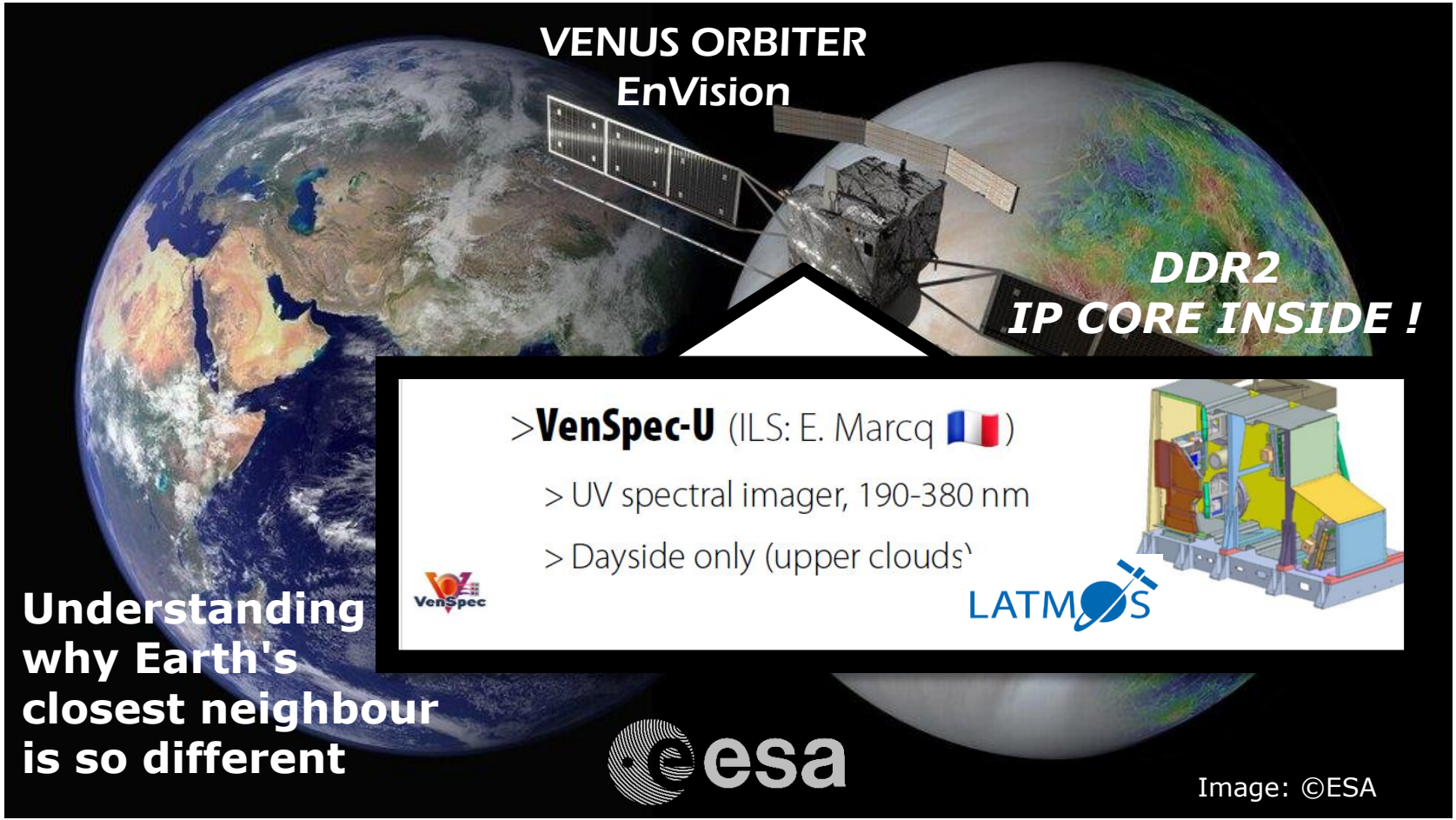




« *Use case* »

DDR2 controller IP core
on VENUS EnVision Orbiter

DDR2 CONTROLLER IP CORE : FLYING TO VENUS !



LGMI Roadmap to NanoXplore solutions

ROADMAP : IP & CUSTOM DESIGN

DDR2 Controller IP
Space-ready version
(NG-MEDIUM)

DDR2 Controller IP
(NG-MEDIUM)

DDR3 Controller IP
(ULTRA 300)

JESD204B & ESISTREAM
implementation
(NG-ULTRA/300)

2024 | 2025 | 2026 | 2027

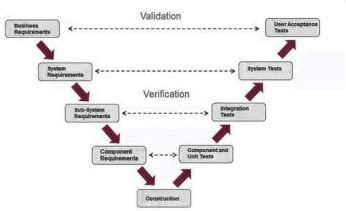
AXI interfaces IPs

DDR3 Controller IP
(NG-ULTRA)

JESD204B &
ESISTREAM evaluation
(NG-ULTRA/300)

Very high speed NVM I/F
& RF algorithm IP

Custom design



THANK YOU !

Contact : **sebastien.ruffat@lgm.fr**