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Space Applications for Versal using Open Standards Based Modules

6th SEFUW (SpacE FPGA Users Workshop) March 2025

David Dolman MEng. MIET, XACE
Director of Systems Engineering
Alpha Data Parallel Systems Ltd.

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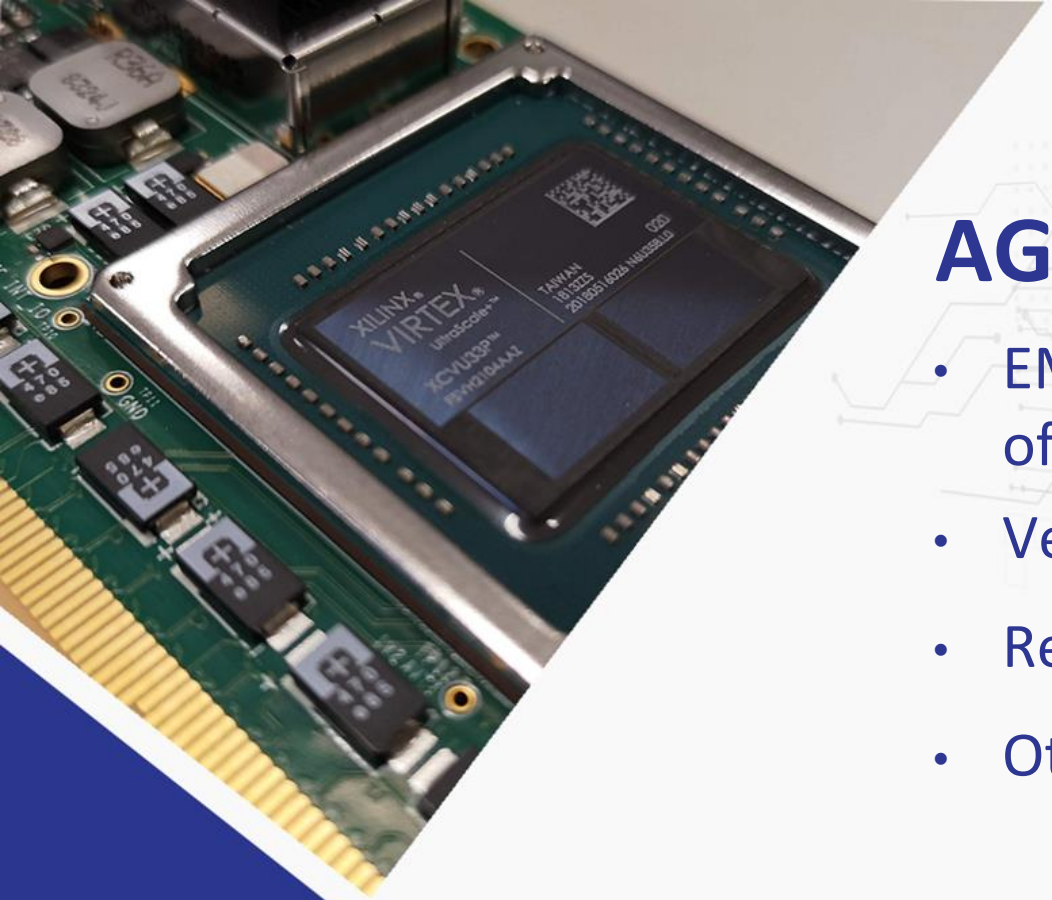

AGENDA

- EMIT – Zynq7000 SoC & Advantages of Open Module Standards
- Versal for Space
- Redesigned EMIT with Versal
- Other Example Application on Versal

  Laser Spectrometer, AI Fault detection, and 1M point FFT
- Deployment options from Alpha Data
- Q & A

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EMIT – Zynq7000 SoC & Advantages of Open Module Standards

Jet Propulsion Laboratory
California Institute of Technology

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CORRECT designs
Right the First Time

mercury systems

EMIT: Earth Surface Mineral Dust Source Investigation

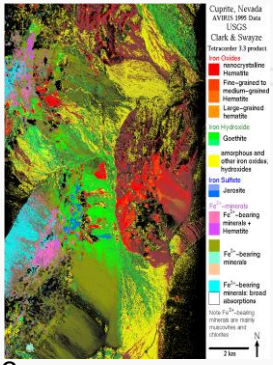
Hyperspecial Imaging System, operating on ISS (ELC-1) for 2 Years, 8 Months, and 12 days

Primary Objective (1 year mission)

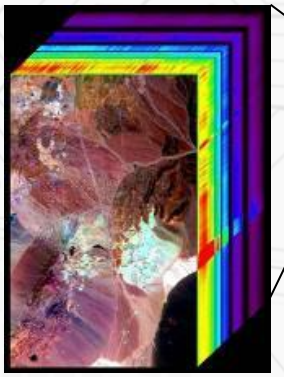
Close the gap in our understanding of mineral dust heating or cooling of the Earth by determining the mineralogy of soils in the arid dust source regions.

Secondary Objectives

- Methane and CO2
- Biodiversity and Ecosystems
- Fire fuels and burn severity
- Hazards
- Surface Plastic
- Algal blooms
- Agriculture
- Mid-Lat snow/ice
- Geology and Resources



10 Mb/s Downlink to Earth



1.6 Gb/s In

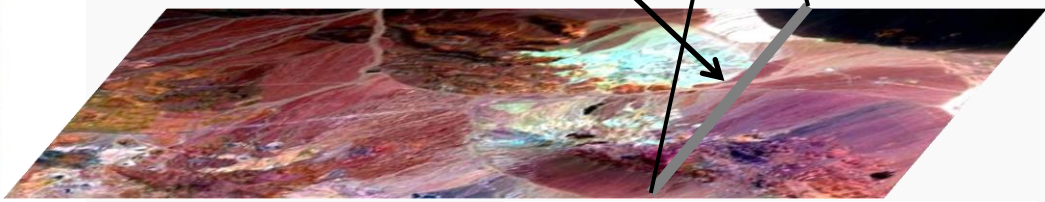
Detector Array

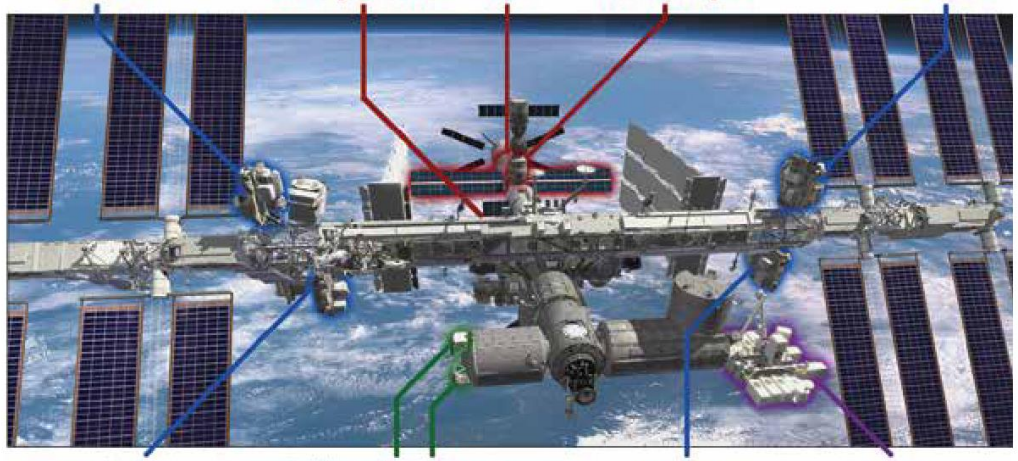
Spectrometer

Telescope

Reflected Sunlight

Direction of flight





Courtesy of Rob Green

Jet Propulsion Laboratory
California Institute of Technology

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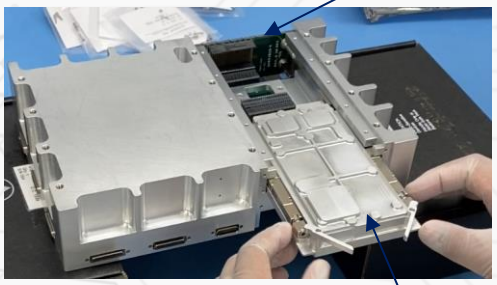
Heart of EMIT: The FPIE-D

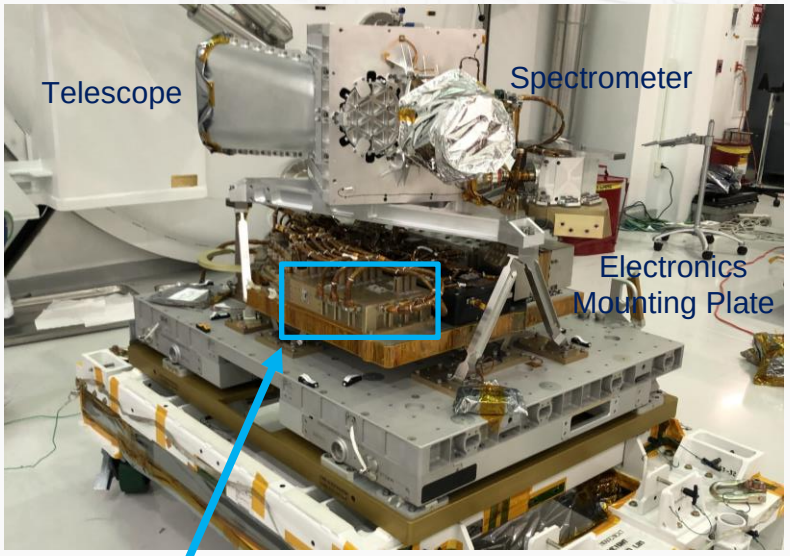
Focal Plane Interface Electronics (Digital)

- Provides Software based control of the instrument
- Collects detector data @1.6Gb/s from FPA (Focal Plane Array)
- Buffers collected data on non-volatile storage (held on a separate VPX module)
- Controls cryocooler, heater control, and FPA power
- Performs System monitoring (voltage, current, and temperate)
- Handles command and telemetry data from ISS via 1553 interface.
- Performs compression of Science Data
- and performs downlink of Science Data

Mission Stats:
- NASA Class C Mission
- Mass Instrument: 188 kg
- Operational Power Average: 140 W Peak: 179 W
- ISS Data average Rate: 3.2 Mbps (Peak 10Mbps)
- Sensor data rate 1.6Gb/s
- Lossless data capture

Focal Plane Interface Electronics Digital (FPIE-D)





Instrument mounted on Vibration Plate

Focal Plane Interface Electronics Digital (FPIE-D)

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Images curtesy of JPL

Open Standards Based Platforms

Key Features

- Many Open Standards out there for embedded electronics
- VITA (VMEbus Industry Trade Association) supports a significant number:

  VPX, XMC, FMC, VNX, **Space VPX** and many others
- Non-VITA Standards too

  CPCI, **AHDA**

All share many advantages:

- Standard units available off the shelf
- Rapid system building
- Module interoperability
- Even custom units can exploit the established connectivity and mechanical constraints to design to lower design risk.
- Savings come through design re-use and higher volume production
- **Reduces your Risk!**

How did this help EMIT?

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FPIE-D Hardware: COTS to Space

FPIE-D hardware/firmware/software development and implementation was only 1.5 years.

Fast time scale was achieved by taking a standard COTS board for initial development and re-spinning it into a full Space Grade design, replacing, where needed, components with their space grade equivalent, and extended the design to add features needed for the mission (e.g. 1553 interface to communicate with the ISS).

(In Defence and other Embedded Industries often termed COTS this refers to the module availability, not the component (individual chip) radiation classification)

The COTS board was a standard VITA XMC form factor board, commonly used in defence and aerospace applications. The Space board is a custom shape, however, acts as a 3U VPX chassis, allowing interfacing with standard 3U VPX module. This allowed the project to use a qualified and well tested SSDR to take care of bulk storage of data.

On 'Day One' of the project engineers could start using the COTs hardware, that looked from a FPGA and software point of view just like the final hardware.

COTS to Space

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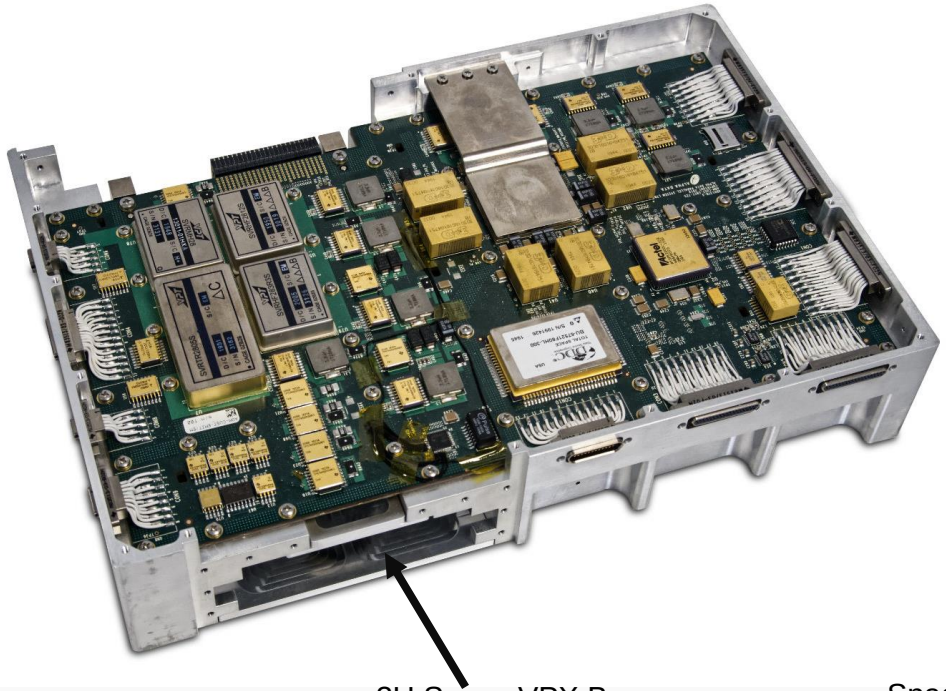
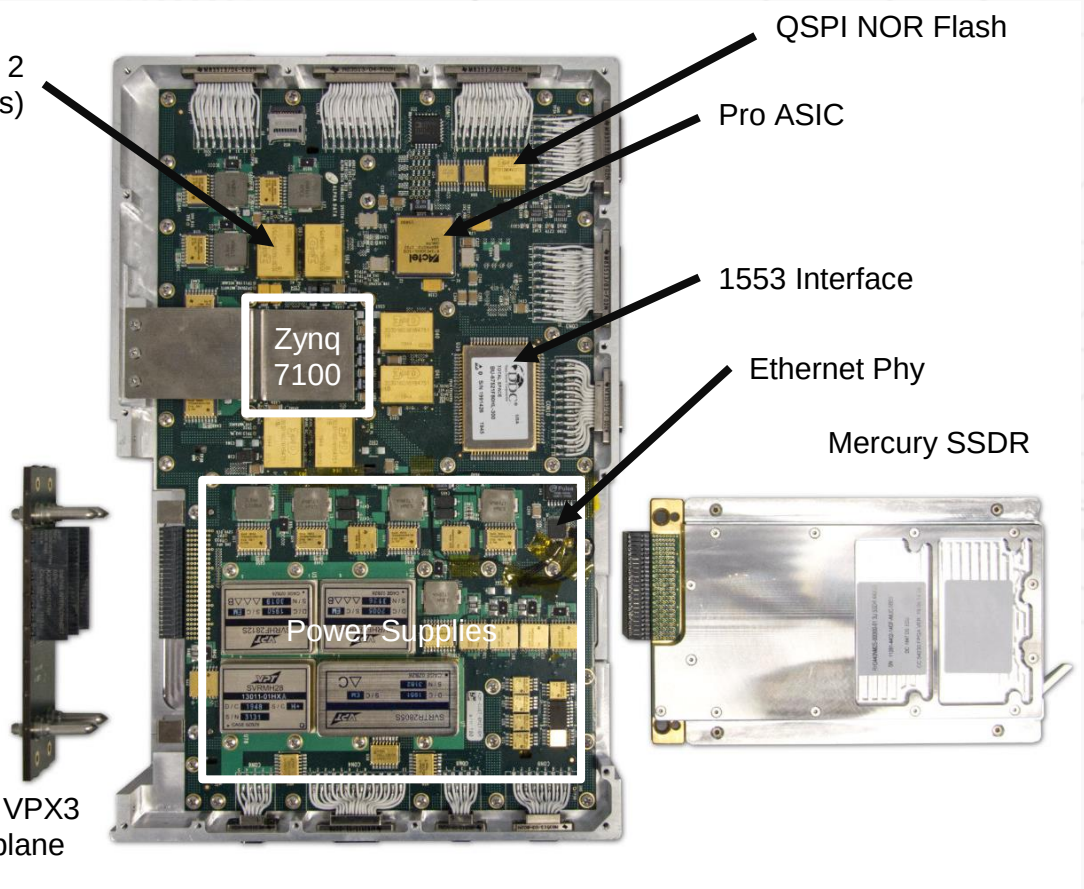
FPIE-D Hardware



3U Space VPX Bay



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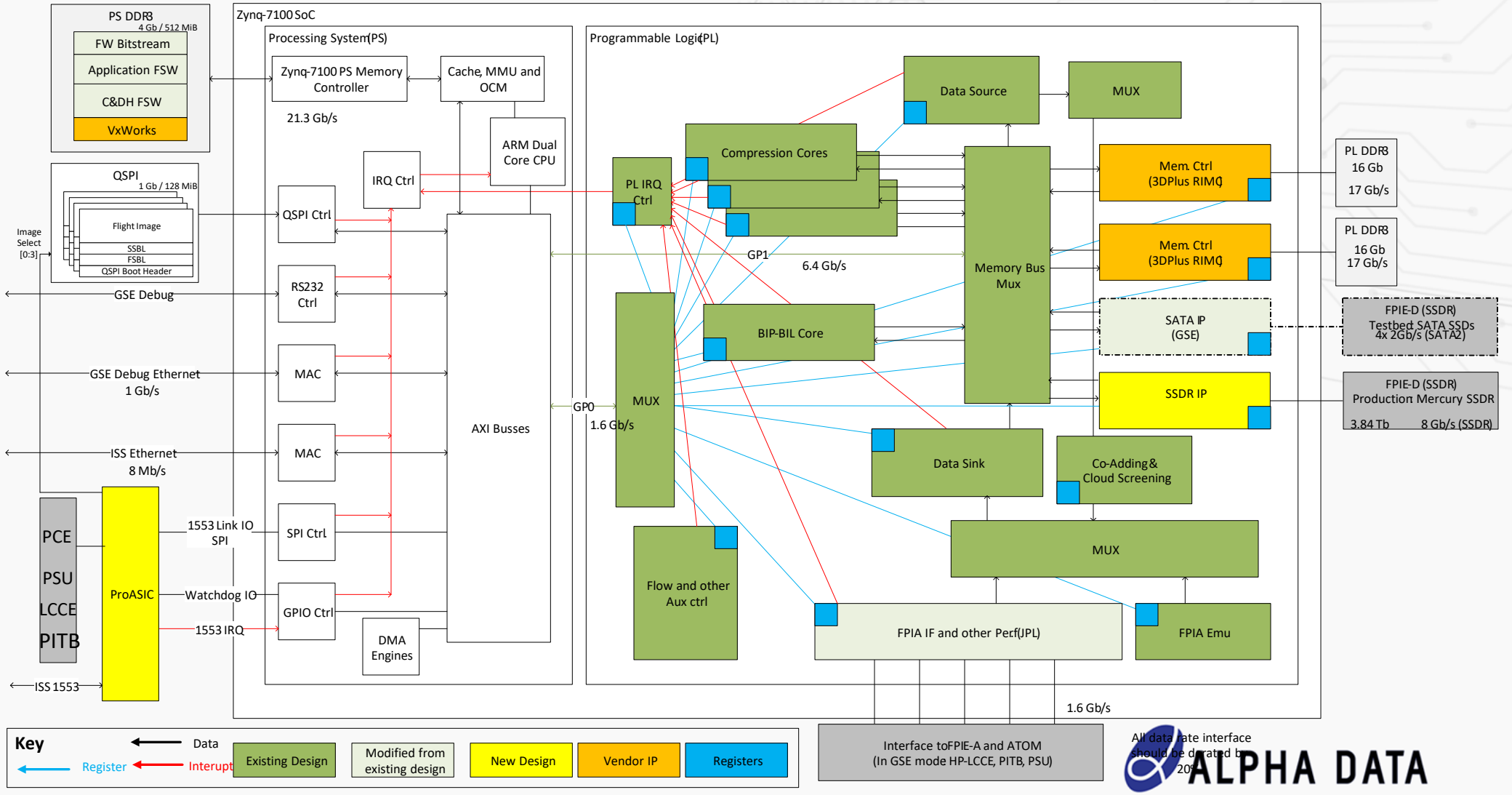
EMIT: SoC configuration and FPGA design



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EMIT: Design Challenges

- Zync-7000 was not a Space Grade Part. It was up screened.

  Cost/Weight/Size where the main reason at the time it made sense to use Zync-7K.

- After the project was underway, radiation testing showed the Zynq-7100 has SEU at a rate in OCM and L1/L2 cache that was unacceptable to the project.

  Solution Disable Cache and OCM (after FSBL execution).

  Forced UP CPU config (single core) (L1. cache is needed for SMP support in Zynq, AMP too complex/risky to pivot to).

  Running CPU without cache is slow, but this was still fast enough, as the heavy lifting is done in the FPGA.

  UP core configuration undid plan to isolate the main application code for the C&DH code on separate CPU cores.

- Bulk storage availability at time of design was hard to find:

  Mercury's SSDR drive provided this as a complete package with a

  VPX 3U Interface.

Will Versal have the same issues? …

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Versal for Space

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Versal Key Features for Space

If you are not already:
Get excited about Versal

Versal is System on a Chip. Combining: FPGA, Processors, Memory Controller, and more, but also brings key feature useful for Space Applications:

- APU: Application Processor: Dual-core Cortex-A72. Both L1 and L2 cache include Parity and ECC.
- RPU: Realtime Processor: Dual-core Cortex-R5F, with Lock Step execution capability. L1 cache and TCM (Tightly Coupled Memory) both including Parity + ECC. - Run your critical code here!
- PMC: Platform Manger Controller: Manages configuration and health of the Versal Platform. Runs on a set of Triple Modular Redundant Micro Blazes. software for these can be customed! – Put your most critical items here.
- Massive FPGA fabric on the VC1902! (Nearly 3x the size of a KU060)
- NoC, programmable interconnect, for harden peripheral, and soft peripherals. (possible to create redundant routing paths, for critical systems.)
- XilSem configuration scrubber: Protects the chips configuration at runtime
- Tested for Space: Immune to single event latch up.
- Used in automotive SAE Level 3 and higher, ISO 26262 compliant. Suitable for ASIL-B or ASIL-D applications.
- Intelligent Engines: An array of up to 400 SIMD VLIW vector processors. Allows multiple simultaneous kernel execution. Has routing for steaming data in and out of the FPGA fabric (in addition to interaction with DDR)

Versal for Space (Currently in two flavours)

Versal has scalable compute, suitable for applications in the range of ~4W to ~100W.

Versal AI Core 1902

- Applications in the range of 20 to 100 W
- 1.968M Logic Cells (~x3 KU060 FPGA)
- 164Mb of BRAM/UltraRam
- 1968 DSP Engines
- No Accelerator RAM
- 400 AIE SIMD VLIW Processors
- 100 Mb AIE Memory

Versal AI Edge 2302

- Applications in the range of 4W to 25 W
- 329K Logic Cells (~0.5x KU060)
- 49Mb BRAM/UltraRam
- 464 DSP Engines
- 32Mb Accelerator RAM
- 34 AIE-ML SIMD VLIW Processors
- 85Mb of AIE-ML Memory

Note: Using the NoC and Hardened Memory controllers saves a lot of fabric!

- Using the NOC for communication between FPGA IP save a lot of FPGA fabric otherwise needed to create busses in the FPGA fabric.
- Saves resource, and faster place a route times ☺
- No timing problems on busses between IPs ☺
- Also have capability of creating redundant routing paths and set QoS ☺

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What EMIT might look like designed with Versal

Not indorsed by JPL

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Choosing a chip and a board

Let's imagine we are going to build a system with a sensor from today that brings in data at 16 Gib/sec.

Mercury has a off the shelf 3U VPX module that can exceed this requirement. We can still use an off the shelf module for storage, it needs 8 GTY lanes (no problem to interface with the 2302). ☺

We have a 10x faster downlink now, Ethernet 100Mib/s. (Versal has a hardened peripheral for this) ☺

JPL's FLEX compression core is now faster, using 1/5th the number of clock cycles, but we still need double the number of compression core instances (to compress at the same rate relative to the input).

Let's compare the Z7100 with the Versal VE2302 and see if it's suitable:

7100	VE2302
444K Logic Cells	329K Logic Cells
26.5Mb BRAM	49Mb BRAM/UltraRam
	32Mb Accelerator RAM
	34 AIE-ML SIMD VLIW Processors
	85Mb of AIE-ML Memory

AIE-ML could be used to do some detection of interesting data onboard

On first look the Zynq 7100 has a larger FPGA. This is true, but a substantial part of the original FPGA design was bus routing, and the memory controllers. These can now be implemented in the NoC and the hardened memory controllers (20-30% of design). With this in mind we are good fabric wise with this chip ☺

The limiting factor on the compression data rate was how many compression cores could be instanced. We have about double the number of BRAM/URAM primitives, this should let us double the core count ☺

Alpha Data has a 3U VPX VE2302 which could use a standard backplane to reduce cost and risk ☺

VE2302 looks large enough, but does it solve the other challenges EMIT had?

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  Running CPU without cache is slow.

  This was still fast enough as the heavy lifting is done in the FPGA.

  UP core configuration undid plan to had a SMP configuration with one core for the application, and one for C&DH.

- Bulk storage availability at time of design was hard to find:

  Mercury's SSDR drive provided this as a complete package with a VPX 3U Interface.

Solved! Space Grade Versal Part,

Solved! ECC & RPU + APU

Solved! There are more options now, and faster version of the previously used one

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Will Versal have the same issues: NO

Other Versal Example Applications

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Tuneable Laser Gas Spectrometer (Customer Project)

A Space Customer designed a Tuneable Laser Gas Spectrometer for the VE2302. The prototyped a proof of concept using a VC1902. (VE2302 was not available at this time).

The design utilities the PL partition on the FPGA to drive a pair of DACs and capture data from a pair of ADCs each running at 100MHz @ 16-bits.

The design makes heavy using of BRAM used for modulation, demodulation, and accumulation of acquired data. The design also use of a large FIR filter (1024 taps).

The APU runs at 1.2 GHz running a Linux based operating system a SMP dual core configuration.

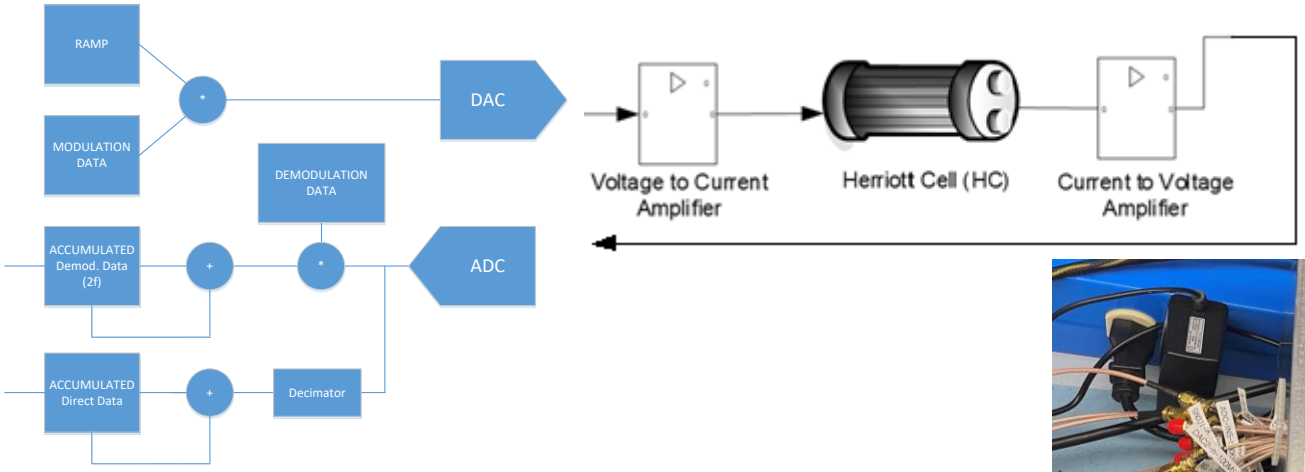
The estimated VE2302 power consumption was 8W @ worst case operating point of 80 degrees C.

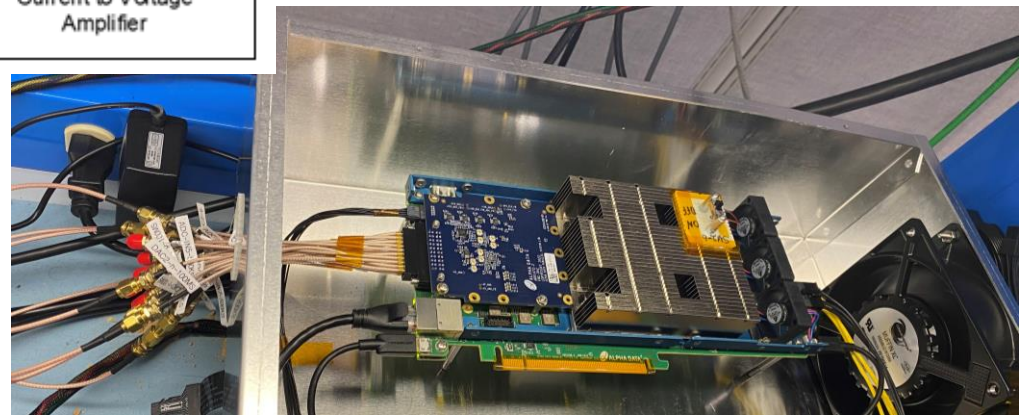
Scope for extension to use AIE-ML engines for gas recognition, via convolution-based algorithms.

Application: Decent landers / probes, and astronaut environmental monitoring.

VE2302 Device Usage:

LUT	11%
LUTRAM	4%
FF	7%
BRAM	55%
URAM	10%
DSP	56%



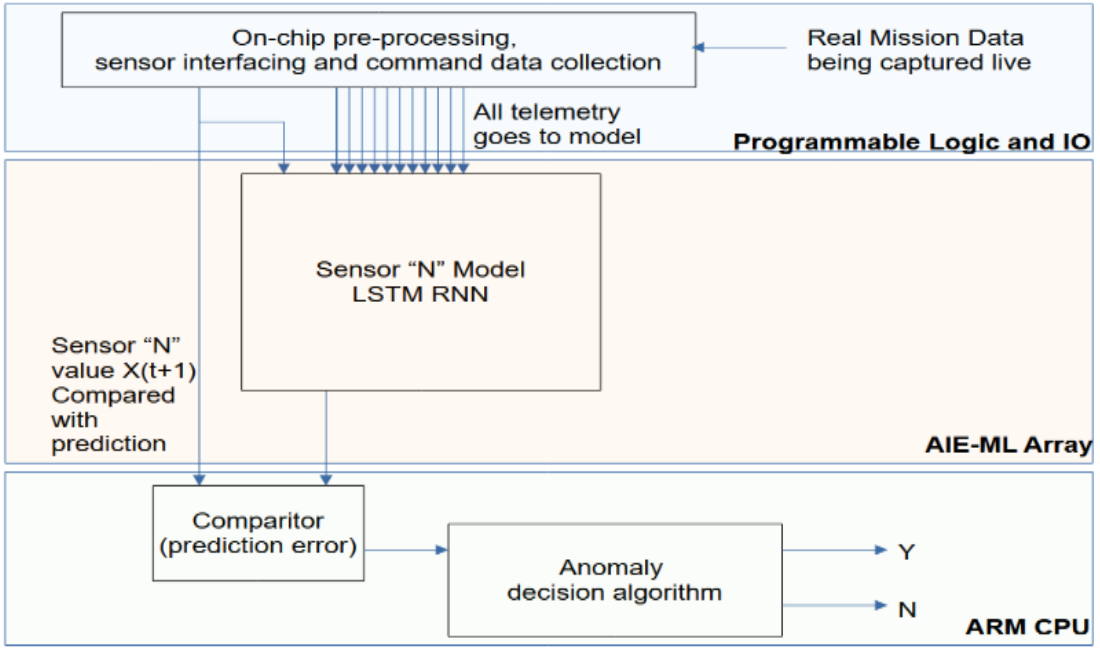


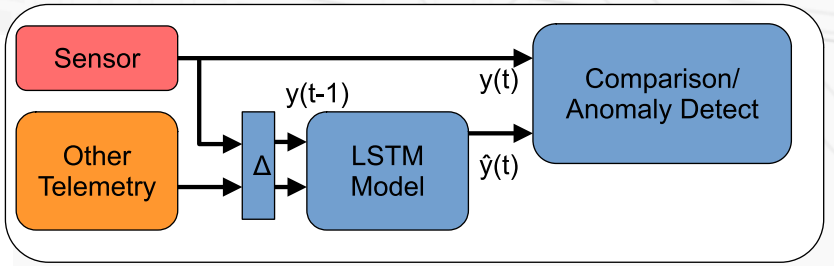
On-Board Sensor Anomaly Detection (Example Design)

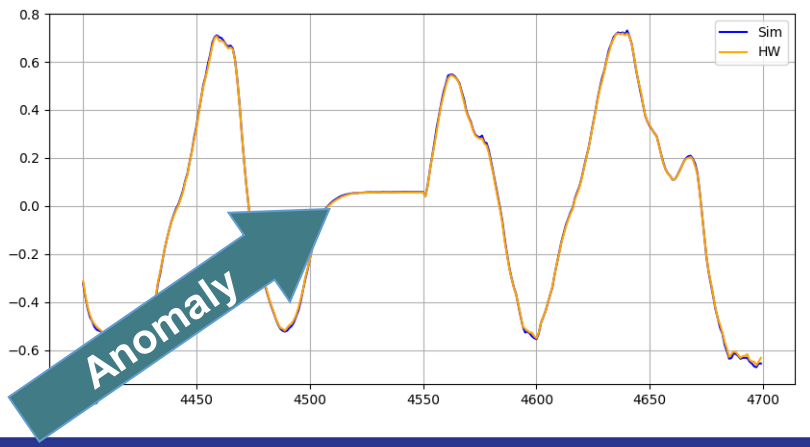
Developed with AMD to show AI Space application for VE2302

- Makes good use of Versal architecture
  - PL used for sensor interfacing: Captures data, and pre-processing input.
  - AIE-MLs are used for AI model implementation (LSTM RNN model inference)
  - ARM CPU used for an anomaly decision algorithm

  The model prediction is compared with the real sensor data, and if the results start to diverge anomalous behavior is reported.







1-Million Point FFT port to ADM-VA601 (Example Design)

Reference design based on a 1M point FFT from AMD implemented on their VCK190 Commercial Board ported to our ADM-VA610 board (VC1902)

- Example demonstrating significant use of AI Engines
  - 352 (out of 400 used)
  - 50W AIE power used
  - 70-80W board power (without significant PL use)

- Porting process
  - Standard ADM-VA601 board file did not work out of box.
  - Customized board file created to closely match the VCK190 interfaces
  - Some TCL scripts were VCK190 specific requiring work arounds.

- Resulting application
  - 28.7 GSPS DSP performance
  - 64 parallel FFT kernels in 32-bit floating point use 352 AIEs
  - Demonstrates FFT processing capability, applicable (generally at smaller size) in many space communication and signal processing/ detection applications

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Versal Deployment with Alpha Data

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Space Reference Platforms from Alpha Data

- At Alpha Data we are experts in high-reliability and rugged board design for terrestrial applications (defense, terrestrial airspace, naval etc). We have done a couple of NRE projects (including EMIT with fully Space qualified boards).

- Aim of our Space boards on the next slides was to design, as close to Space flight ready as possible, being suitable for multiply applications.
  - All components can be fitted with a rad-tolerant version.
  - Space-Enhanced Plastic components used, as many have non-flight EP alternatives.
  - Space Ready form factor selected : VITA SpaceVPX.
  - Can be fitted with either Space VPX or Standard VPX connectors.

- We provide the full schematic for these boards, BOM and board files so you can use our board as a starting point for your own. (Also provide BSP, and power estimator).

- We would love to engage with, to turn these boards into a truly off the shelf computer for your Space Projects and get some flight heritage on these or modified versions on them.

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ADM-VA601

Versal AI Core Reference Platform for Space

SoC:	**AMD Versal AI Core XCVC1902-1MSI**
Form:	**6U 220mm deep VPX**
Front IO:	**FMC+** (GPIO + 24 GT lanes)
Rear IO:	(VPX) PCIE, 10GigE, SpW, CAN, SelectMAP
Power:	Rad-tolerant Power Solution (160A 0.8V rail) from Texas Instruments and EPC Space
DRAM:	Rad-tolerant DDR4 memory 2x 8GB (1G x 72) from Teledyne e2v
Config:	2Gb QSPI on daughtercard Config options available
Other:	Space Grade SysMon from Vorago RTM for IO Breakout & custom scrubbing Ref Designs & Schematic

Developed in Partnership with

AMD

Texas Instruments

TELEDYNE e2v
Everywhereyoulook™

EPC·SPACE

Availability: Shipping since July 2024

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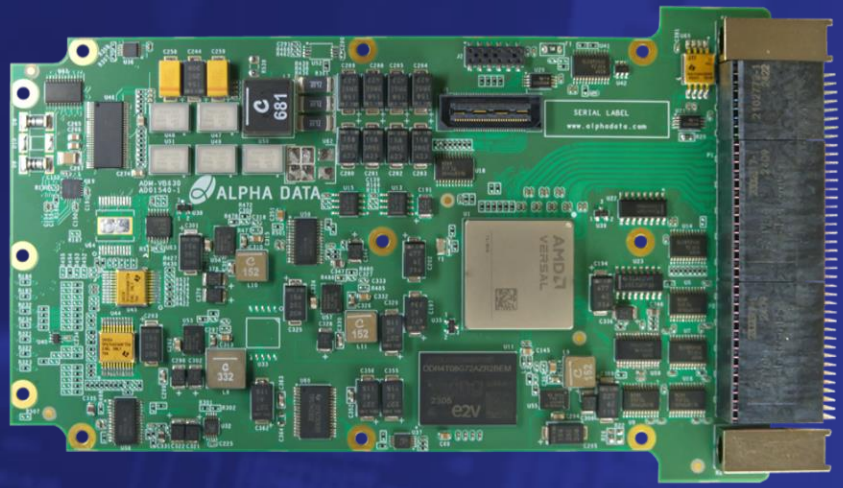
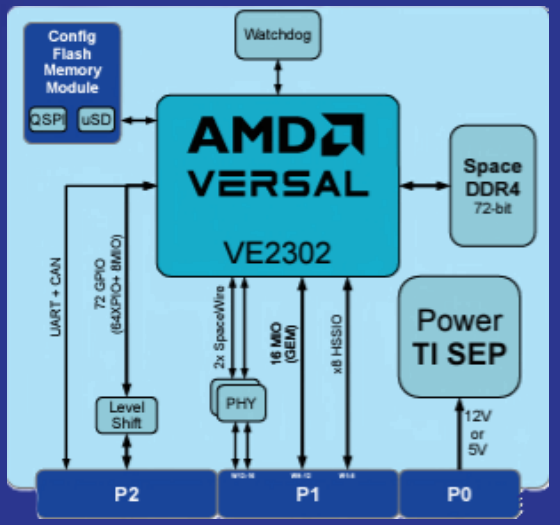
ADM-VB630 “Edge Processing Module”

Versal AI Edge System-On-Module for Space





SoC: **Versal AI Edge VE2302**

Package: SFVA784

Rear IO: 8x GTYP for PCIE/10GE/SRIO/SpaceFibre
2x Serial COM ports, RGMII, 2x SpaceWire
2x CAN bus, 56 PL GPIO, 10 PS GPIO

DRAM: 8GB DDR4 (1G x 72)

Cooling: Air-cooled, Conduction-Cooled

Applications

LEO Data Processing Unit with ML
Earth Observation
Multi-mission payloads

Availability: Development (XC) Q1’25
Flight Model (XQR) tbc

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30 Years of Innovation

Thank You

Any Questions?

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