SEFUW 2025

KBT TRANSCEIVER FOR LUNAR GATEWAY: FPGA DEVELOPMENT AND VALIDATION

MARCH 27TH 2025

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THALES-ALENIA SPACE ITALIA

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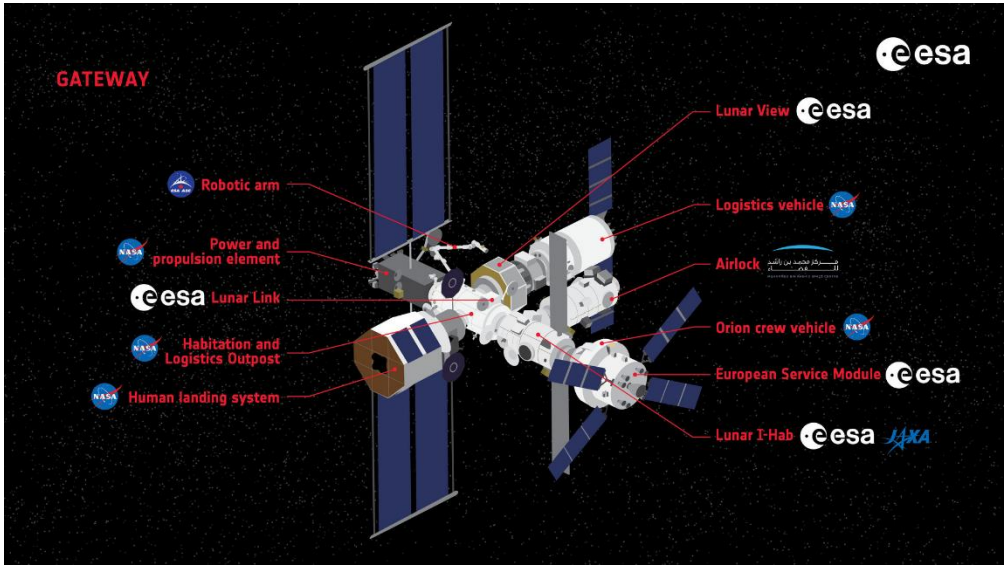
1 Introduction – Lunar Link

LUNAR GATEWAY – LUNAR LINK (1)

/// Lunar Gateway is central to the Artemis missions for returning to the Moon for scientific discovery and chart a path for the first human missions to Mars.

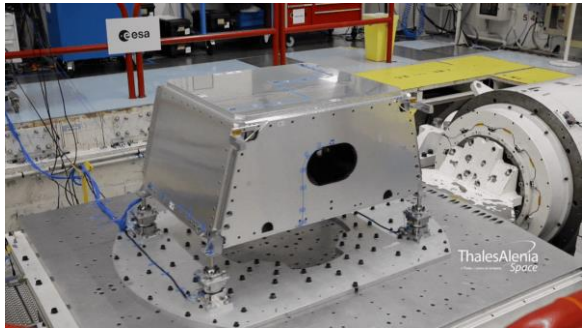
/// The small space station will be a multi-purpose outpost supporting lunar surface missions, science in lunar orbit and human exploration further into the cosmos.



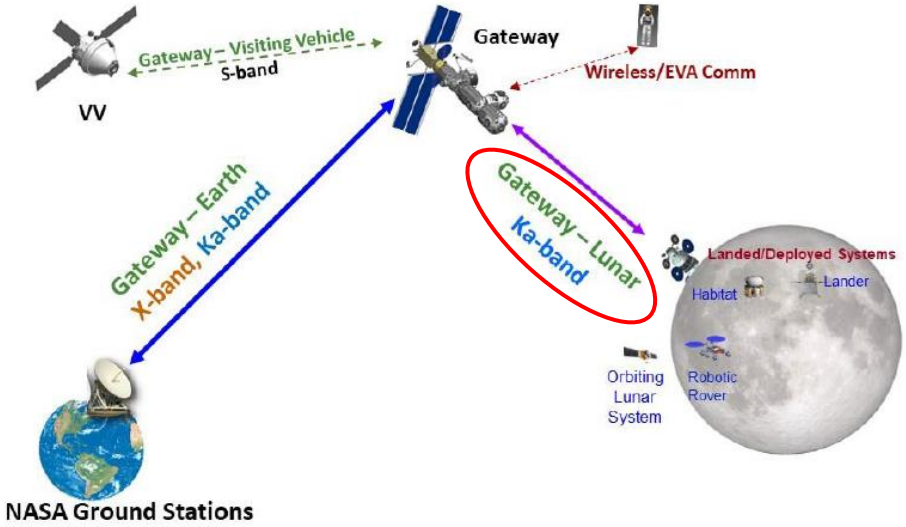
- Its flight path is a highly-elliptical orbit around the Moon – bringing it both relatively close to the Moon's surface but also far away making it easier to pick up astronauts and supplies from Earth – around a five-day trip.
- It will provide shelter and a place to stock up on supplies for astronauts *en route* to more distant destinations.
- The spaceship will also offer a place to relay communications and can act as a base for scientific research.

LUNAR GATEWAY – LUNAR LINK (2)

/// A range of data rates are needed for communication with ground and with Lunar missions to support crew communication, imagery, data relay from other systems and modules, on-board storage dumps, and science utilization.



/// The Lunar Link provides communication for lunar systems manned and unmanned stations, vehicles, and science instruments and supports real-time remote control of unmanned surface rovers from the Gateway with minimal latency.



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K-BAND TRANSCEIVER FOR LUNAR COMMUNICATION (1)

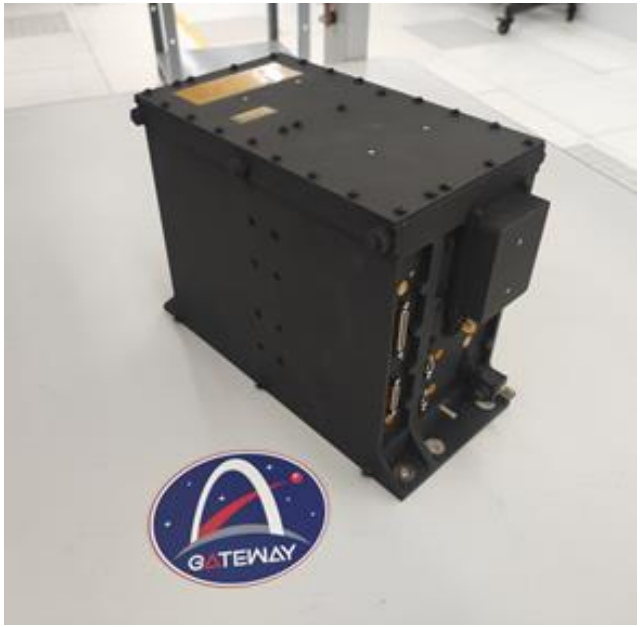
/// TAS-I has designed and developed the K-Band Transceiver (KBT) for the Gateway Lunar Link.

/// Main Features

- **Proximity link communication in K-Band (Rx: ~27.4 GHz, Tx: ~23.4 GHz)**
- **Dual-frequency capability on both Rx and Tx sides.**
- **Autonomous radio capabilities for link establishment between the Lunar vehicles and the Lunar Platform**
- **High data rate Modem:**
  - SRRC-OQPSK demodulator up to 50 Msps
  - SRRC-OQPSK modulator up to 20 Msps
- **LDPC coding/decoding and frame synchronization**
- **SpaceWire interfaces towards platform for user and housekeeping data**
- **Support to antenna pointing and tracking with accuracy better than <0.5 dB ensured by *floating point* processing implemented by embedded software**
- **Low mass: <3.5 kg**

/// Milestones

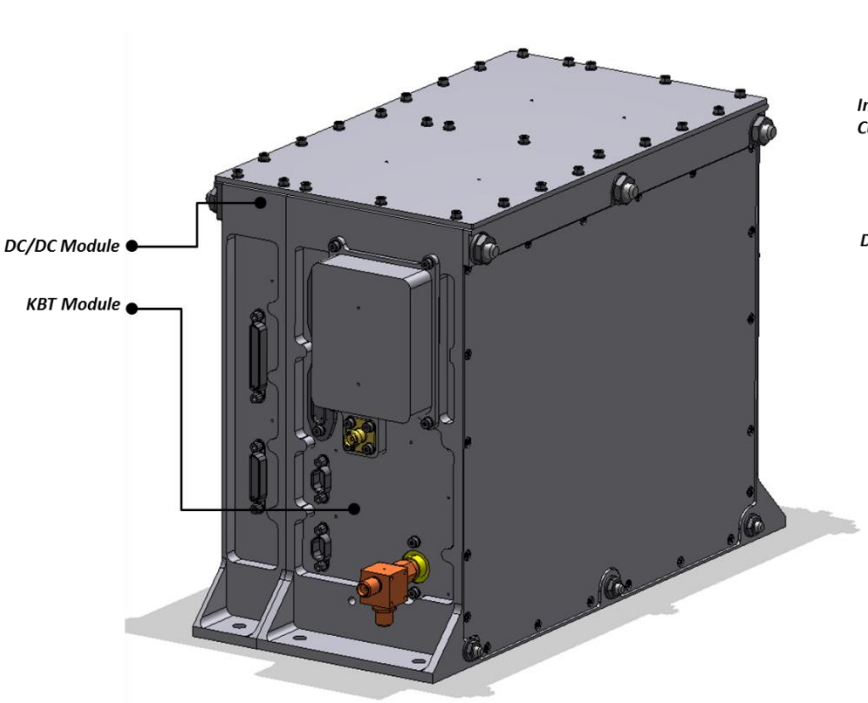
- **EM** **May 2024**
- **PFM** **March 2025**
- **FM** **May 2025**

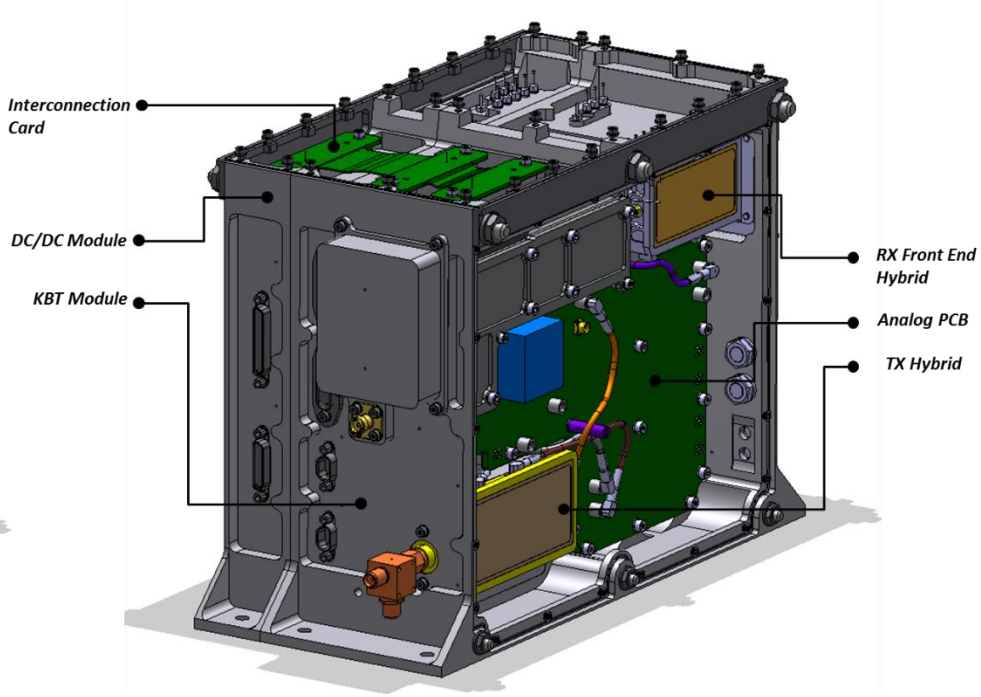


KBT Proto Flight Model(PFM)

K-BAND TRANSCEIVER FOR LUNAR COMMUNICATION (2)

/// The Transceiver has a compact implementation based on two modules, i.e. DC/DC Converter and K-Band housing RF and digital sections:





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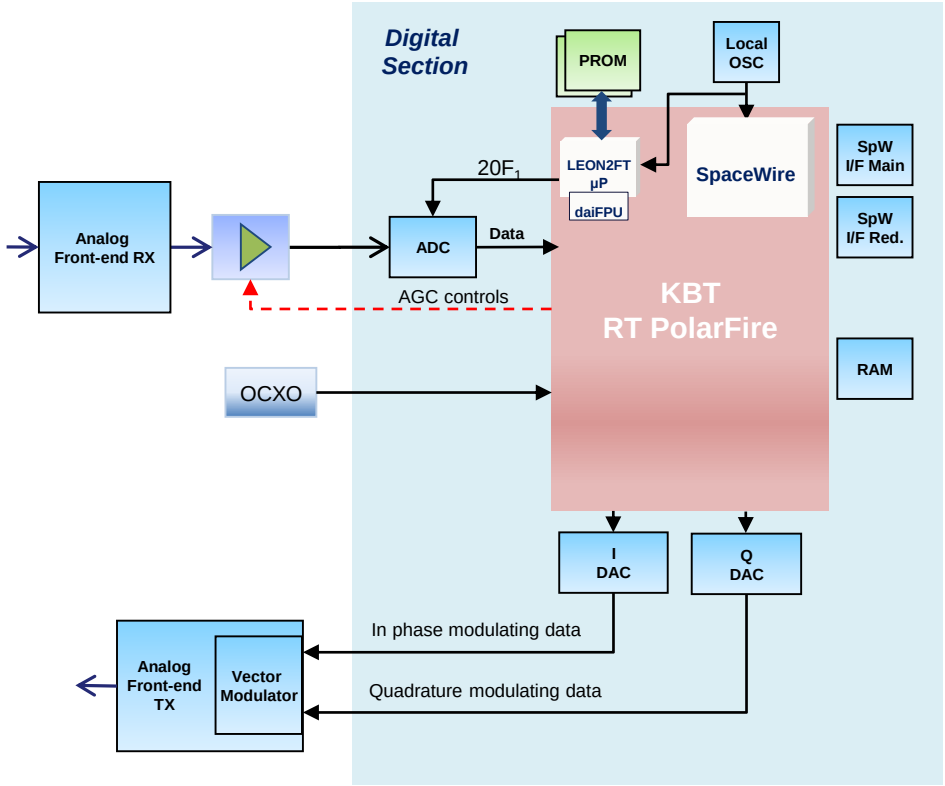
K-BAND TRANSCEIVER FOR LUNAR COMMUNICATION (3)

/// Architectural design

- Receiver section based on a single frequency conversion from K-Band to IF (=150 MHz) and downsampling.
- Transmitter section based on direct X-band synthesis followed by a frequency conversion to K-Band.
- Frequency synthesis based on OCXO and state-of-art Fractional-N PLL offering superior phase noise performance in K-Band.
- Digital processing implemented in state-of-art RT PolarFire FPGA hosting a LEON2FT embedded processor for low rate task and floating point operations.
- Secondary voltages distribution is based on a new generation of DC/DC Converter able to supply RF and digital circuits fully complying to relevant requirements.



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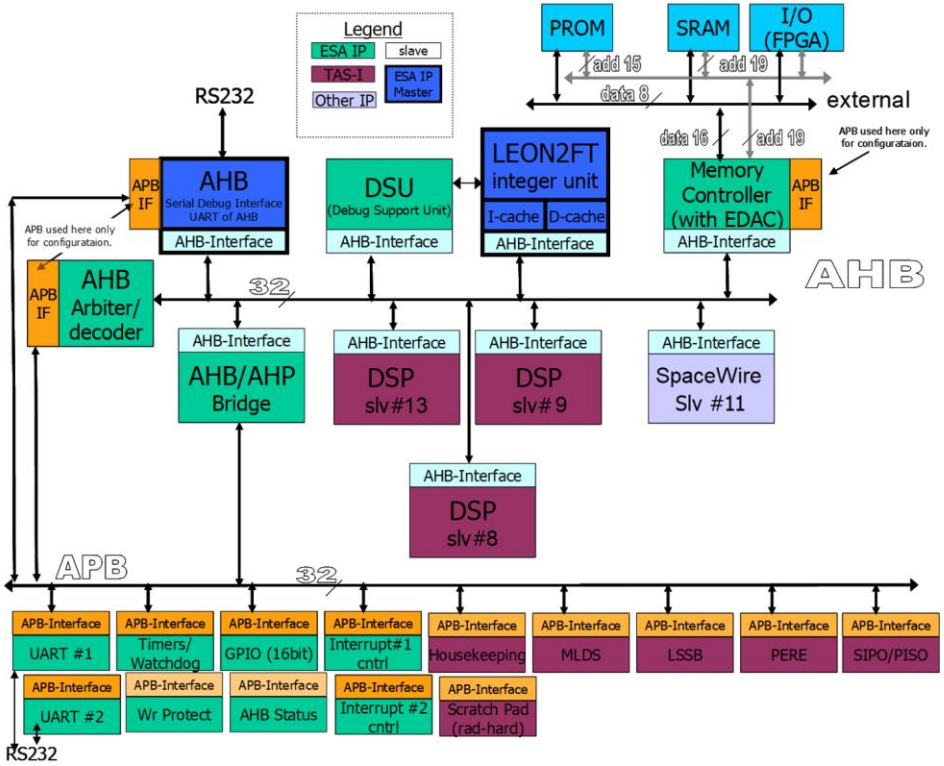
FPGA ARCHITECTURE

/// **All modules communicate with the LEON2FT Processor through the AMBA 2.0 on-chip bus architecture. The AMBA bus is the "backbone" of the entire FPGA architecture. Its highly configurable and modular structure make it an easy and robust design "platform".**

/// **This interface strategy offers many advantages:**

- It allows the portability of the DSP modules.
- Adding or modifying such blocks is carried out in a very easy and standard way.
- Access to the Integer Unit and peripherals are made easy using the well-defined AMBA standards.

/// **The AMBA bus is divided into the AHB (high-speed bus) and the APB (low speed-bus). The APB bus is access through the AHB-to-APB Bridge.**



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FPGA MAIN FUNCTIONS

/// **LDPC Encoding/Decoding function using an off-the-shelf IP duly optimized for the specific application.**

/// **Rx data demodulation is based on a Gardner's loop designed in cooperation with University of Rome – Tor Vergata.**

- Return link coded symbol rates are configurable on-board from 2 to 50 Msps.

/// **Tx data processing includes baseband shaping. The in-phase and quadrature streams are delivered to the relevant DAC in view of the vector modulation performed in the RF module.**

- Forward link coded symbol rates are configurable on-board from 2 to 20 Msps.

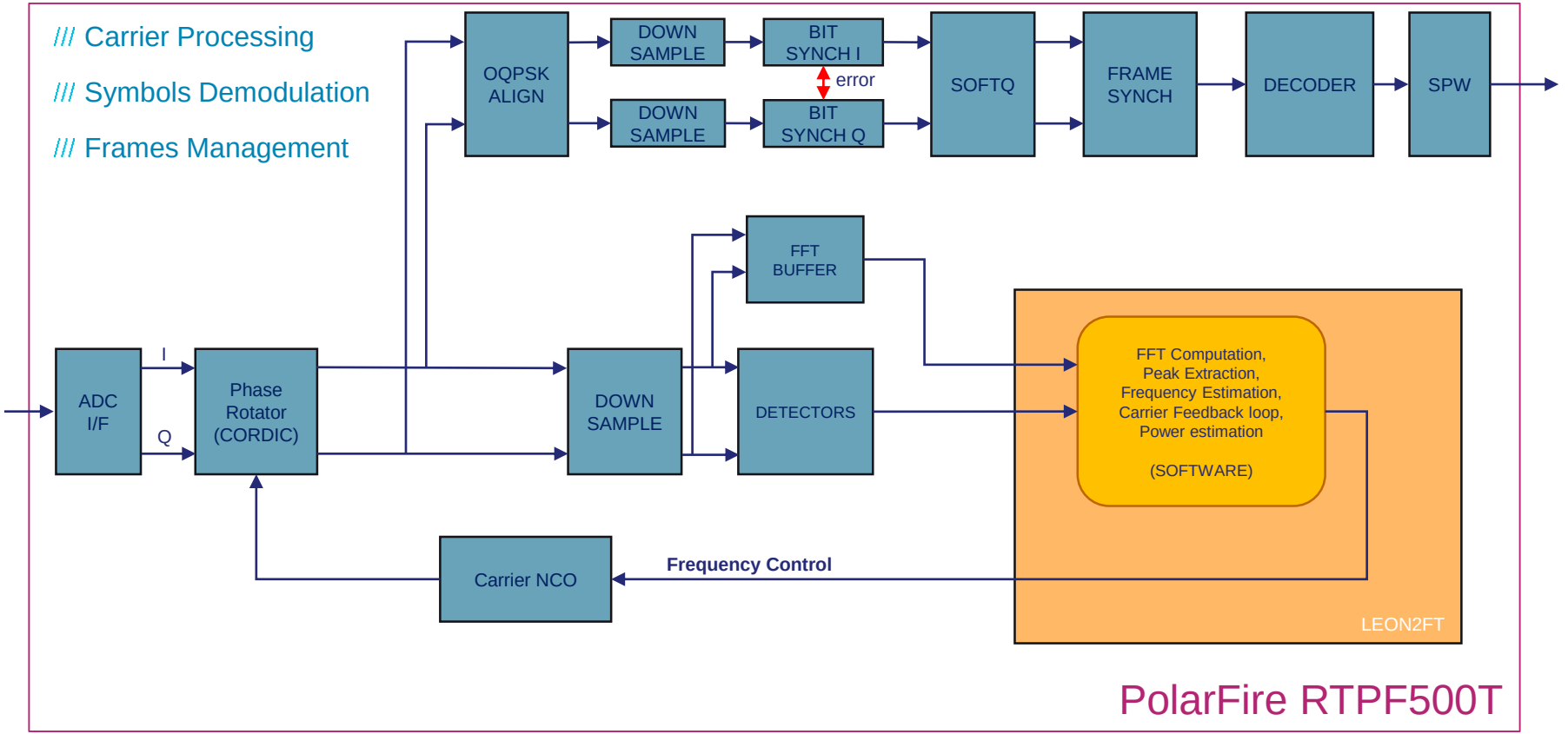
/// **Local sweeping on the transmitter side for autonomous establishing of the Lunar link**

/// **Interface with On-Board Computer is based on SpaceWire protocol used for the first time in TT&C application.**

/// **The KBT SoC embeds the LEON2FT Processor that is in charge of equipment-level management and low rate signal processing tasks.**

- It also includes the “daiFPU” Floating Point Unit (from daiteq s.r.o.) used to implement fine power estimation algorithms as needed for supporting the antenna pointing towards the Lunar asset. This is the first time that the daiFPU IP is used in a space applications.

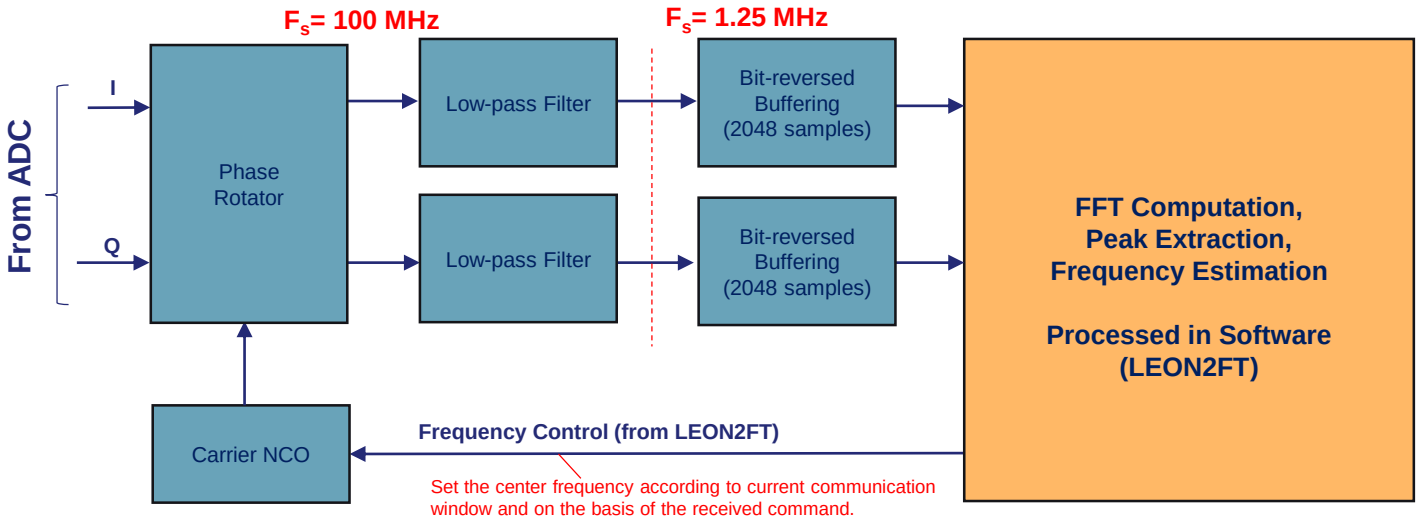
SRRC/OQPSK RX PROCESSING



FFT PROCESSING (1)

/// DSP Overview

- The digital samples at Phase Rotator output are low-pass filtered by a Low-Pass Filter
- The Low-Pass Filter output are stored in two buffers, one for the in-phase and one for the quadrature arms, of 2048 complex 12-bit samples (24 total).
- In order to speed-up the FFT post-processing, the buffering shall be performed in *bit-reversed* ordering.



FFT PROCESSING (2)

/// The following tasks are performed by the firmware routine in charge of the FFT:

1. Read the I and Q samples from the relevant buffers
2. FFT computation:
   - X=fft(I+jQ), *complex spectrum*
   - S=abs(X), *amplitude spectrum*
3. Search for the maximum in the FFT *amplitude* spectrum (index = m_k, amplitude = S_M,)
4. Comparison of S_M with a pre-defined threshold
5. In case the threshold is passed then the best estimate frequency is computed as:

$$\delta = \frac{X(m_{k+1}) - X(m_{k-1})}{2X(m_k) - X(m_{k-1}) - X(m_{k+1})},$$

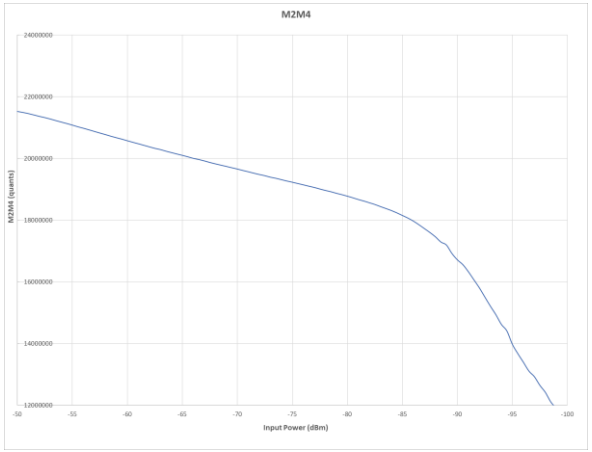
$$m_{\text{peak}} = m_k - \text{real}(\delta),$$

   - Initialize the carrier NCO
   - Start the carrier acquisition process
6. In case the threshold is not passed, restart from step 1

M2M4'S ALGORITHM

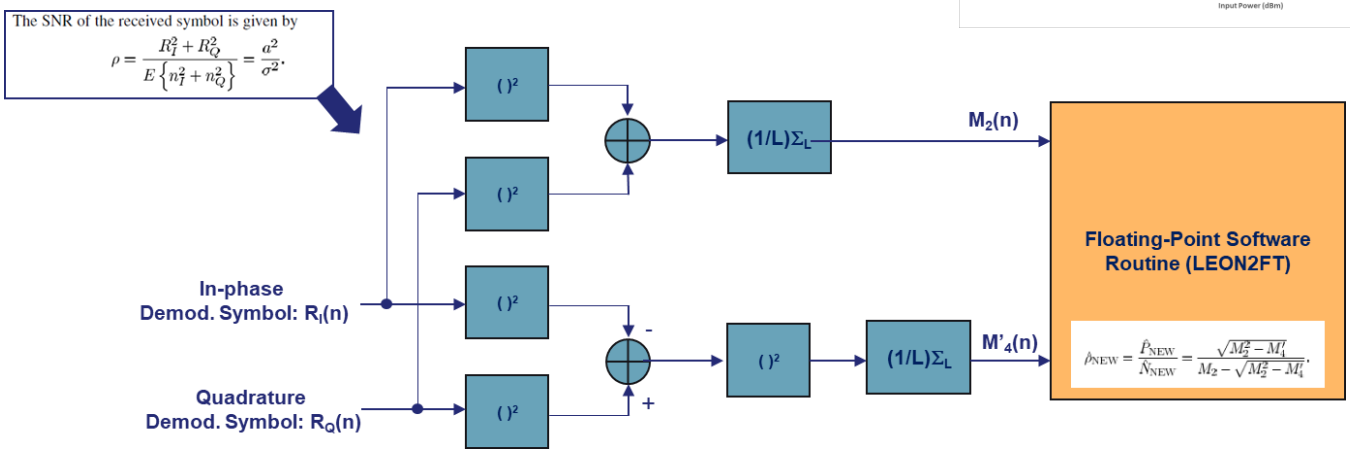
/// Power Estimation with modulated data is based on M2M4's algorithm

- When the KBT is demodulating the data, the power estimation is based on the M2M4's algorithm:
  - Power estimation accuracy: ≤0.5 dBpp for energy symbol-over-noise power spectral density down to 0 dB.
  - Integration time (L): ≥ 131072 symbols



The SNR of the received symbol is given by

$$\rho = \frac{R_I^2 + R_Q^2}{E\left\{n_I^2 + n_Q^2\right\}} = \frac{a^2}{\sigma^2}.$$

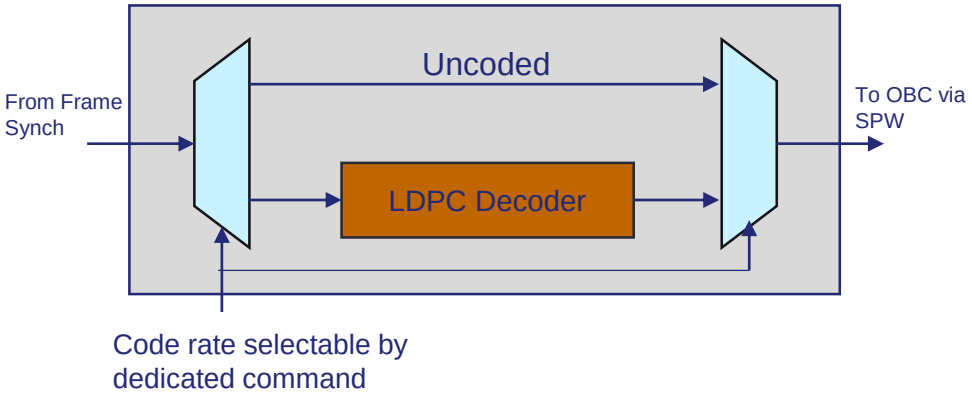


RX PROCESSING LDPC DECODER (1)

/// The KBT receiver embeds CCSDS Low Density Parity Check (LDPC) code with coding rates of:

- ½, ⅔, ⅘ k=16384 bits
- ⅞ k =7136 bits
- uncoded

The Decoder is able to process data up to 50Msps (max coded data rate)



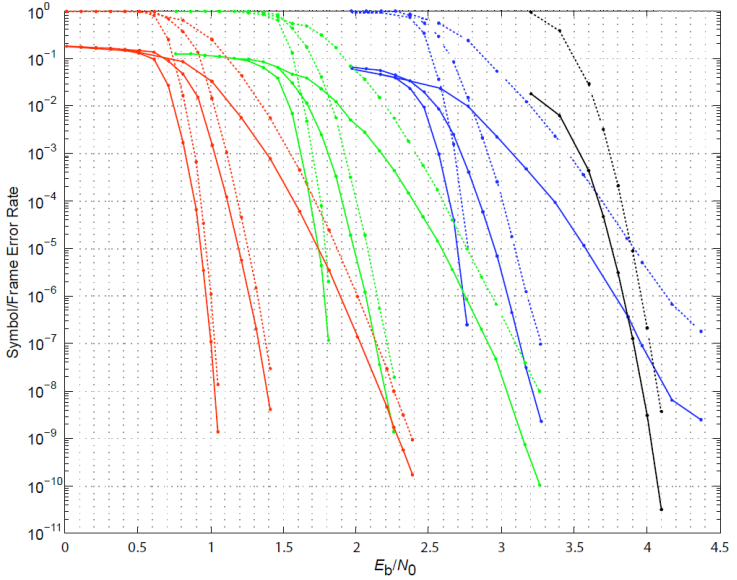
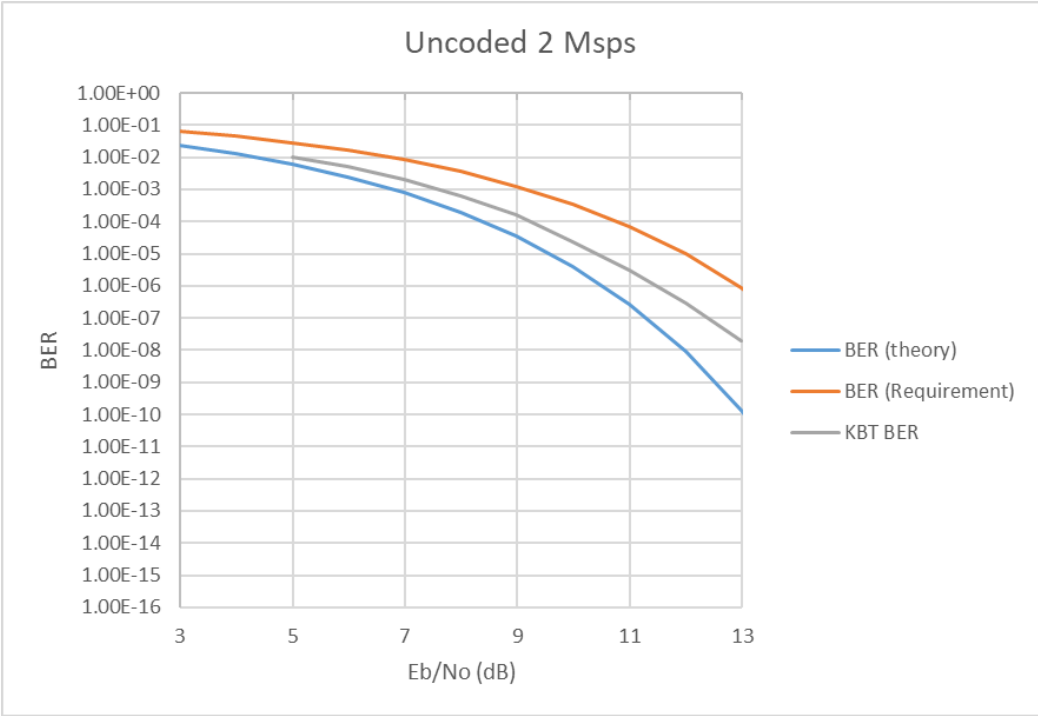


Figure 8-8: Bit Error Rate (Solid) and Frame Error Rate (Dashed) for Nine AR4JA Codes and C2, with Code Rates 1/2 (Red), 2/3 (Green), 4/5 (Blue), and 7/8 (Black); and Block Lengths *k*=16384, 4096, 1024 (Left to Right in Each Group), and 7156 (Code C2)

RX PROCESSING LDPC DECODER (2)

/// Uncoded, 2 Msps, Static carrier

- **Demodulation loss at BER 10^{-7} is slightly above 1.5 dB.**



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Ref: Not referenced
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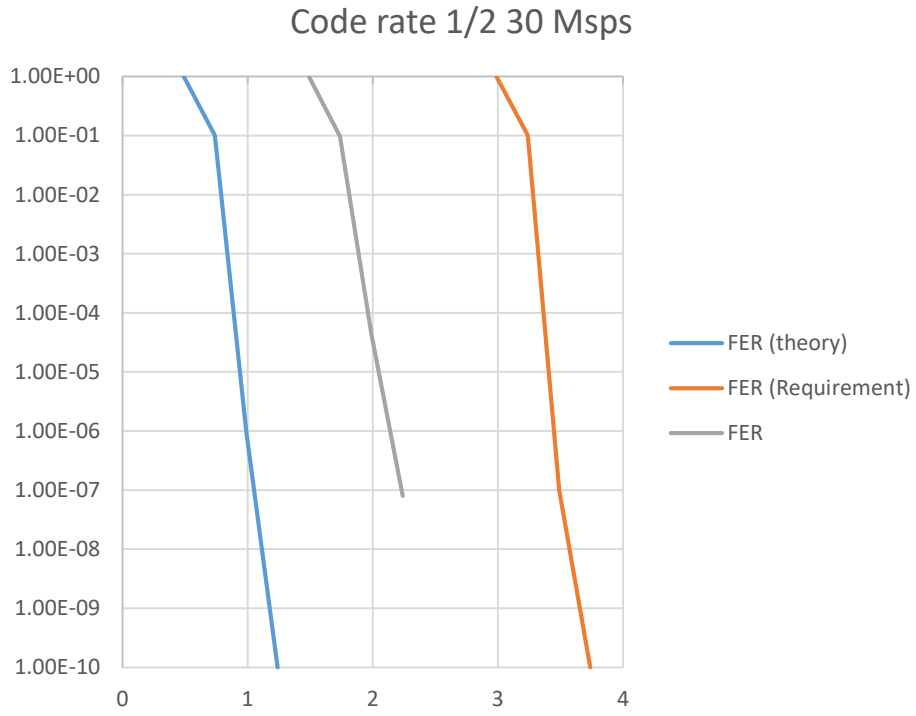
RX PROCESSING LDPC DECODER (3)



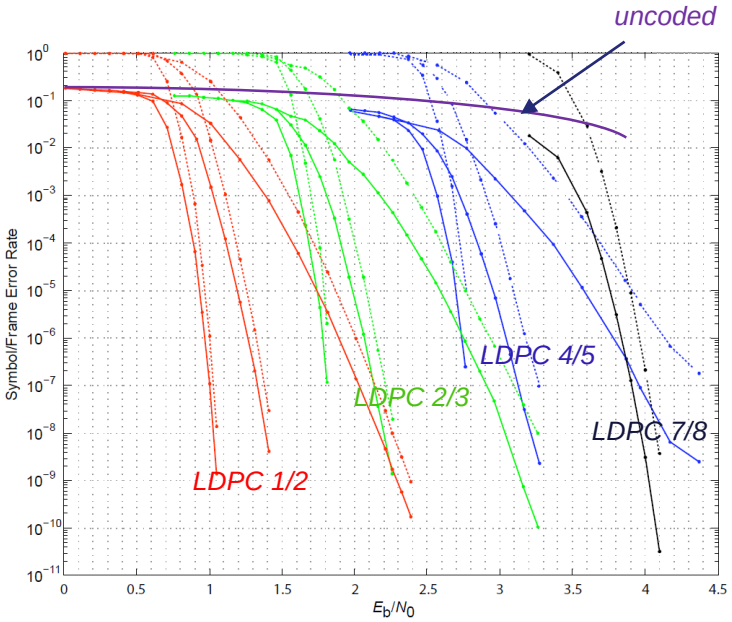
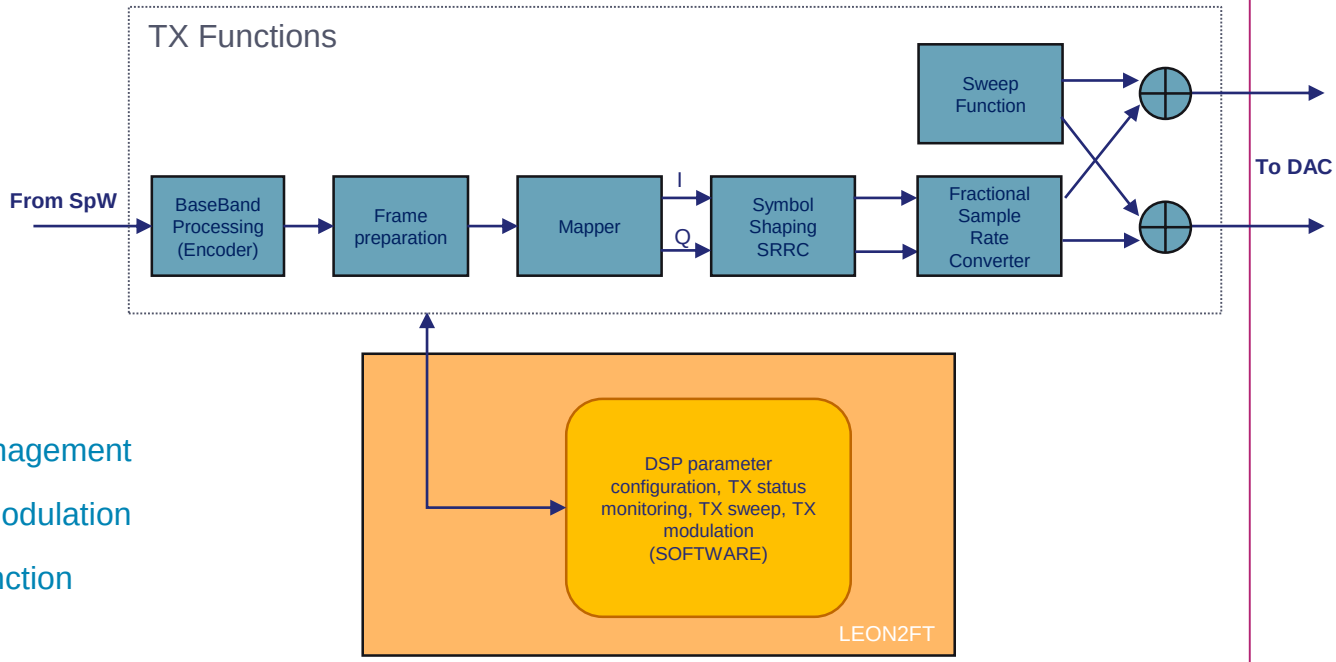


Figure 8-8: Bit Error Rate (Solid) and Frame Error Rate (Dashed) for Nine AR4JA Codes and C2, with Code Rates 1/2 (Red), 2/3 (Green), 4/5 (Blue), and 7/8 (Black); and Block Lengths k=16384, 4096, 1024 (Left to Right in Each Group), and 7156 (Code C2)

Demodulation loss at FER 10^{-7} is about 1 dB.

TX PROCESSING SRRC/OQPSK TX PROCESSING (1)



/// Frame Management

/// Symbols Modulation

/// Sweep Function

PolarFire RTPF500T

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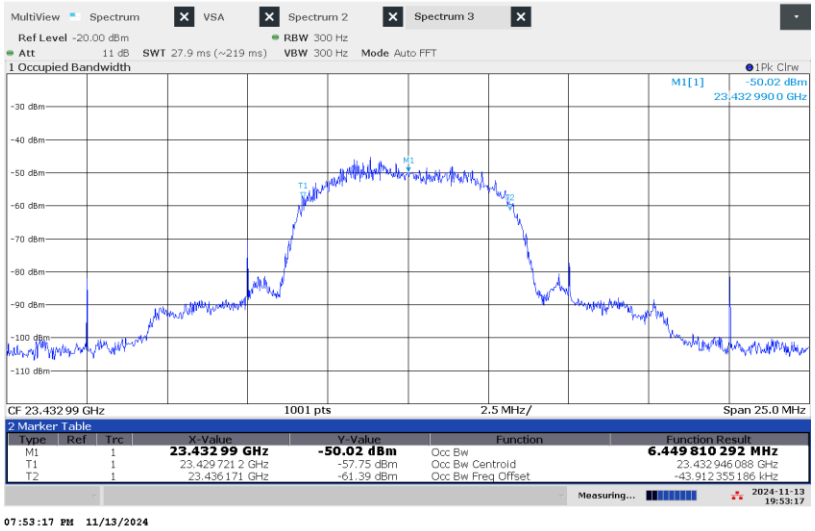
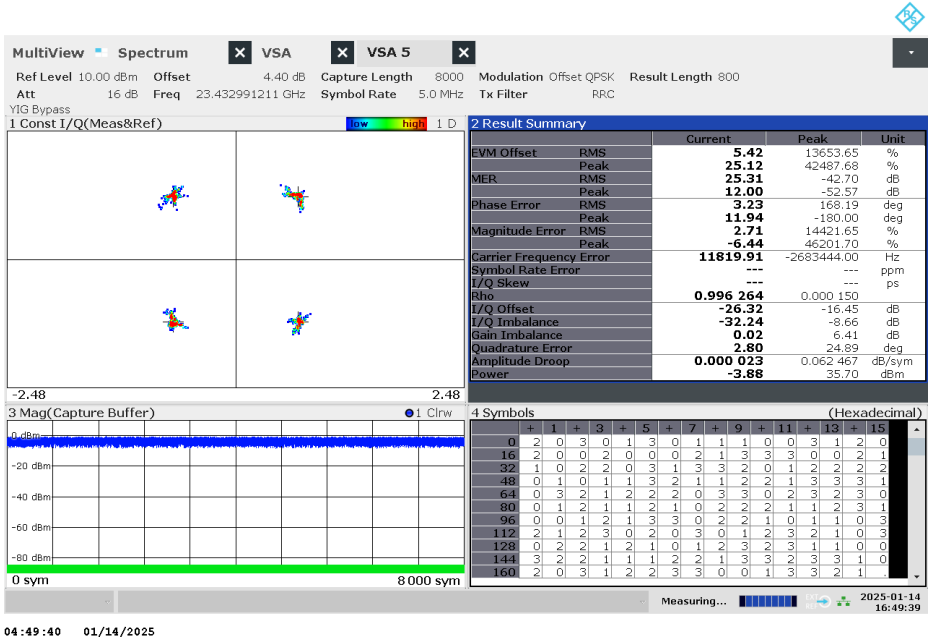
TX PROCESSING SRRC/OQPSK TX PROCESSING (2)

- **Code rate 1/2,**
- **Coded Data rate 10 Msps**
  - Occupied BW = 6.449 MHz
  - Roll-off factor = 0.5





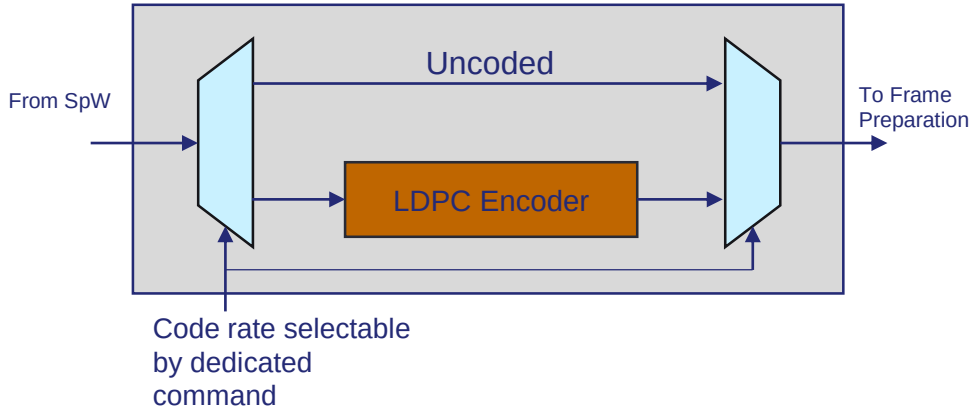
- EVM = 5.42%

TX PROCESSING LDPC ENCODER

/// The KBT transmitter embeds CCSDS Low Density Parity Check (LDPC) code with coding rates of:

- ½, ⅔, ⅘ k=16384 bits
- ⅞ k =7136 bits
- uncoded

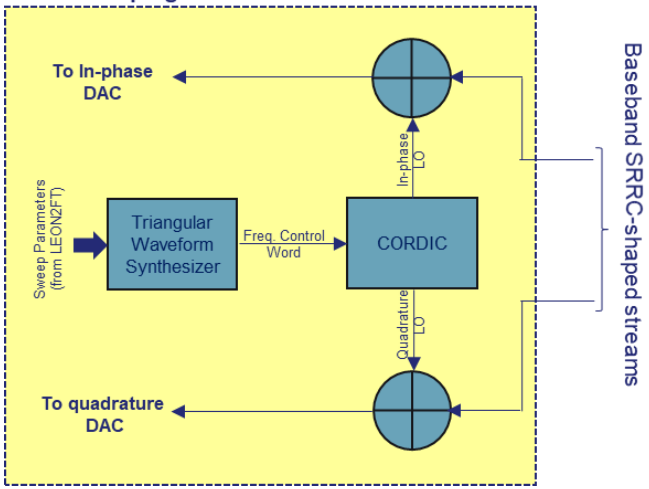
The Encoder is able to process data up to 20Msps (max coded data rate)



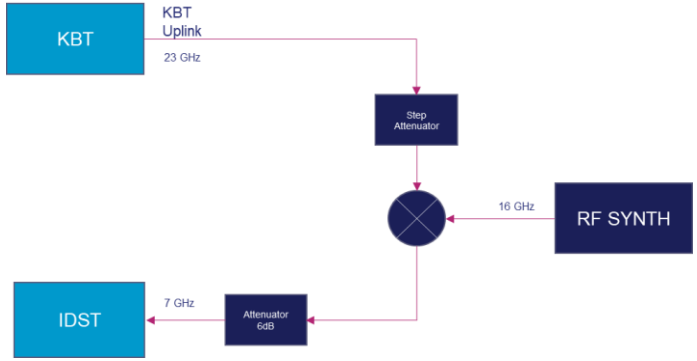
TX SWEEPING

/// Top-level block diagram

Tx sweeping block inside the KBT FPGA



- **This mode of working is needed at KBT level to establish the lock of the Lunar system receiver.**
- **KBT parameters for Tx sweeping are:**
  - Frequency Sweeping range: 10 kHz ➔ 250 kHz
  - Frequency Sweeping rate : 2 kHz/s ➔ 50 kHz/s
  - Sweeping cycles number
- **RF compatibility test for acquisition purpose with IDST (X-Band Deep Space Transponder) has been performed implementing the set-up here below:**

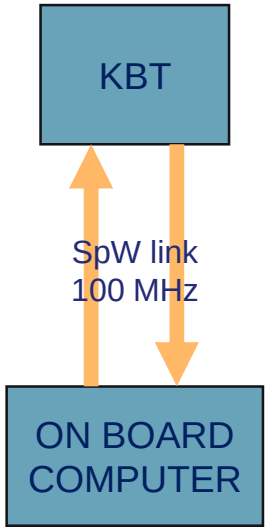


SPACEWIRE INTERFACE TO OBC

/// SpaceWire (used in KBT)

- Standardized in Jan 2003
- State-of-the-art On-Board data handling protocol
- Max datarate : 400Mbps
- No QoS and fault detection, isolation and recovery

  - This block uses the SpWB CODEC IP supplied by ESA.
  - The SpaceWire Interface block has to manage both TC/TM commands and RF traffic data.
  - The SpaceWire Interface implement a cold redundancy for RF traffic data and an hot redundancy for TC/TM commands.
  - It is mainly divided in two functional block chain completely independent: one for TX and one for RX.



FPGA PERFORMANCE AND RESOURCE USAGE

Clock Domain	Frequency (MHz)
ADC_SYSCLK100MHz	109.349
CLK_96MHZ	500
CLK160MHz	170.184
CLKLeon32MHz	44.289
CLKSPW_100MHz	111.944
CLKSPW_10MHz	80.128
CLK50MHz_ldpc	53.548

Type	Used	Total	Percentage
4LUT	307858	481272	63.97
DFF	163666	481272	34.01
I/O Register	0	1896	0
User I/O	275	632	43.51
Single-ended I/O	237	632	37.5
Differential I/O Pairs	19	316	6.01
uSRAM	289	4440	6.51
LSRAM	528	1520	34.74
Math	260	1480	17.57
H-Chip Global	31	48	64.58
Local Global	5	1440	0.35
PLL	4	8	50
DLL	0	8	0
Transceiver Lanes	0	24	0
Transceiver PCIe	0	2	0
ICB_CLKINT	7	72	9.72

- Resource usage ≃ 65%

RADIATION HARDENING APPROACH

RT PolarFire is a Radiation Tolerant FPGA, then the design needs an appropriate strategy in order to mitigate the radiation impact.

Considering the resource usage of the function implemented in the KBT FPGA, It is not possible to protect the entire design from radiation effect, then the following strategy has been implemented:

- TMR on SPW IP and LEON2FT
- TMR on critical signals (FSMs, control signals, counters, …)
- The MEMEDAC is enabled for the internal processor memories.
- Scrubbing performed on the RAM only in the sections that contain code and sensitive data.
- No mitigation strategies applied in block that not represent critical functions of the KBT.

4 Q/A

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