Politecnico di Torino Politecnico Reconfigurab	eliability Analysis of <u>SEFUW: 6th Space</u> ole Systems
CONTACTS: corrado.desio@polito.it	<sup>,</sup> Sarah Azimi, Davide Nicolini, Luca Sterpone <b>Politecnico di Torino, Italy</b>
MOTIVATION	PYXEL: A TOOLKIT FOR ANALYSIS OF RECONFIGURABLE SOCS
Reconfigurable SoC are flexible and performant radiation- sensitive, heterogenous, increasingly complex Systems. We need methodology, techniques, and experimenta flow for evaluating and assessing the robustness of System and Application based on Reconfigurable SoCs for safety-critical domains.	<ul> <li>SoC Robustness Assessment aware of SoC and System Architectures</li> <li>Emulation and Analysis of SEU and Fault Models</li> <li>Complex Evaluation Flow, Fully Integrated with modern CAD tools</li> <li>Supporting Latest AMD Devices</li> </ul>
EVALUATION AND MITIGATION FLOW	APPING BLACK BOX





Circuit	Error Rates					
CIICUII	DDC	UD	SDC	Total		
Original PaR	5.47%	1.39%	1.12%	7.98%		
Hardened PaR	2.82%	0.27%	0.00%	3.09%		



Home Vie	w Analysis Tools					
Bitstrea	m Information		Bitmap View		Hardware	View
Name	01_dma_1_wrapper.bit				Resource	Interconnections
Size	10008 x 3232		○ Plain	Resources	Туре	INT_L
Part	xc7z020clg400-1		Pesources Filters		Name	INT_L_X52Y16
Configur	ation Memory View		✓ Logic ✓ Othe	rs ✔ BRAM (Interfaces)	Configura	ation Memory Statistics
Frame	6952	Value Ø	✓ Interconnections ✓ Cloc	k Lines ✔ BRAM (Data)	1-Bit	2464900
Bit	1085	Essential	✔ Flip-Flop	✔ DSP (Interfaces)	1-Ratio	7.620 %

from pyxel import Xbitstream

Xbs = Xbitstream('bitfile.bit') Xbs.cmem.flip\_bit(42, 1024) Xbs.visualize()

#### exit(0)

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VIEW 7	nalysis Tools	
<u>,                                    </u>	E Reliability Analysis fo Programmable Hardware	r
orkspace	C:/Users/Corrado/Documents/pyxel/gui/workspace	
itstream	C:/Users/Corrado/Documents/PyXEL/gui/workspace/bitstreams/design_1_wrapper.bit	
ssential E	its	
itstream ] Family	Series7	
itstream ] Family Part	series7 xc7z020clg400-1	
itstream ] Family Part Vendor	nformation Series7 xc7z020clg400-1 ARM-Xilinx Inc. KLNX® ZYNQ™ XC7Z020™ CLG400ABX1749	
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# **ENABLE DEVICE CHARACTERIZATION AND** FAULT MODELING

- Analysis of Different **CRAM Technologies SEE** Cross-Sections, **MBU** Characterization
- Characterization of **On-Chip RAM** 
  - SEUs, MBUs, SEFIs Cross-Sections
  - MCUs based on Physical RAM Layout

16nm FINFET VS 28nm CMOS



#### PAUL SCHERRER INSTITUT

**PROTONS 40-160 MEV** 



## ZYNQ-7020 ON-CHIP MEMORY





## SUPPORT RELIABILITY ANALYSYS OF RECONFIGURABLE SOCS

Methodologies for Analysis of components of Reconfigurable SoCs

ZYNQ-7 RECONFIGURABLE SOC

2 PyXEL - Reliability Analysis for Programmable Hardware

### FIRENN: NEURAL NETWORKS RELIABILITY EVALUATION ON HYBRID PLATFORMS



- Hard and Processors, Accelerators
- Hardware and Software Stacks
- Fault Modeling and Analysis



**RTOS** SOFTWARE STACK ON SOFT PROCESSORS

AGAINST SEU AND MCU IN CRAM

**BAREMETAL VS RTOS** SOFTWARE STACK ON HARD PROCESSORS AGAINST SEU AND MCU IN OCM

