ingeniars

THE ART OF INNOVATION

IngeniArs IP Cores Portfolio: Satellite Communications, Artificial Intelligence and High-Speed Serial Links

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Outline

- **Introduction**
- **IngeniArs IP Cores Portfolio**
- **Conclusions**
- **Q&A**

Satellite Communications

Radio Frequency:

- CCSDS 131.2-B Transmitter
- CCSDS 131.2-B Receiver

Optical:

- HPE CCSDS 142.0-B Optical Transmitter
- O3K CCSDS 142.0-B Optical Transmitter

Artificial Intelligence

- GPU@SAT

High-Speed Interfaces

- SpW CODEC & Router
- SpFi CODEC & Router
- WizardLink TLK Equivalent

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Introduction

What is IngeniArs?

- SME based in Pisa, Italy
- Founded in 2014 as innovative start-up and spin-off company of University of Pisa
- Running project with ESA as prime contractor
- Official partner of Microchip and AMD, CCSDS Associated Member
- ISO9001 Certified

Space Business Fields:

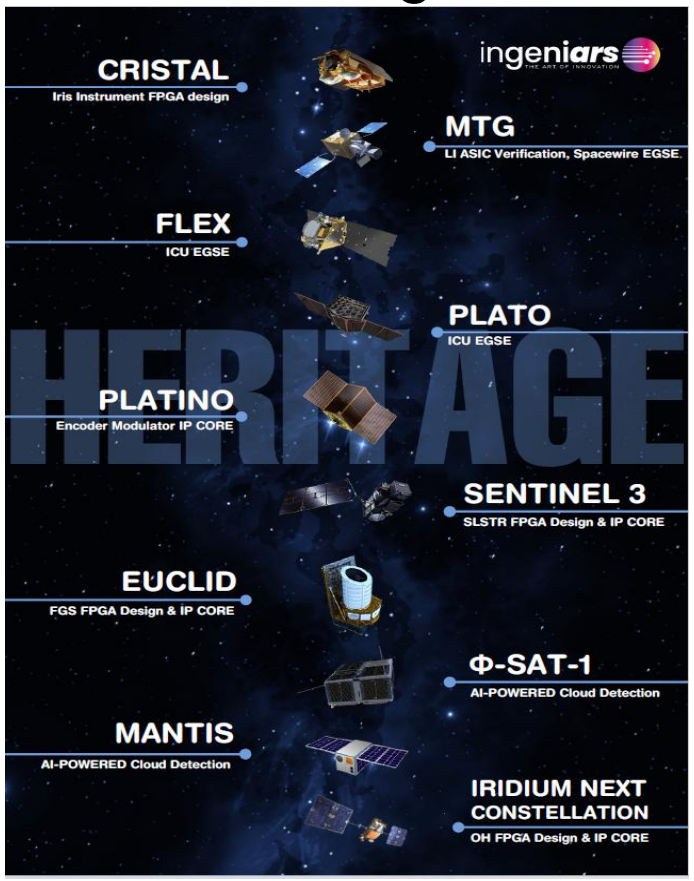
- Satellite Communications
- Artificial intelligence
- On-Board High-Speed Communication Links and Networks

Introduction

Providing expertise in:

- Flight PCB Design
- Digital Signal Processing
- FPGA/ASIC design
- IP Core design
- Software design – System modelling
- Verification

Heritage



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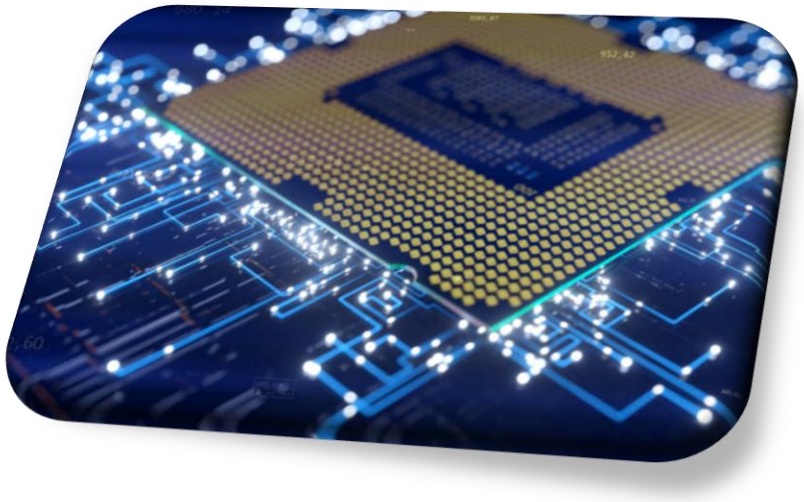
IngeniArs IP Cores Portfolio
Satellite Communications

- **IngeniArs IP Cores Portfolio**

- Developed in **VHDL** language
- Technology-Independent
- Fully verified and validated
  - 100% code coverage
- Optional features:
  - EDAC
  - Dead-lock free FSM design
- Highly configurable
- Easy integration in higher-level designs



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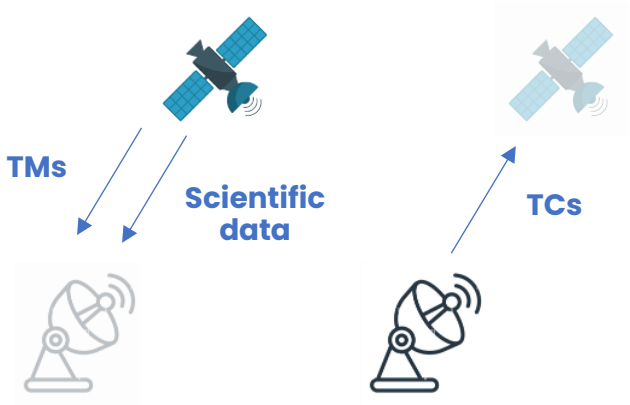
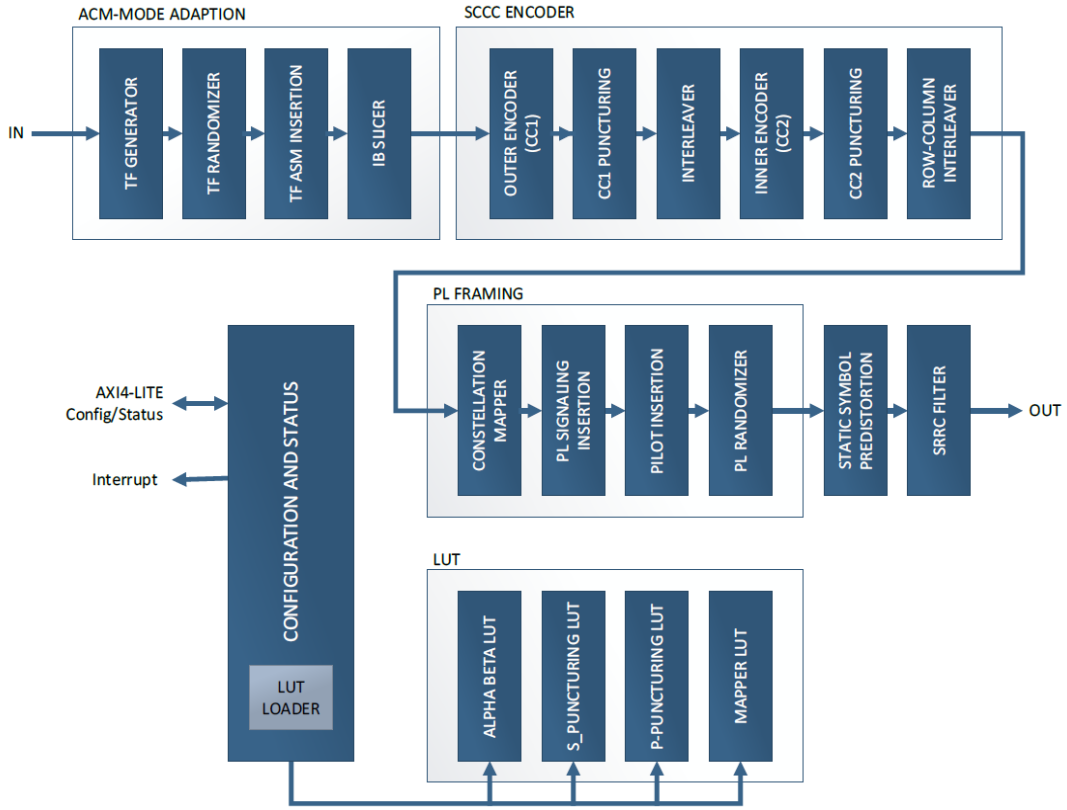
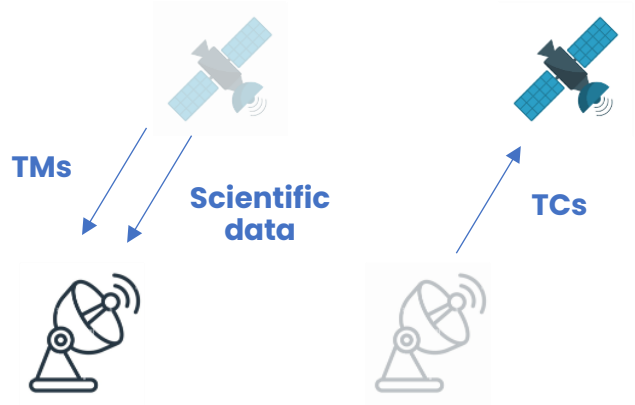


CCSDS 131.2-B Transmitter

- **Satellite-to-Ground communication in EO missions**
  - **TT&C**
  - **Payload Data Transmission**
- 27 ModCods supported (SCCC encoding , from QPSK to 64-APSK)
- Support Extended range of ModCods (128-APSK and 256-APSK, with combined SCCC/BCH coding)
- **Symbol rate up to 1.2Gbaud (6.5Gb/s)**
- Optional pre-distortion and SRRC baseband filtering
- Characterized on space FPGA:
  - Microchip RT PolarFire
  - Microchip RTG4
  - AMD Xilinx Kintex Ultrascale KQRKU060

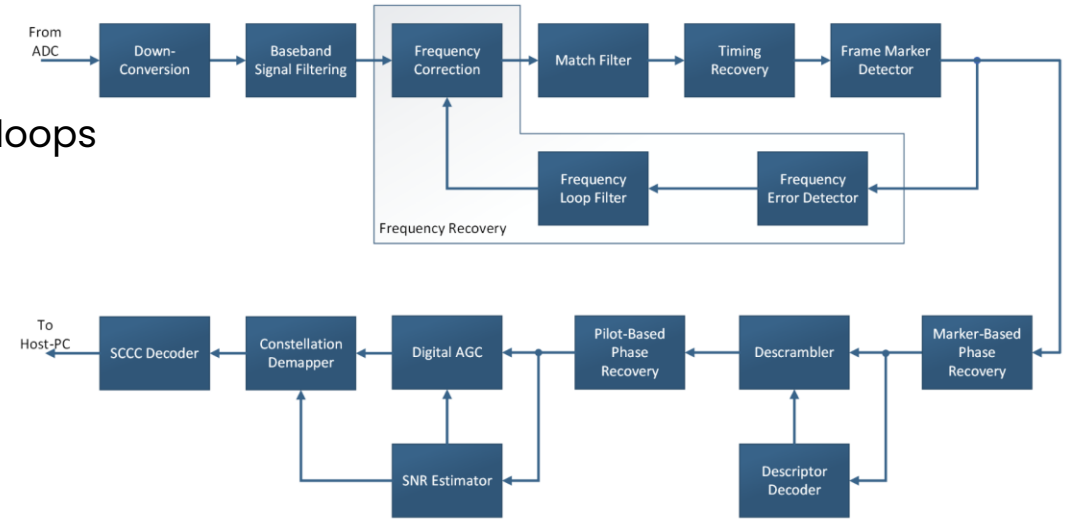


IngeniArs IP Cores Portfolio
Satellite Communications



CCSDS 131.2-B Receiver

- **Satellite-to-Ground communication in EO missions**
  - **TT&C**
  - **Payload Data Transmission**
- 27 ModCods supported (SCCC encoding , from QPSK to 64-APSK)
- Baseband I/Q signal as input frequency phase and timing recovery loops
- **Symbol rate up to 500Mbaud**
- Standard AXI Lite and AXI Stream interface, for easy integration
- Ground (Downlink) version characterized on commercial FPGAs:
  - AMD Xilinx ZynQ/Virtex UltraScale+
  - Intel Stratix 10
- Optimized Space (Uplink) version characterized space FPGAs;
  - Microchip RT PolarFire
  - AMD Xilinx Kintex Ultrascale KQRKU060



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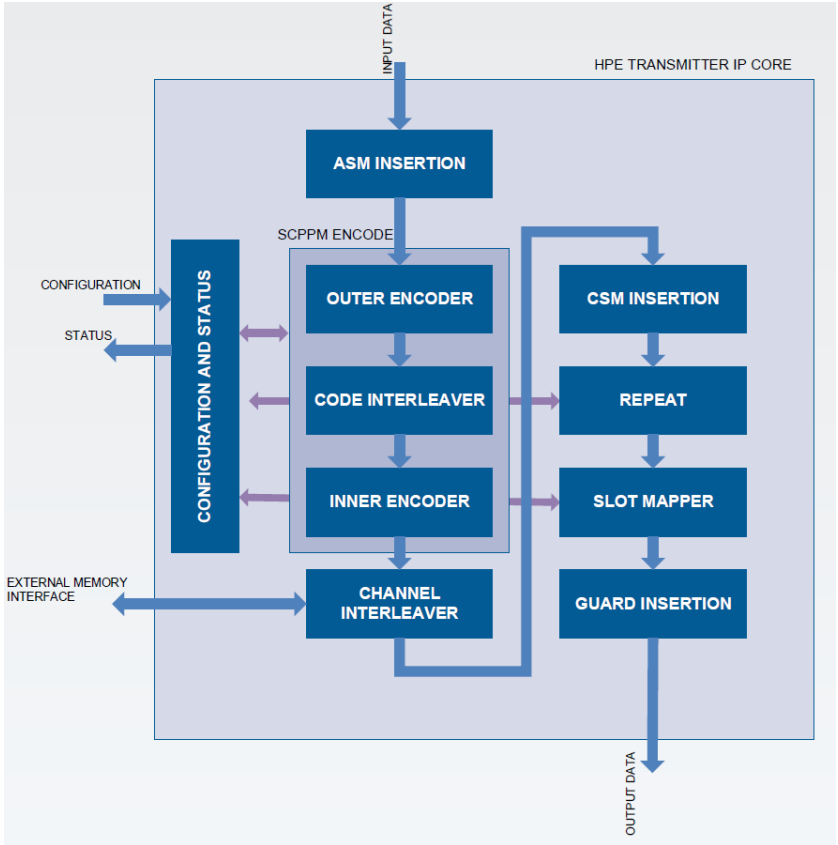
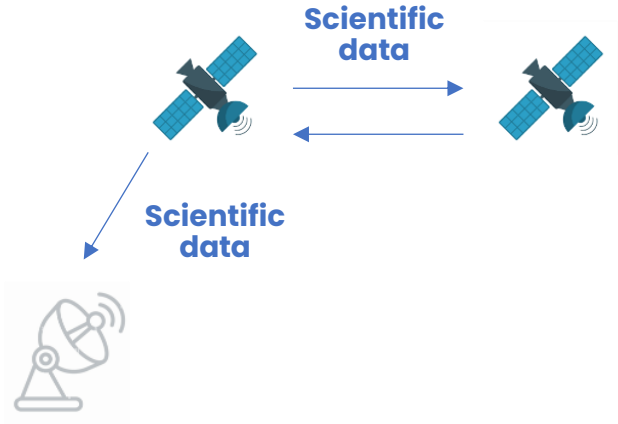
IngeniArs IP Cores Portfolio
Satellite Communications

High-Photon Efficiency (HPE) Transmitter

- Compliant with CCSDS 142.0-B standard – Deep Space
  - Photon Starved Links
- Satellite-to-Ground communication
  - **Payload Data Transmission**
- Highly Configurable:
  - Repeat Factor, Code Rate, PPM Order and Convolutional Interleaver Parameters
- **Symbol rate up to 8 Gbaud**
- Dedicated AXI interface for external DDR
- Characterized on AMD Xilinx Kintex Ultrascale KU060 space FPGA
- Validated on commercial Xilinx KU105 DevKit

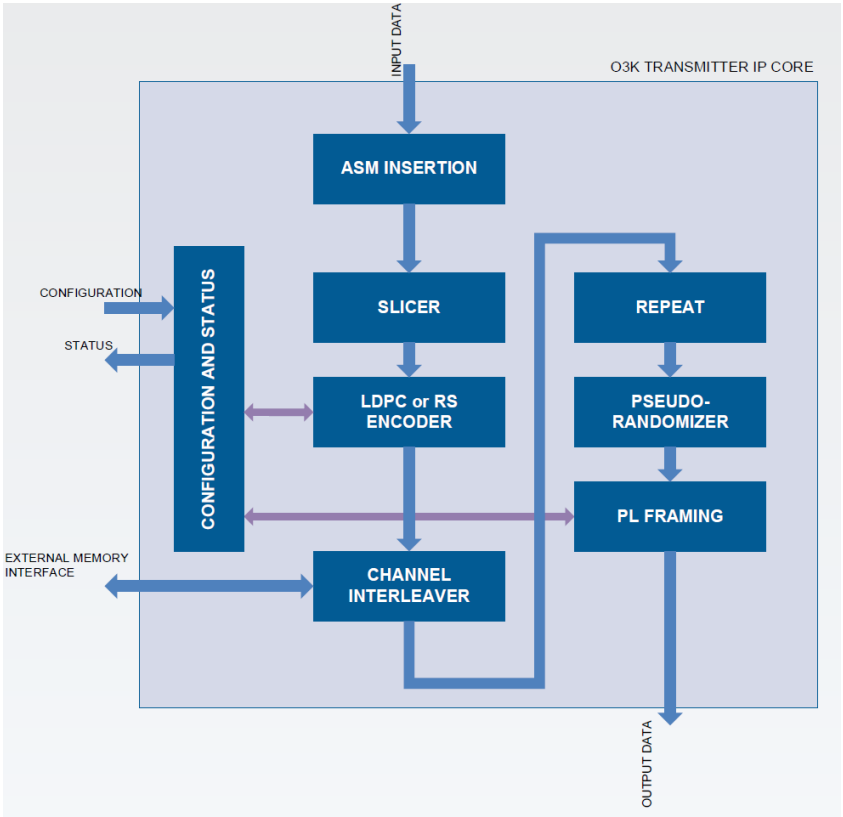


IngeniArs IP Cores Portfolio
Satellite Communications



Optical On-Off Keying (O3K) Transmitter

- Compliant with CCSDS 142.0-B standard – Earth Orbits
  - High-Photon Flux Regime
- Satellite-to-Ground communication and Inter-Satellite Links
  - **Payload Data Transmission**
- Highly Configurable:
  - Reed-Solomon or LDPC encoding
  - Repeat Factor, LDPC Code Rate, Channel Interleaver Parameters
- **Symbol rate up to 10 Gbaud**
- Dedicated AXI interface for external DDR
- Characterized on AMD Xilinx Kintex Ultrascale KU060 space FPGA
- Validated on commercial Xilinx KU105 DevKit



IngeniArs IP Cores Portfolio
Satellite Communications

High-Photon Efficiency (HPE) and Optical On-Off Keying (O3K) Receivers

- Under development – ESA Project

- Development Roadmap:
  - **Q3 2026: IP Core developed, tested and validated**
  - Characterization and Validation campaign on AMD Virtex Ultrascale+ or AMD Versal Premium

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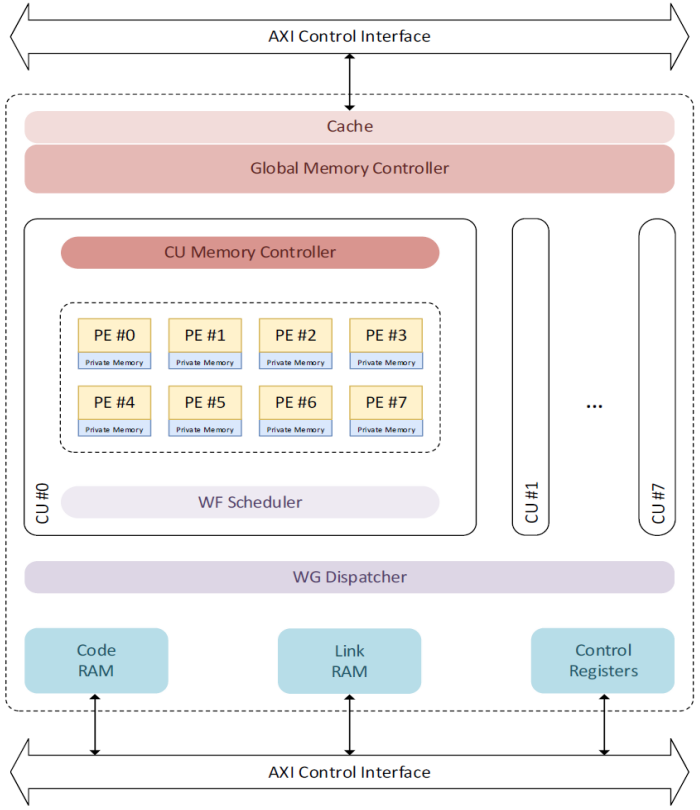
IngeniArs IP Cores Portfolio
Artificial Intelligence

GPU@SAT

- GPU Soft Core for FPGA/ASIC (**supporting also Class 1 High Reliability Missions**)
- **Support Artificial Intelligence, Computer Vision and High-Performance Computing algorithms for On-Board Data Processing and Handling**
- Compatible with Science and Telemetry data rate of current Earth Observation Missions
- **Configurable number of Computational Units**
- **Up to 16 GOPS**
- Implemented in several Rad-Hard FPGAs: AMD Kintex Ultrascale KU060, Microchip MPF500T, Microchip RTG4
- Support of real-time image processing up to an integration time of 2 ms
- Power consumption < 5W



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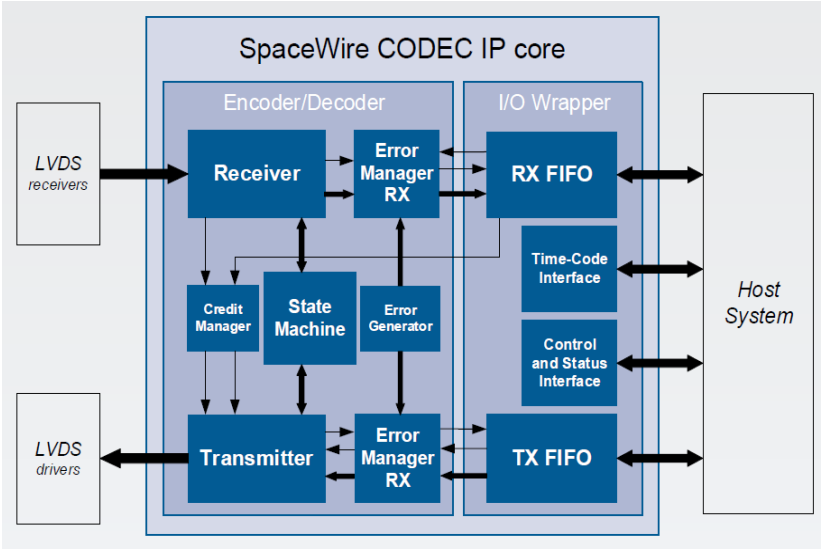
IngeniArs IP Cores Portfolio
High-Speed Interfaces

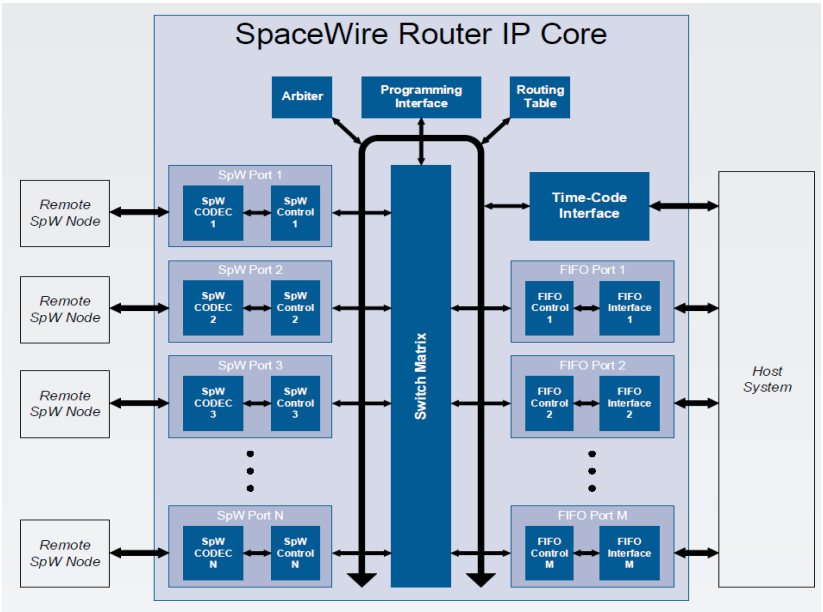
SpaceWire CODEC

- Support full-duplex communication, **up to 400Mbps**
- **TRL 9**
  - ESA Sentinel-3 mission, ESA Euclid mission, IRIDIUM NEXT constellation



SpaceWire ROUTER

- **Up to 31 SpW and/or host data (FIFO) ports**
- Support full-duplex communication



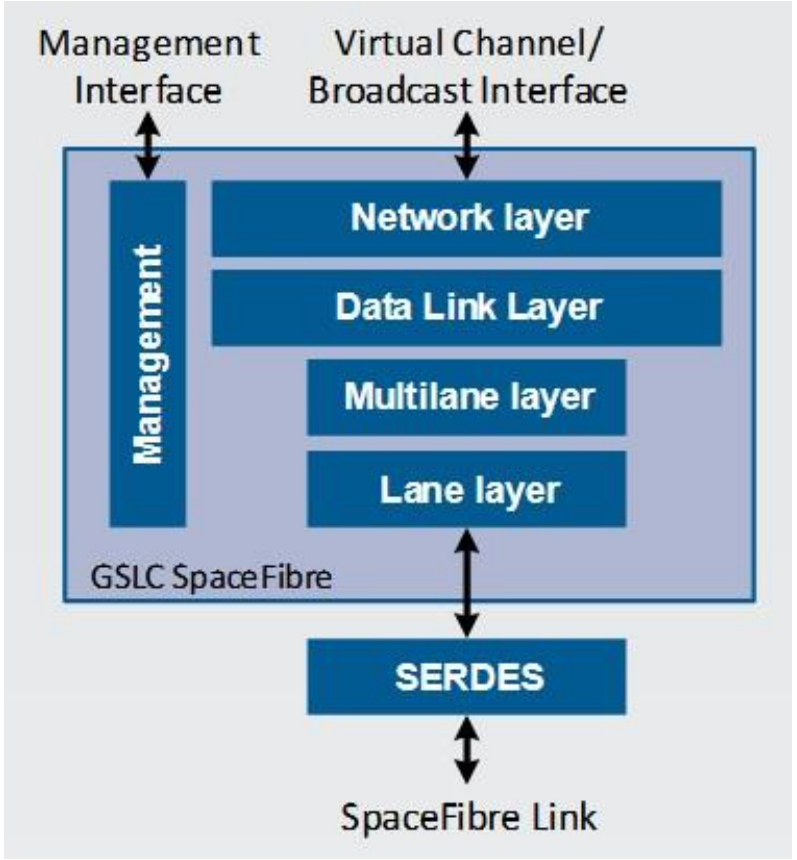
Common Features

- Compliant with ECSS-E-ST-50-12C standard, rev. 1
- Automatic Link Initialization and Link Flow Control
- Support Time-Code and Interrupts traffic
- Support path, logical and regional addressing
- Extendable with DMA and AMBA AXI
- Support RMAP commands

IngeniArs IP Cores Portfolio
High-Speed Interfaces

SpaceFiber CODEC

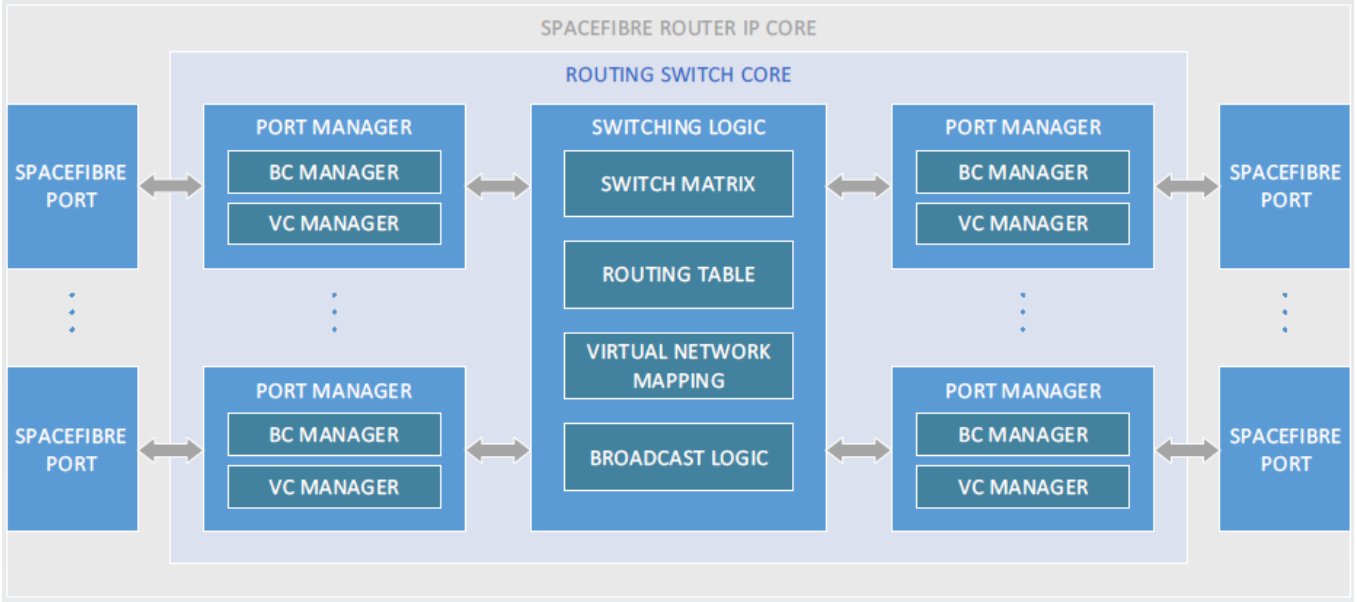
- Compliant with ECSS-E-ST-50-11C standard
- **Max TX rate supported (6.25Gbps/lane)**
- **Multi-Lane supported (Max 4 - up to 25Gbps)**
- Retro-compatible with SpW at Packet Level
- Configurable number of Virtual Channel
- Quality of Service (QoS)
  - Bandwidth reservation, priority, time scheduling
- Fault Detection, Isolation and Recovery (FIDR)
- Supported interface with the most relevant SERDES
  - Xilinx, Microchip, TLK2711…
- Simplified version available to save 40% HW resources
  - Without frame-retransmission and broadcast services



IngeniArs IP Cores Portfolio
High-Speed Interfaces

SpaceFiber Router

- Compliant with ECSS-E-ST-50-11C standard
- Configurable number of SpW, SpFi and Host Ports
  - Integration of SpW CODEC IP Cores
  - Integration of SpFi CODEC IP Cores
  - FIFO-based Host ports
- Virtual Network mapping logic
- Supported Multicast
- Supported Group Adaptive Routing
- Supported Virtual Channel Timeout



IngeniArs IP Cores Portfolio
High-Speed Interfaces

WizardLink TLK Equivalent

- WizardLink is a family of transceivers
  - Texas Instrument TLK2711 Chip is the reference
  - Implementing error detection with 8b/10b encoding-decoding
  - Integrated SERDES
  - Upper layers defined by the user
- SERDES are actually integrated into different Space-Qualified FPGAs
  - TI TLK2711 SERDES is no more useful

- IngeniArs TLK Equivalent IP Core:
  - Implements of 8b/10b coding
  - Connects with SERDES of FPGA
  - The control logic of TI TLK2711 can be maintained

→

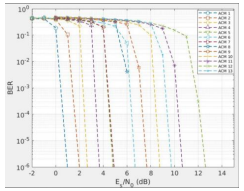
Replacement of TI TLK2711
when using FPGA with integrated SERDES
with consequent design simplification

IngeniArs IP Cores Portfolio
HW products related to presented IP Cores

Lyralink
YOUR RELIABLE RECEIVER

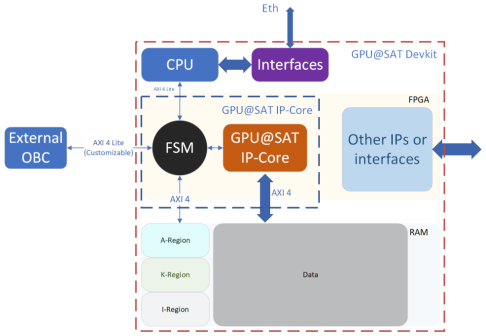
CCSDS 131.2-B Receiver

- **Complete EGSE solution implementing the receiver for end-to-end testing**



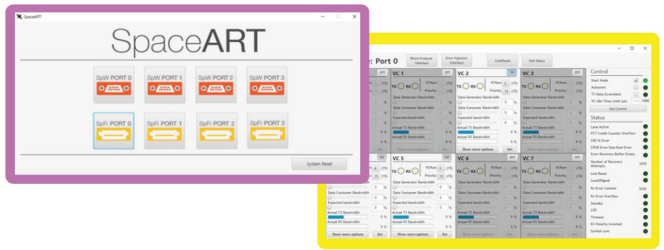
GPU@SAT DevKit

- **Complete Hardware Solution for On-Board AI-based Processing, implementing GPUSAT**



SpaceART Gen2 EGSE

- **Complete EGSE solution for testing of SpaceWire, SpaceFiber and WizardLink interfaces**



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Instagram

THANK YOU FOR YOUR ATTENTION

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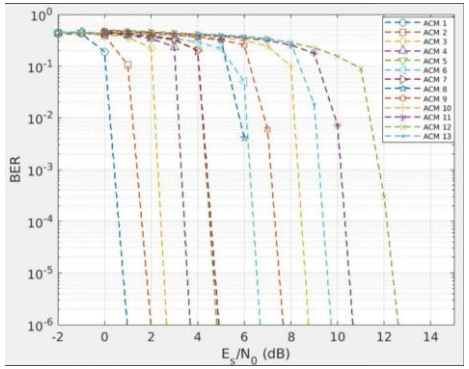
Satellite Communications

CCSDS 131.2-B Receiver – Lyralink
YOUR RELIABLE RECEIVER



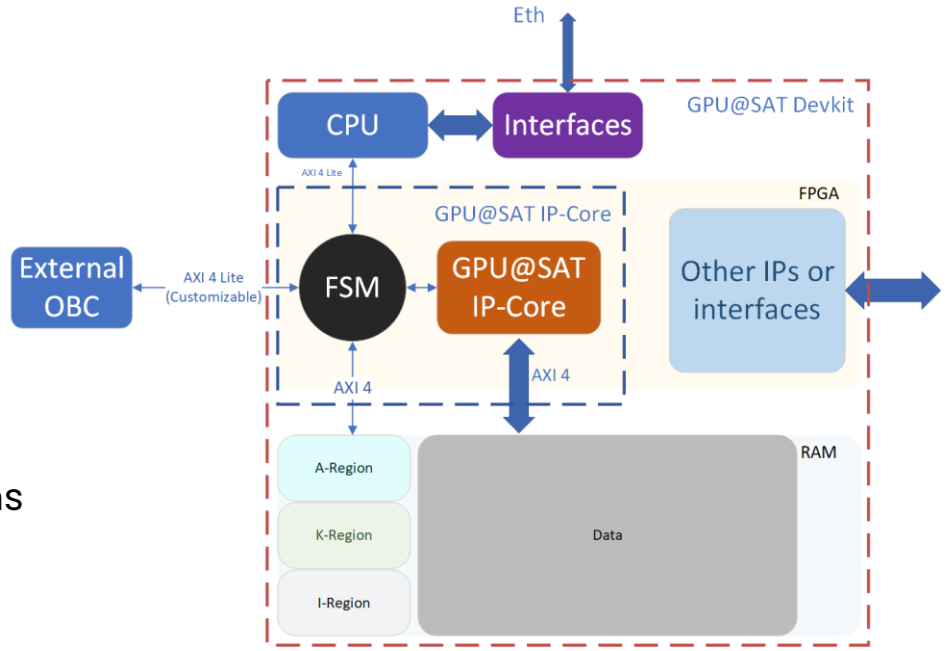
- **Complete EGSE solution**
  - **Transmitter + Channel Emulator option for end-to-end testing**
- **Configurable Symbol Rate up to 500Mbaud**
- Input IF range [530:2700] MHz
- Input power manager [-50:-10] dBm
- 50-ohm input SMA female connector
- Low Implementation Loss
- **Integrated Bit Error Rate Meter (BERT)**
- Remote Control via GUI
- High Storage Capacity for data analysis

IngeniArs IP Cores Portfolio
Artificial Intelligence

GPU@SAT – DevKit

- Complete Hardware Solution for On-Board AI-based Processing
- Reduced effort of programmers for implementation of AI and CV algorithms

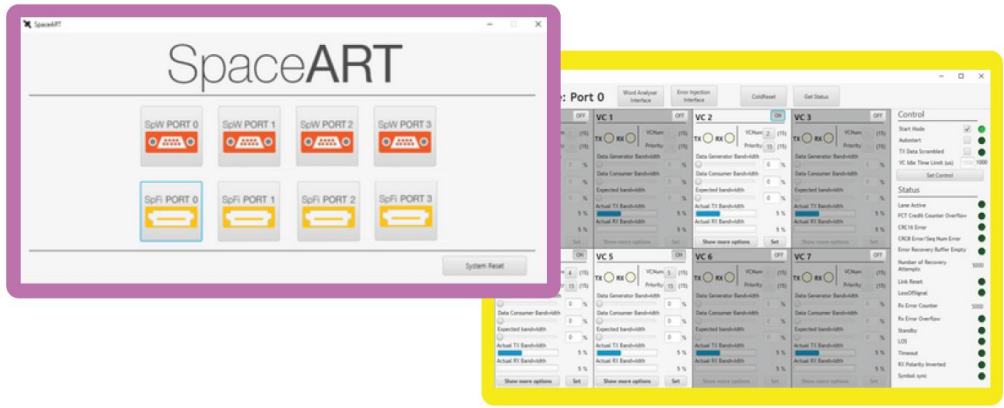
- Available with:
  - 4 CUs @ 250MHz (next steps: 8 Cus)
  - **Up to 8 GOPS**
  - With CPU, hosting the Python server application



IngeniArs IP Cores Portfolio
High-Speed Interfaces

SpaceART Gen2 EGSE

- New generation of testing equipment for high-speed data interfaces
  - **Support SpaceWire, SpaceFiber and WizardLink protocols**
- Real-time packet generation, processing and consumption
- Analysis of different levels: packet, frame, character
- Eye-Diagram measurement on HSSL
- Advanced Error Injection / word replacement capability
- Easy-to-use GUI



Interfaces:

- Up to 12 SpaceWire ports
- Up to 4 SpaceFiber or WizardLink (HSSL)
- Up to 4 custom functionality discrete I/Os, on SMA connectors
- Host Interface: PCI Express, CompactPCI Express, or Ethernet

IngeniArs IP Cores Portfolio
FPGA Implementation

CCSDS 131.2-B Transmitter

FPGA Device	Frequency	Symbol-Rate	LUT	Flip-Flops	BRAM	DSP
AMD KU060	320MHz	320Mbaud	13k (3.82%)	16k (2.40%)	137 (12.7%)	104 (3.77%)
	320MHz	640Mbaud	22k (6.50%)	26k (3.9%)	138 (12.8%)	210 (7.54%)
	305MHz	1220Mbaud	41k (12.34%)	51k (7.7%)	180 (16.6%)	420 (15.07%)
	290MHz	1740Mbaud	63k (18.8%)	77k (11.5%)	208 (19%)	624 (22.6%)

All ModCods

Internal LUTs

SEE Off

Filter Enabled (OSR = 4, SPAN = 12)

IngeniArs IP Cores Portfolio
FPGA Implementation

CCSDS 131.2-B Receiver – Downlink Version

FPGA Device	CLB FF	CLB LUT	BRAM	URAM	DSP	Max Baud Rate
AMD Virtex UltraScale+	366777 (10,61%)	731451 (42.33%)	1123,5 (41,8%)	678 (52,97%)	1652 (13.44%)	500Mbaud

FPGA Device	FF	ALM	RAM	DSP	Max Baud Rate
Altera Stratix 10	325104 (8.71%)	303440 (32,52%)	4085 (34,85%)	1242 (21,56%)	388Mbaud
Altera Agilex 7	348570 (6,67%)	297771 (22,81%)	4085 (21,55%)	1242 (10.10%)	415Mbaud

CCSDS 131.2-B Receiver – Uplink Version

FPGA Device	CLB FF	4-LUT	LSRAM	URAM	DSP	Max Baud Rate
Microchip PolarFire RT	265478 (55,16%)	362961 (75,42%)	986 (64,87%)	463 (10,43%)	1272 (85,95%)	127,35Mbaud

FPGA Device	CLB FF	CLB LUT	BRAM	DSP	Max Baud Rate
AMD Kintex Ultrascale	145047 (21.87%)	146203 (44.08%)	608 (56.3%)	1213 (43.95%)	200Mbaud

IngeniArs IP Cores Portfolio
FPGA Implementation

HPE (CCSDS 142-0.B) Transmitter

FPGA Device	LUT	*LUTRAM*	Flip-Flops	BRAM
AMD KU060	38,5% (127779 / 331680)	0,82% (1208 / 146880)	6,34% (42048 / 663360)	6,71% (72/1080)
AMD KU040	54,07% (131063 / 331680)	1,07% (1208 / 146880)	8,68 (42070 / 663360)	12,08% (72,5 / 1080)

N = 32
B = 1024
PPM Order = 4
Code Rate = 1/2

O3K-LDPC (CCSDS 142-0.B) Transmitter

FPGA Device	LUT	*LUTRAM*	Flip-Flops	BRAM	*DSP*
AMD KU060	39,34% (130495 / 331680)	0,63% (930 / 146880)	11,37% (75420/ 663360)	17,5% (189 / 1080)	0,18% (5 / 2760)
AMD KU040	51,98% (126008 / 331680)	0,82% (930 / 146880)	15,55% (75370 / 663360)	31,5% (189 / 1080)	0,18% (5 / 2760)

N = 64
K = 120
Interleaving = 8
Repeat = 1
N_SUB = 1

O3K-RS (CCSDS 142-0.B) Transmitter

FPGA Device	LUT	*LUTRAM*	Flip-Flops	BRAM	*DSP*
AMD KU060	22% (73025 / 331680)	0,50% (728 / 146880)	10,17% (67485 / 663360)	26,16% (282,5/ 1080)	0,14% (4/ 2760)
AMD KU040	29,64% (71839 / 242400)	0,65% (728 / 112800)	13,92% (67471 / 484800)	47,08% (282/ 600)	0,21% (4/ 1920)

IngeniArs IP Cores Portfolio
FPGA Implementation

GPU@SAT – AMD Xilinx

N_CU	Frequency [MHz]	Power [W]		LUT	Flip-Flops	LUTRAM	BRAM	URAM	DSP	
		Static	Dynamic							
4	52,63	0,653	1,806	131171	216262	8010	170,5	-	256	AMD KU060
				39,55%	32,60%	5,45%	15,79%	-	9,28%	
4	80	0,653	2,632	131171	216262	8010	170,5	-	256	
				39,55%	32,60%	5,45%	15,79%	-	9,28%	
4	105,26	0,653	3,498	131071	216262	8010	170,5	-	256	
				39,52%	32,60%	5,45%	15,79%	-	9,28%	
4	128,21	0,653	4,291	131158	216262	8010	170,5	-	256	
				39,54%	32,60%	5,45%	15,79%	-	9,28%	
4	142,86	0,653	4,718	131039	216262	8010	170,5	-	256	
				39,51%	32,60%	5,45%	15,79%	-	9,28%	
4	142,86	0,653	2,64	71200	114525	2582	170,5	-	128	
				21,47%	17,26%	1,76%	15,79%	-	4,64%	
4	161,29	0,653	2,995	71164	114525	2582	170,5	-	128	
				21,46%	17,26%	1,76%	15,79%	-	4,64%	
4	178,57	0,653	3,303	71325	114589	2582	170,5	-	128	
				21,50%	17,27%	1,76%	15,79%	-	4,64%	
4	188,68	0,653	3,581	71333	114609	2582	170,5	-	128	
				21,51%	17,28%	1,76%	15,79%	-	4,64%	
4	200	0,653	3,778	71343	114596	2582	170,5	0	128	
				21,51%	17,28%	1,76%	15,79%	-	4,64%	
										AMD ZCU104
8	-	-	-	123563,52	199710,72	10389,696	306,5088	0,9984	255,9168	
				53,63%	43,34%	10,21%	98,24%	1,04%	14,81%	
2	204,08	0,296	1,398	46547	67225	2360	121,5	1	80	AMD KRIA K26I
				39,74%	28,70%	4,10%	84,38%	1,56%	6,41%	

IngeniArs IP Cores Portfolio
FPGA Implementation

GPU@SAT – Microchip

N_CU	Frequency [MHz]	Power [W]		LUT	Flip-Flops	uSRAM (0.7 Kb)	LSRAM (20 Kb)	uPROM Kb	DSP	
		Static	Dynamic							
4	52,91	-	-	294647	376809	523	244	0	128	Microchip PolarFire MPF500T
				61,26%	78,34%	11,78%	16,05%	0,00%	8,65%	
2	57,14	-	-	167169	199001	377	206	0	64	Microchip PolarFire MPF200T
				87,07%	103,65%	21,37%	33,44%	0,00%	10,88%	
1	57,14	-	-	95531	105364	178	123	0	32	
				49,76%	54,88%	10,09%	19,97%	0,00%	5,44%	
N_CU	Frequency [MHz]	Power [W]		LUT	Flip-Flops	uSRAM (1.5 Kb)	LSRAM (24.5 Kb)	uPROM Kb	DSP	
		Static	Dynamic							
4	68,97	-	-	293271	390386	136	309	0	128	Microchip RT4G150
				193,17%	257,13%	64,76%	147,85%	0,00%	27,71%	
2	68,97	-	-	164415	201849	101	167	0	64	
				108,29%	132,95%	48,10%	79,90%	0,00%	13,85%	
1	68,97	-	-	96611	107560	84	96	0	32	
				63,63%	70,85%	40,00%	45,93%	0,00%	6,93%	

IngeniArs IP Cores Portfolio
FPGA Implementation

SpW CODEC

FPGA Device	Combinational	Registers	RAM Blocks
Michrochip RTAX2000S	2,97% (639/21504)	3.53% (380/10752)	3.125% (2/64)
Michrochip PolarFire RTPF500T	0.14% (672/481272)	0.09% (444/481272)	uSRAM: 0.07% (3/4440) LSRAM: 0% (0/1520)
Michrochip RTG4G150	0.58% (883/151824)	0.32% (490/151824)	uSRAM: 1.43% (3/210) LSRAM: 0% (0/209)

SpW ROUTER

FPGA Device	Combinational	Registers	RAM Blocks
Michrochip RTAX2000S (4 SpW ports + 1 host port)	30.576% (6575/21504)	40.718% (4378/10752)	15.625% (10/64)
Michrochip RTAX2000S (8 SpW ports + 1 host port)	52.097% (11203/21504)	64.402% (6817/10752)	28.125% (18/64)
Michrochip RTG4G150 (9 SpW ports + 1 host port)	11.94% (18126/151824)	5.92% (8983/151824)	uSRAM: 13.333% (13/210) LSRAM: 0% (0/209)

IngeniArs IP Cores Portfolio
FPGA Implementation

SpFi CODEC

FPGA Device	VC	Combinational	Registers	RAM Blocks
Michrochip RTAX2000S	1	28.61% (6152/21504)	16.18% (2815/10752)	18.75%
	2	35.37% (7605/21504)	33.42% (3592/10752)	25.00%
	4	45.81% (9852/21504)	44.72% (4808/10752)	37.50%
Michrochip RTG4G150	1	3.11% (4689/151824)	1.50% (2291/151824)	2.52%
	2	3.76% (5713/151824)	1.90% (2888/151824)	2.85%
	4	4.65% (7073/151824)	2.52% (3835/151824)	3.53%
	8	6.62% (100065/151824)	3.76% (5273/151824)	4.88%
Xilinx Virtex 5	1	3.56% (2919/81920)	2.08% (1702/81920)	2.35%
	2	4.46% (3657/81920)	2.68% (2199/81920)	4.03%
	4	6.15% (5037/81920)	3,67% (3003/81920)	5.73%
Xilinx Zynq-7000	1	1.07% (2346/218600)	0.38% (1665/437200)	1.10%
	2	1.29% (2824/81920)	0.51% (2245/437200)	1.10%
	4	1.88% (4110/81920)	0.73% (3203/437200)	2.20%

IngeniArs IP Cores Portfolio
FPGA Implementation

SpFi ROUTER

FPGA Device	Setup	Combinational	Registers	RAM Blocks
Michrochip RTG4G150	4 ports, 4 VCs	12.8%	4.9%	6.7%
	4 ports, 8 VCs	37.8%	10.9%	26.1%
	8 ports, 4 VCs	39.2%	11.1%	16.6%
	8 ports, 8 VCs	132.5%	26.6%	28.5%
	4 ports, 4 VCs, No multicast	11.7%	4.3%	5.7%
	8 ports, 8 VCs, No multicast	120.4%	24.0%	26.1%
Xilinx Virtex 6	4 ports, 4 VCs	9.8%	2.1%	0.5%
	4 ports, 8 VCs	24.3%	5.3%	0.5%
	8 ports, 4 VCs	26.1%	6.2%	1.0%
	8 ports, 8 VCs	78.8%	14.9%	1.0%
Xilinx Zynq-7000	4 ports, 4 VCs	5.9%	1.7%	0.18%
	4 ports, 8 VCs	16.4%	3.8%	0.18%
	8 ports, 4 VCs	15.9%	3.9%	0.36%
	8 ports, 8 VCs	50.3%	9.4%	0.36%