AGGA-4 IP Core for Modern FPGAs

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Overview

- Differences between AT7991 and the AGGA-4 IP core
- AGGA-4 IP configuration
  - Generics
  - Configuration GUI
- Implementation in XCKU040 and MPF300
  - Resources
  - Timing
  - Characterisation of the configuration options
- Validation
  - RTL simulation
  - Tests in hardware
- Digital Front-End
- Conclusions

This work has been performed under an ESA contract 4000138911/22/NL/SD.

AGGA-4 ASIC vs IP-Core

FROM

AGGA-4 ASIC (AT7991)

ATC18RHA

GNSS clock ≤ 50MHz/125MHz

LEON clock ≤ 87 MHz

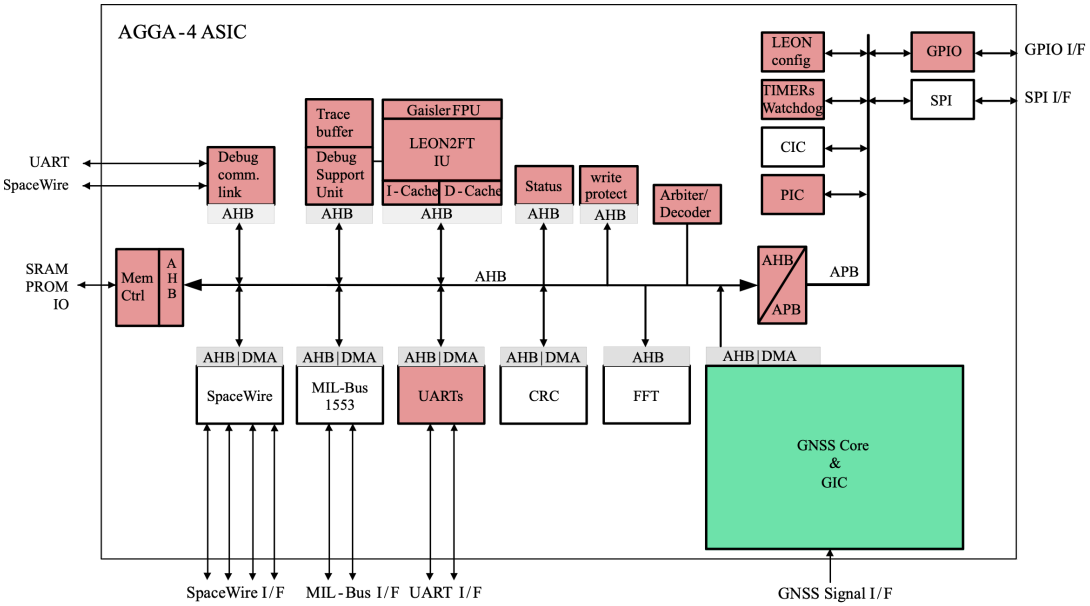
TO

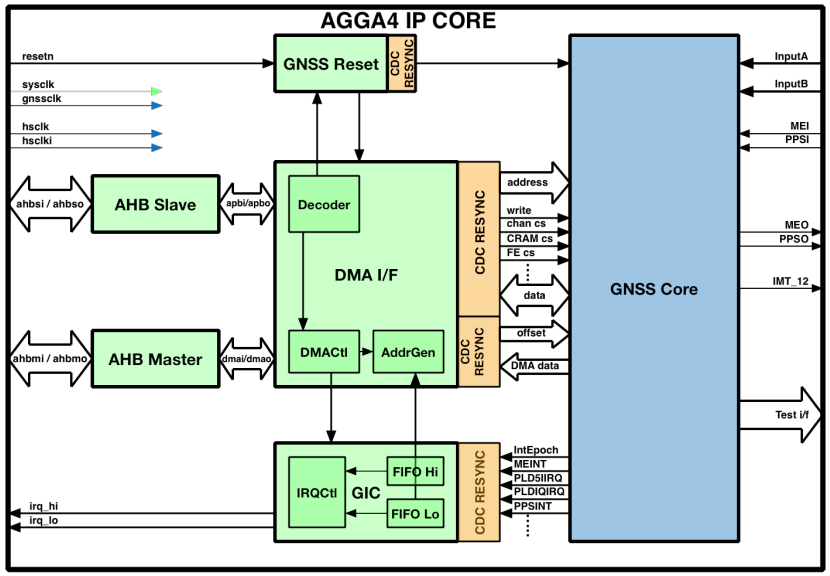
AGGA-4 IP Core

FPGA: AMD, Microchip, NanoXplore, …

GNSS clock ~ 60MHz/150MHz

LEON clock ~ 100 MHz





Legend:
GIC: GNSS Interrupt Controller
CIC: Communication Interrupt Controller
PIC: Primary Interrupt Controller

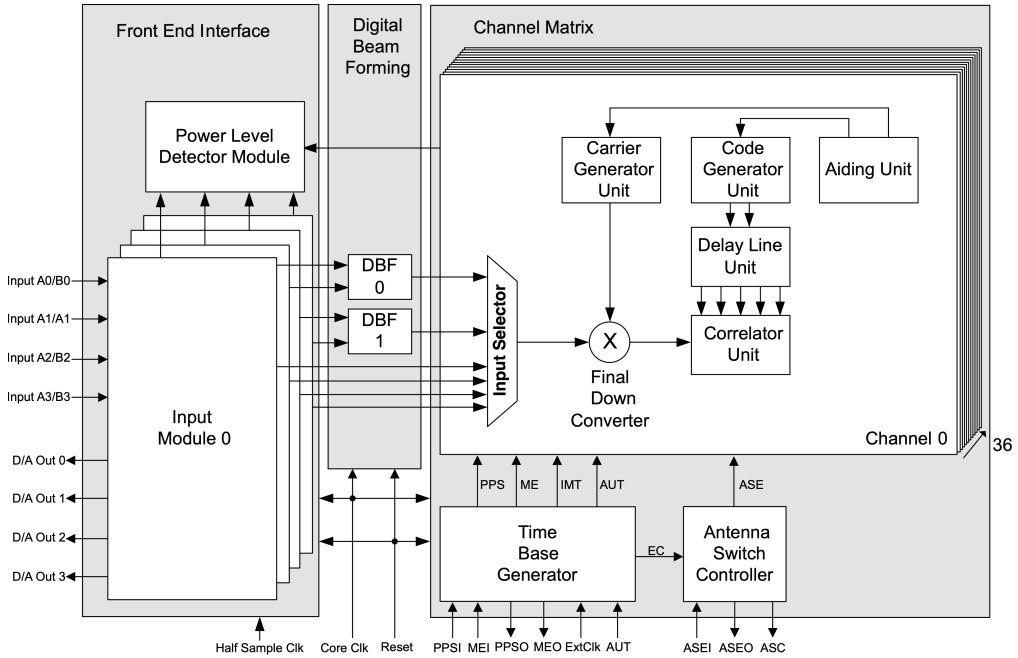
AGGA-4 ASIC vs IP-Core

Many parameters of the AGGA-4 IP core are configurable at synthesis time.
The table states max values.

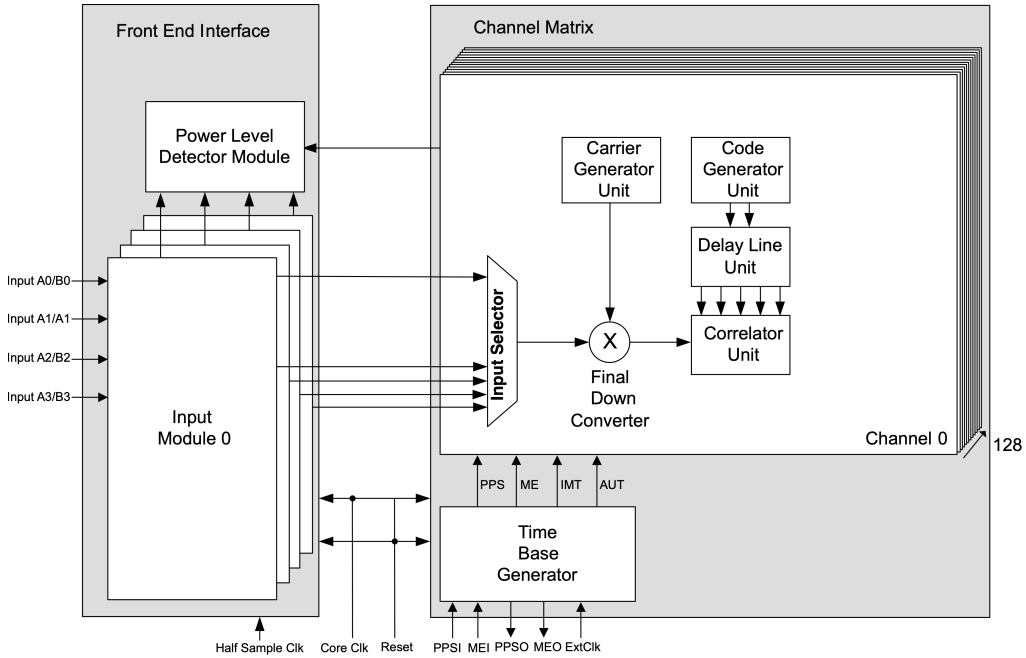
Feature	AGGA-4 IP	AGGA-4 ASIC
Front-End I/F	4 input modules: IFC, 4xDDC. Common PLD. 3-bit samples.	4 input modules: IFC, R2C, 2xDDC. Common PLD, DBF. 3-bit samples.
Channels	128 tracking channels	36 tracking channels
Code Generation	2x pri mem (≤10240c), 2x pri VFCG (≤32b), 2x sec mem (≤1800c)	2x pri mem (≤5120c), 1x pri VFCG (≤28b), 2x sec mem (≤100c)
Correlators per Channel	5 complex (I/Q)	5 complex (I/Q)
Channel Slaving	SW slaving	HW and SW slaving
Observables	21 observables	21 observables
Microprocessor	External, 2x AHB I/F	LEON2-FT on-chip
Additional modules	AGGA DSU, SigGen, AGGA GPIO	CRC, FFT, SPI, GPIO
DMA performance	23 observables transferred in 24 bus cycles	23 observables transferred in 188 bus cycles

Differences in the GNSS Core

AGGA-4 ASIC

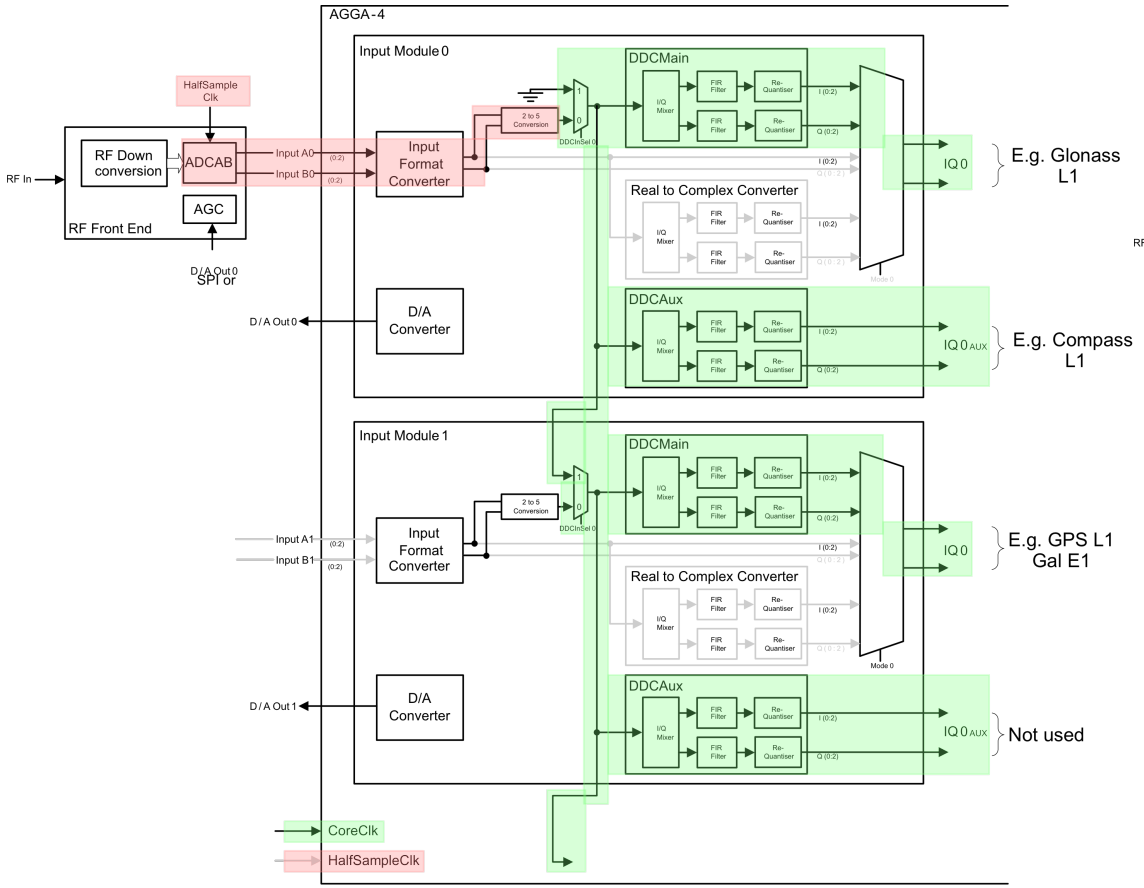


AGGA-4 IP Core

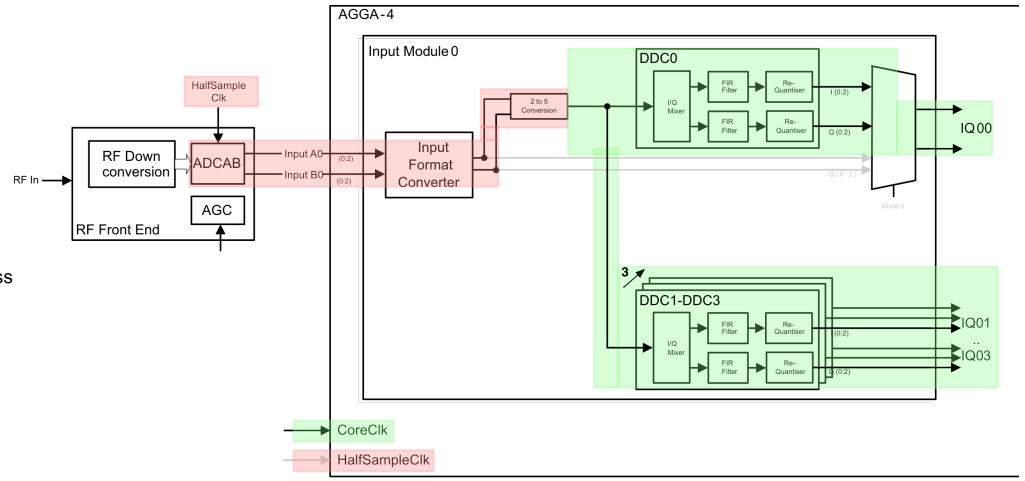


Differences in the Input Modules

AGGA-4 ASIC

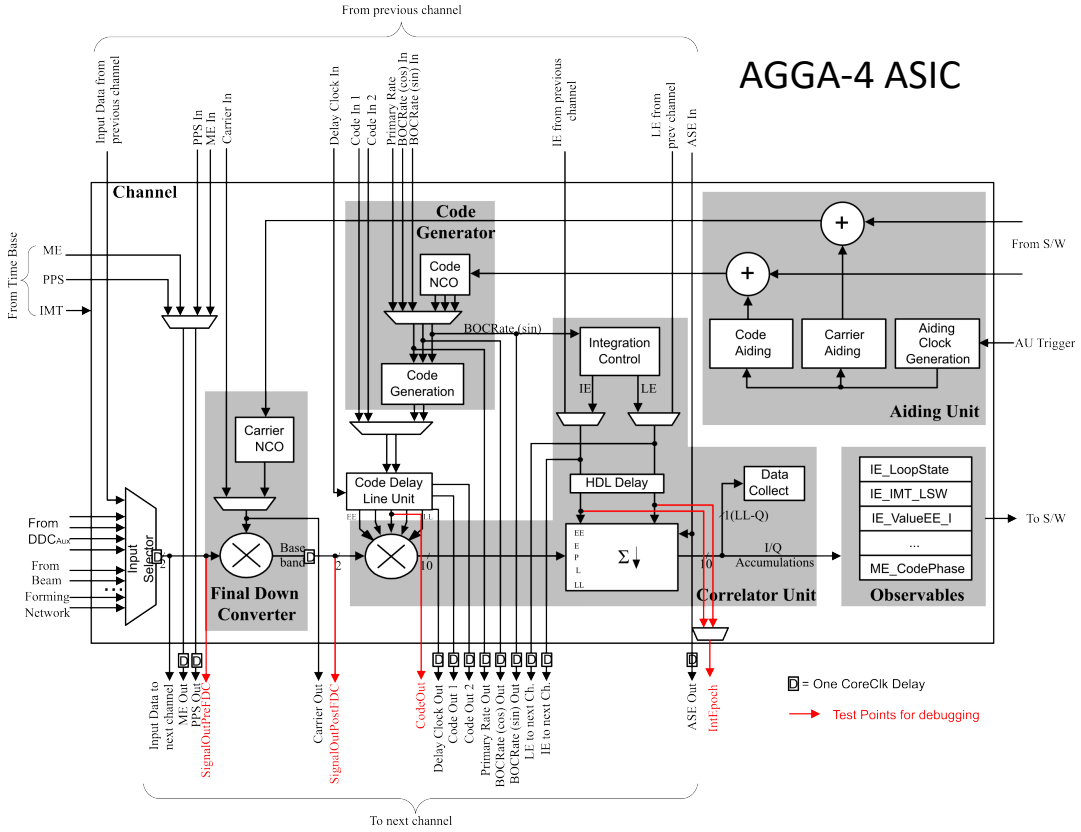


AGGA-4 IP Core

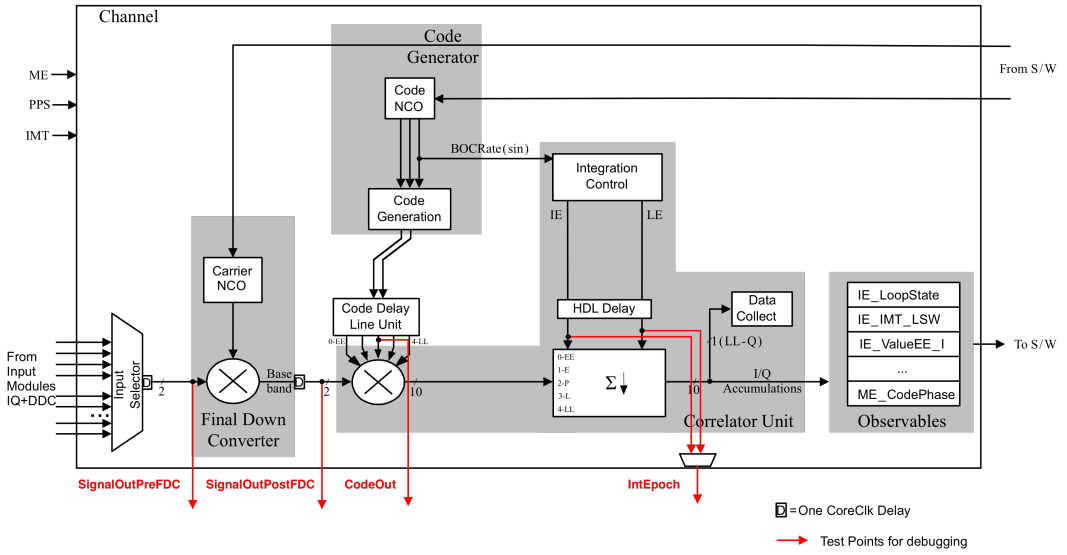


Differences in the Tracking Channels

AGGA-4 ASIC

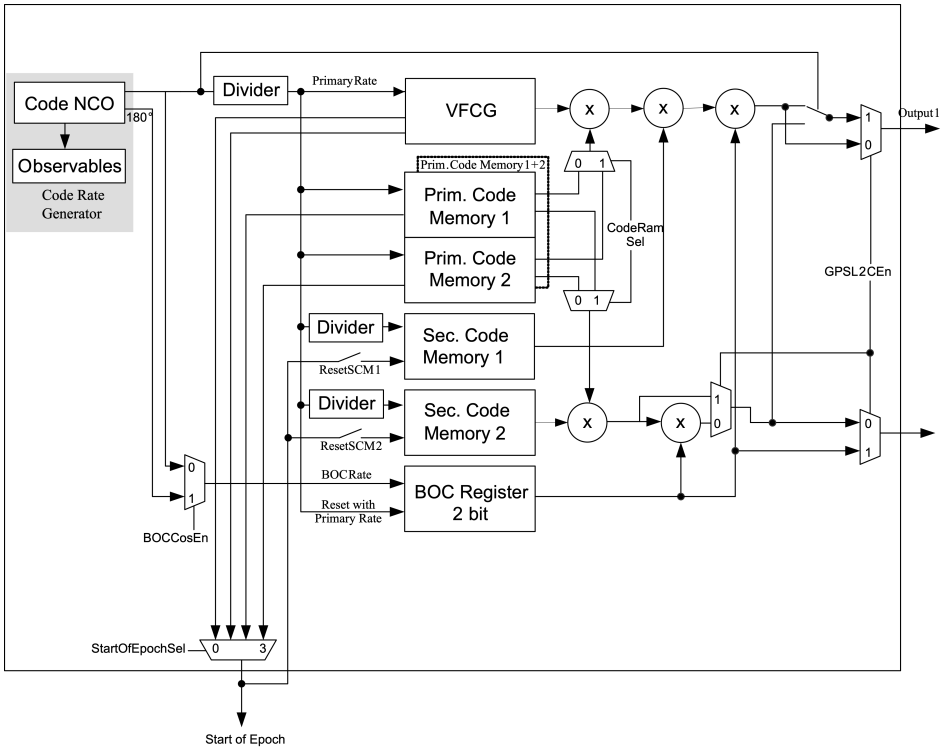


AGGA-4 IP Core

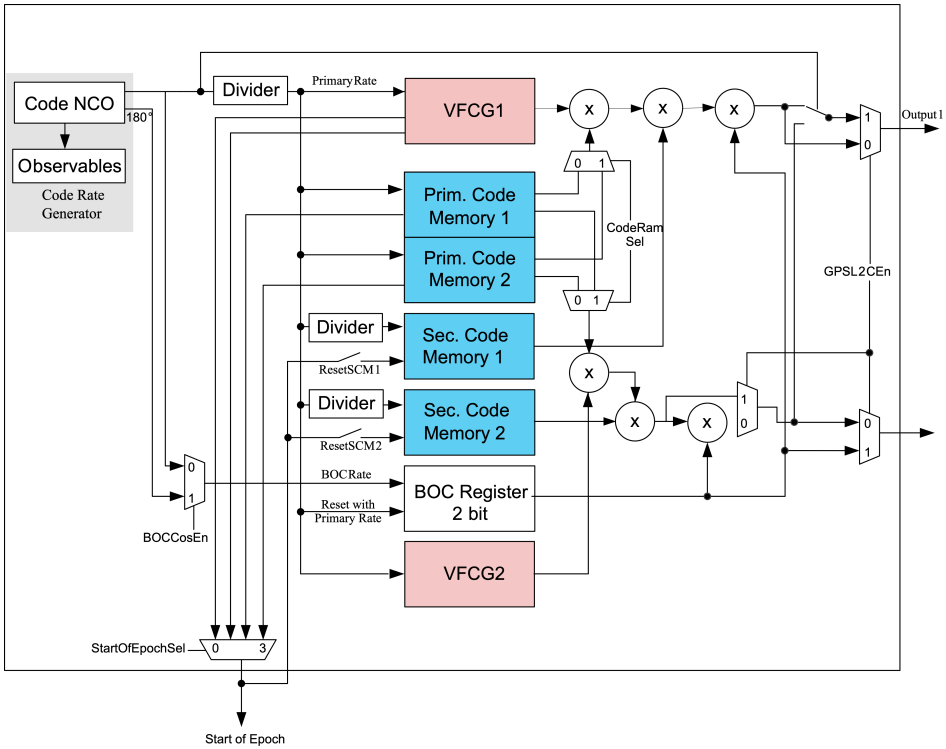


Differences in Code Generators

AGGA-4 ASIC



AGGA-4 IP Core



GNSS Core Synthesis-Time Parameters (Generics)

Configured before synthesis:

- N_IM - number of input modules (from 1 to 4)
- N_DDC - number of DDCs per input module (from 0 to 4)
- IFC Format: 0:sgn/magnitude, 1: unsigned, 2: 2's complement
- DDC Phase Increment
- N_CHGRP - number of tracking channel groups (from 1 to 128)
- N_CHINGRPi - number of tracking channels in each group (from 1 to 128)
- N_CORR - number of correlation pairs (from 1 to 5)
- DLY_STGi - max number of delay stages (from 1 to 32)
- CORR_BITS - width of correlation accumulators (from 1 to 32)
- N_PMEM - number of primary code RAMs (0,1,2)
- SEC_LENi - size of secondary code RAMs (0=not configured, 100b=DFFs, or 1800b=BRAM)
- N_VFCG - number of VFCGs for primary code (0,1,2)
- N_LFSR - number of LFSRs in VFCG (1,2)
- LFSR_BIT - LFSR width, common to both LFSRs (from 1 to 16)
- CODE_LENi - LFSR code length, separate for each LFSR
- CODE_POLi - LFSR polynomial
- CODE_INIi - LFSR initial value

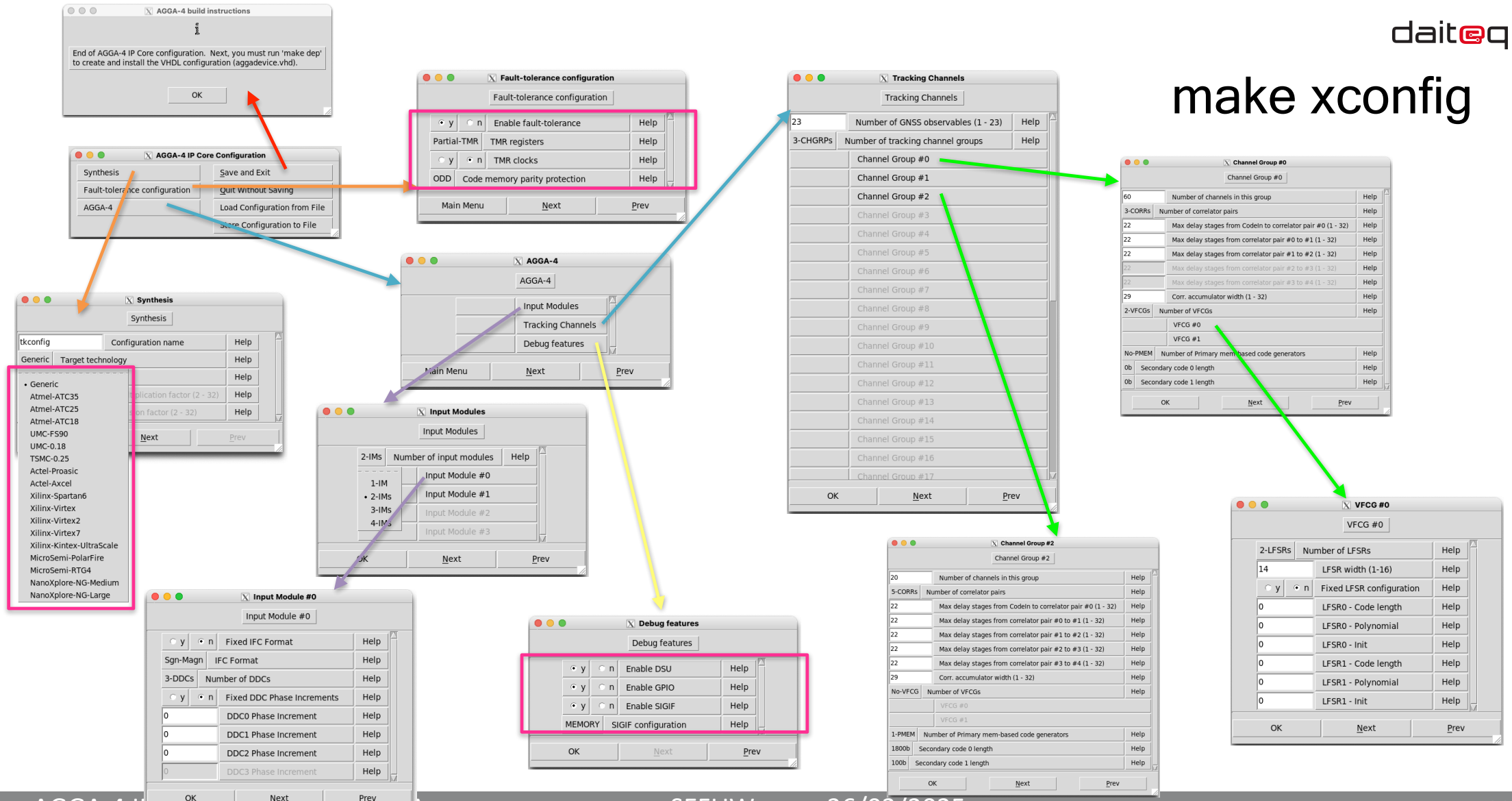
… can be made hard-wired.

AGGA-4 Configuration

- Organization of AGGA-4 IP configuration files:
  - aggatarget.vhd, aggadevice.vhd, aggaconfig.vhd – techmap-specific types, configurations and functions (like in LEON2-FT)
  - gnsspkg.vhd – types and constants for GNSS computations

- New menu-driven configuration tool for the AGGA-4 IP core (like in LEON2-FT)
  - make xconfig – configuration GUI
  - make dep – invokes mkaggadevice and creates aggadevice.vhd

make xconfig



AGGA-4 ASIC vs IP Core

GNSS core resources in XCKU040
Channels compatible with AGGA-4 ASIC
N_IM=4, N_CH=20

Module	original	non-diversified	diversified
i_gnss_core	63451	66003	56485
.CM	59439	61977	53021
..ASC_i0	26	26	.
..ChannelMatrixControl_i0	200	199	170
..TimeBase_i0	673	772	639
..ChannelGroup[0].Channel_i0	2927	3048	2640
.DBF0	90	93	.
.DBF1_GEN.DBF1	90	93	.
.FE	3832	3840	3464
..InputModule_i0	599	601	524
..PLDModule_i0	1436	1436	1368
...PLD5I	287	287	287
...PLDIQ	496	497	443

AGGA-4 IP core resources in XCKU040
Customised channels
N_IM=2, N_CH=36

Input Modules	N_DDC	
.	0 (R3a)	3 (R3b)
AGGA4 default (R4a)	109966	111112
Min L1 C/A (R4b)	86627	87776
Memory-only (R4c)	98589	99733
LFSR-only (Sec 1800b) (R4d)	100976	102120
LFSR-only (Sec 100b) (R4e)	107627	108916

Timing — Xilinx Kintex UltraScale

Configuration	Freq(MHz)	WNS(ns)	TNS(ns)	WHS(ns)	THS(ns)
Original AGGA-4	60/150	1.399	0.000	0.030	0.000
Pre-diversified AGGA-4	60/150	1.161	0.000	0.029	0.000
Diversified AGGA-4	60/150	2.228	0.000	0.030	0.000

Timing — Microchip PolarFire

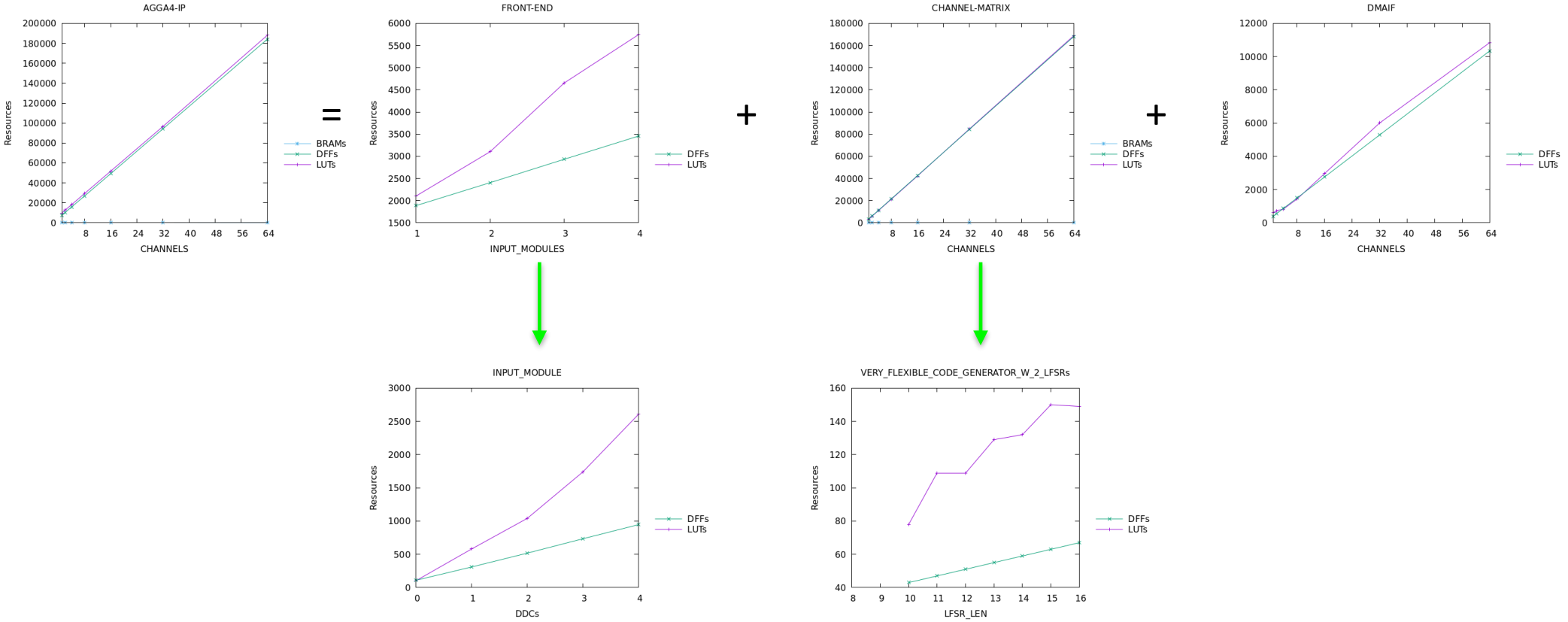
Clock Domain	clk_50mhz	gnssclk	gnssclki	hsclk	hsclki
Original AGGA-4					
Required Period (ns)	20.000	16.666	.	6.666	6.667
Required Frequency (MHz)	50.000	60.002	.	150.015	149.993
Worst Slack - Max (ns)	18.845	6.389	.	2.374	.
Worst Slack - Min (ns)	0.082	0.035	.	0.078	.
Non-diversified AGGA-4 (Phase 1)					
Required Period (ns)	20.000	16.666	16.667	6.666	6.667
Required Frequency (MHz)	50.000	60.002	59.999	150.015	149.993
Worst Slack - Max (ns)	18.922	6.563	3.178	2.447	.
Worst Slack - Min (ns)	0.078	0.021	8.158	0.078	.
Diversified AGGA-4 (Phase 2)					
Required Period (ns)	20.000	16.666	.	6.666	6.667
Required Frequency (MHz)	50.000	60.002	.	150.015	149.993
Worst Slack - Max (ns)	19.353	6.737	.	2.290	.

Resource Requirements – XCKU040

AGGA-4 IP Core:
N_IM=2, N_DDC=2

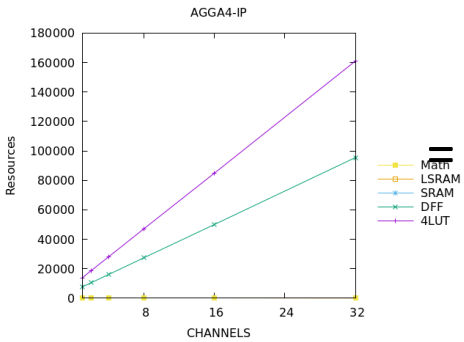
N_DDC=2

Channel cfg matches AT7991



Resource Requirements – MPF300

AGGA-4 IP Core:
N_IM=2, N_DDC=2



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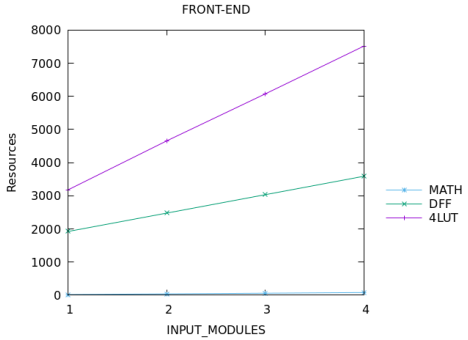
N_DDC=2



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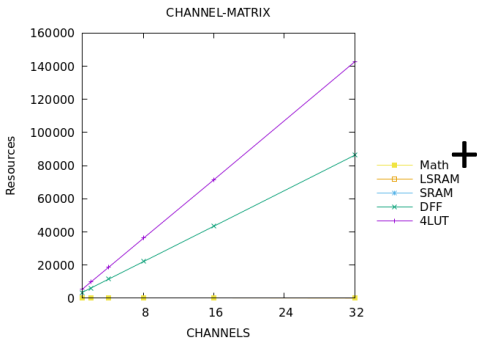
Channel cfg matches AT7991



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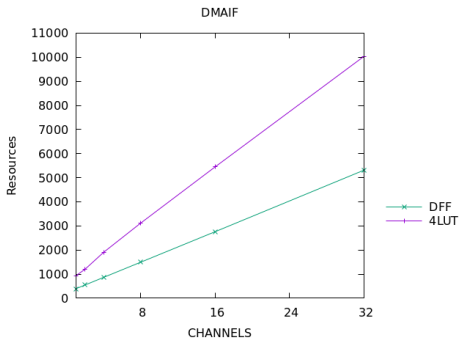
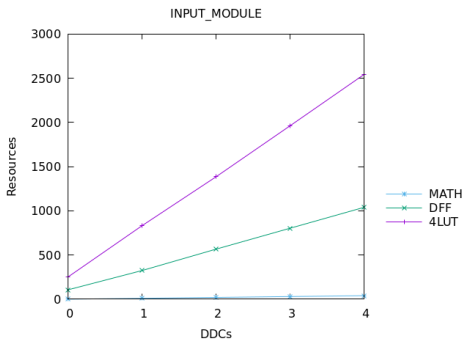
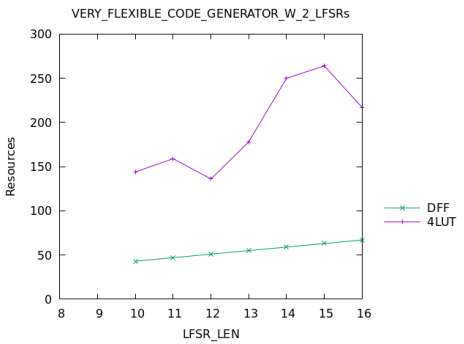






AGGA-4 IP Core Validation

VHDL simulation

- Existing VHDL test cases part of the AT7991 design database
- Derived test cases to match new features (CodeGen, DDCs, …)
- New test cases to test DMA I/F and GNSS IRQ CTRL
- Code coverage for almost all files (all but 7) reached 100% with a very small number of coverage exceptions.

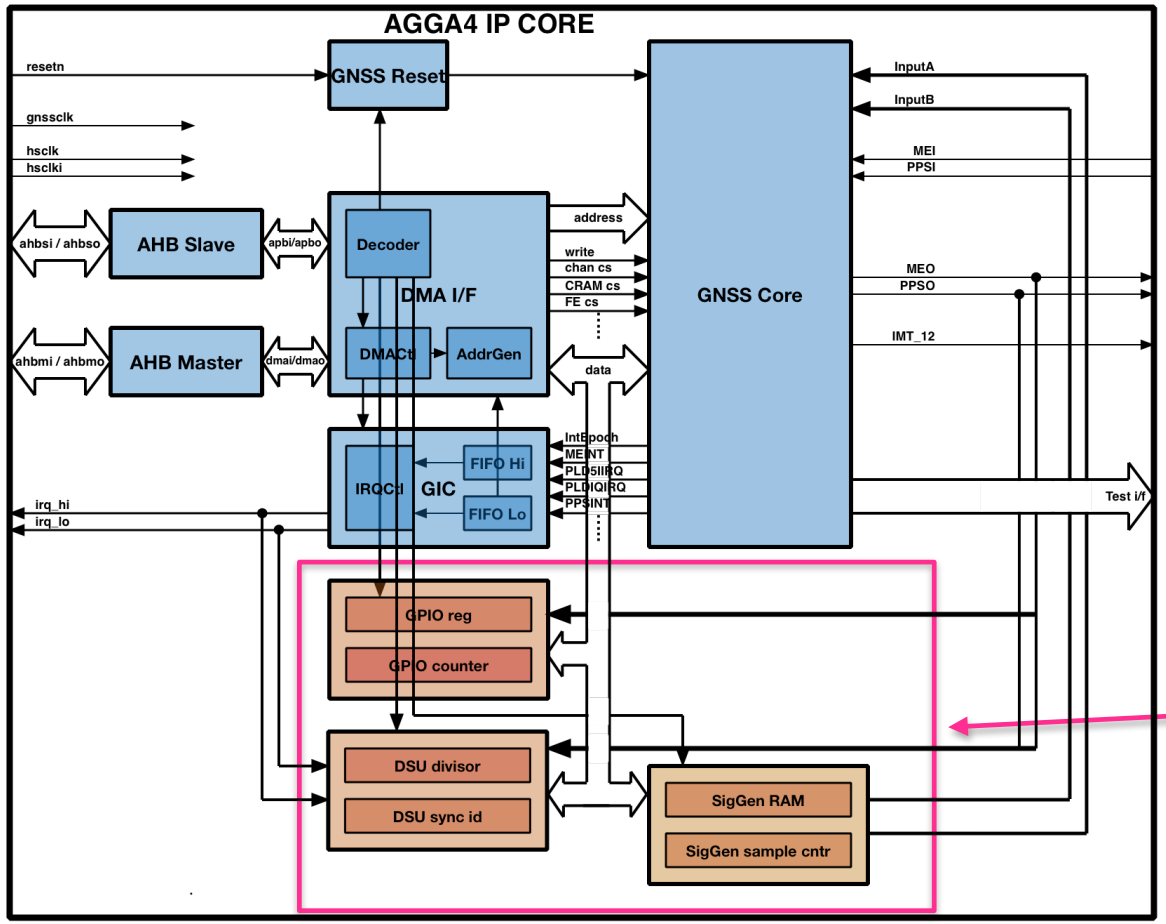
File	Line	Type	Comment
CFGInfo.vhd	276	s	when others
syncfsm.vhd	93	s	when others
channelcontrol_rtl.vhd	817-818	s	CodeRAM parity errors not injected
channelcontrol_rtl.vhd	221-288	s	TEST code not exercised
coderamarbiterfsm_rtl.vhd	322-325	s	Memory access not pipelined
DMAFSM.vhd	182	s	AHB RECOVERY transition to RETRY not exercised
pldcontrol_rtl.vhd	238	s	when others
twotofivechannelconv_rtl.vhd	231-232	s	FIFO pointer always increased by 2
twotofivechannelconv_rtl.vhd	237-238	s	FIFO pointer always increased by 2

Hardware execution

- Selected tests converted to C programs for LEON2-FT w/ AGGA-4 IP core and executed in KCU105.

```
01-s-boc-2      01-s-cr-5       01-s-e5b-2      01-s-l5-3
01-s-cdl-1      01-s-cr-7       01-s-e5b-3      01-s-pf-1
01-s-cdl-3-1    01-s-cu-1       01-s-fdc-2      01-s-pld-2
01-s-cfg-1      01-s-cu-4       01-s-fdc-3      01-s-pld-3
01-s-cg-2       01-s-cu-5       01-s-if-2       01-s-pld-regs
01-s-cg-4       01-s-ddc-1      01-s-if-3       01-s-vf-3-1
01-s-cg-5       01-s-e1-1       01-s-imt-1
01-s-cg-6       01-s-e1-2       01-simtest
01-s-ch-regs    01-s-e1-3       01-s-l2c-1
01-s-cm-regs    01-s-e5a-1      01-s-l2c-2
01-s-cr-1       01-s-e5a-2      01-s-l2c-3
01-s-cr-2       01-s-e5a-3      01-s-l5-1
01-s-cr-3       01-s-e5b-1      01-s-l5-2
```

Running Tests in HW: AGGA-4 w/ Debug Features



Suitable for running bit-exact, cycle-exact tests of basic AGGA-4 functions in hardware using tests derived from original AGGA-4 ASIC VHDL test cases

AGGA-4 single-clock version shown

Optional debug features

Support for Execution of AGGA-4 VHDL Testcases in HW

- APB R/W transactions to set AGGA4 registers
- GPIO for
  - sampling AGGA4 signals
  - setting AGGA4 signals
  - time-stamping for measurements of pulse duration (execution cycle counter)
- GNSS IRQ CTRL for interrupt detection
  - only transitions from 0 to 1 are sampled and registered
- AGGA4-DSU (debug support unit) for precise execution of timing-critical sections
  - run AGGA4 for a specified number of clock cycles - precise and deterministic execution cannot be implemented via CPU execution due to compiler and cache issues
  - run AGGA4 until a specified event occurs - typically an IRQ or a signal changing to a specified value - cannot be implemented via CPU only since typically several clock cycles lapse before the CPU detects an interrupt
  - allow reading/writing AGGA4 registers while halted to enable precise and simultaneous setup of channels and input signals
- Signal generators for generation of input sequences
  - set signal period - must be divisible by the CoreClock period
  - start signal generation - precise timing has to be guaranteed to ensure correct correlation with the code sequence.

Constructs from the AGGA-4 sim scripting language supported in HW

- `read/write <address> <data>`
- `run <signal> <0/1>` - signal: ASEO, EpochClock, MEO, PPSO, StartOfEpoch
- `run <IRQ> 1` - IRQ: IntEpoch MEInt, PPSInt, PLD5IIRQ, PLDIQITQ
- `def <variable> now` - variable: t1, t2, t4
- `def <variable> 'tx-ty'` - variable: t3, t5
- `compare <variable/signal> <value>` - signal: ASEO, ASC, MEO, PPSO, PPSInt, variable: t3, t5
- ~~`set AUTrigger <0/1>`~~
- ~~`set ExtClock Period <33ns/100ns>`~~
- `set test_start Value 1` - immediate or delayed TestReset
- `set InputXX Start` - immediate or delayed input signal generation

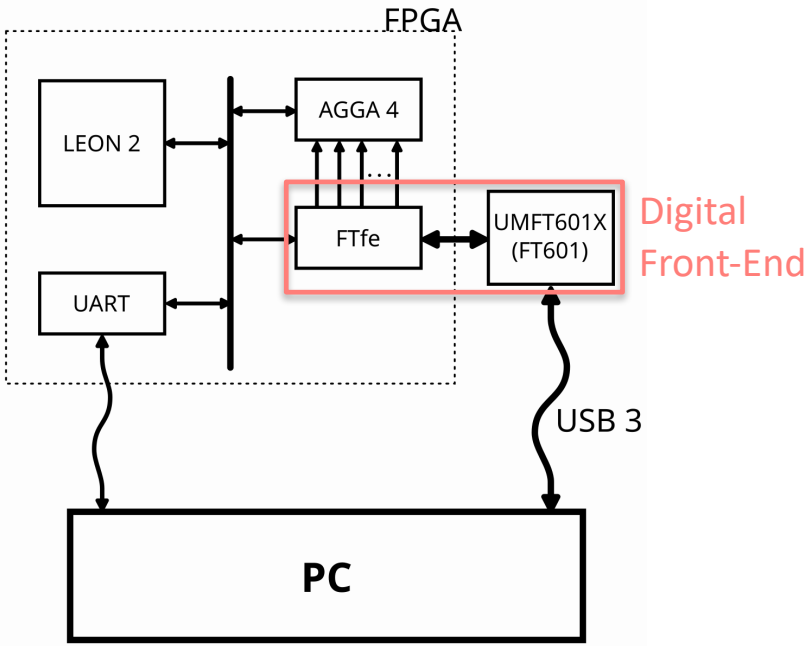
AGGA-4 + Digital Front-End = Hardware-in-the-Loop

LEON2 executes a monitor program that converts commands from UART to read and write accesses to AGGA-4 and DFE registers (LEON DSU)

- AGGA4 – set configuration, read results, control AGGA-4 execution (halt/step/run)
- DFE – set and control distribution of GNSS samples (halt, one sample, number of periodical samples), read trace buffer with released data

PC executes an application that

- configures and halts AGGA-4
- configures data path in the Digital Front-End
- sends data samples to DFE
- sends UART commands to perform tests in AGGA4
- receives results from UART
- evaluates results – AGGA-4 tests or GNSS application software



Conclusions

- New AGGA-4 IP core in the ESA IP core portfolio
  - Supports a number of modern FPGA technologies
  - Better DMA performance
  - High confidence in design correctness due to high code coverage achieved and execution of complex tests in hardware
- New Digital Front-End can be used for design and test of GNSS programs.
- New optional AGGA-4 debug features can be used for cycle-exact debugging of AGGA-4 computation.

THANK YOU