A driven pose estimation for spacecraft in-orbit servicing using FPGA acceleration

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DEPLOYING ONTO THE FPGA Monocular In this poster the proposed **DL method** doesn't apply to classic camera for the close-range phase of the pose estimation. 3D fiducial rendezvous is presented. markers



DPU	С	ZD	X	8	G	ISA1	B512
DPU IP core	CNN (ResNet50)	Hardware platform is Zynq DDR	Quantization method is DECENT™ (Deep Compression Tool)	Quantization bitwidth is 8-bit	General purpose	Instruction Set Architecture version	512 DSP blocks allocated

Resource	Utilization	Percentage in KRIA
LUT	30030	25.64%
LUTRAM	3602	6.25%
FF	41171	17.58%
URAM	18	28.13%
DSP	134	10.74%
BUFG	4	1.14%
PLL	1	12.50%

Platfor mLatencyGPU*126,000 msFPGA30,100 ms		N° instances evaluated	Avg time per instance	
		16,456	7.657 ms	
		100	301 ms	
inferenc	e time given	the resource	utilization.	
inferenc	e time given	the resource	utilization.	
inferenc	e time given State	the resource Avg Powe	utilization. r Consumption	
KRIA	e time given State KR260 Idle	the resource Avg Powe 3.	utilization. r Consumption 820 W	
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shows a performance degradation of 4.22% for position and 10.96% for orientation of the quantized model on the FPGA compared to the original model on the





After quantization, fewer than 30 of 16,456 test images failed, mainly in extreme illumination cases. The model **remains robust** despite quantization and hardware transition. The model outperformed the classic CAT method in handling occlusions, lighting changes, and sudden shifts. Future work could merge both methods or apply filtering for added reliability.

Funan	Total avg. ab	Allow. Error		
Error	GPU*	FPGA	(red lines)	
Position	2.011 mm	2.096 mm	20 mm	
Rotation	0.073 deg	0.081 deg	3 deg	

*NVIDIA GeForce RTX 3070 (5888 CUDA cores). 8GB memory. Driver version 560.35.03. CUDA version 12.6

Future migration to a space-certified platform could be achieved using either a NanoXplore FPGA, which would require a complete redesign due to its unique architecture and lack of compatibility with the Vitis Al workflow, or a radiation-tolerant FPGA from AMD Xilinx. The latter includes options such as the XQR Versal, which offers built-in Al acceleration, improved fault tolerance, and a more familiar development environment, potentially allowing for partial reuse of the existing workflow.