

FEC LDPC codecs for deep space and QKD Reconciliation based on FPGA

R. Prosperococco^(a), B. De Flaviis^(b), D.Giancristofaro^(c), L.Simone^(c), V.Stornelli^(b), G.Ferri^(b), F.Santucci^(a), L.Trotta^(c)

^aUniversità degli studi dell'Aquila (DISIM),
^bUniversità degli studi dell'Aquila (DIEEE),
^cThales Alenia Space – Italia.

Abstract

- Thales Alenia Space Italia often implements FEC codec on FPGA,
- Long dated collaboration with ESA and academic institutions [1],[2], and CCSDS [3].
- TAS-I has implemented PCCC [3],SCCC [1] and LDPC codecs.
- As FPGA technology advances, **efficient high-speed designs require optimized use of hardware architectures**,
- Extrinsic information transfer requires a state-of-the-art trade off among random memory access and switch fabrics.
- Belief propagation for among processors and bit-decision nodes for SCCC, LDPC, and PCCC [4].
- LDPC is currently used in AWGN channels (deep space, ESPRIT [7],[8]), earth observation (PLATINO).
- The present study **implements LDPC on Binary Symmetric Channels (BSC)** for BB84 QKD Reconciliation.
- In-depth analysis of regular and irregular LDPC, using density evolution [5] and progressive edge growth [6] has allowed reducing simulation time via Tanner graph tree analysis [9].

Progressive improvement of LDPC code design

LDPC codes are classically designed following a few subsequent algorithms based on sound theoretical background:

- Probability density evolution theory that leads to variable and check nodes optimal degree distribution (generating non uniform LDPCs);
- Progressive edge growth (PEG) that connects edges among variable and check nodes avoiding cycles shorter than 4 (code girth);
- Subsequent theories (Divsalar) leading to codes with guaranteed minimum distance increasing with block size: these codes belong to the RA, ARA, ARJA categories.

Precoding gain decreases for high rate codes for which the regular codes have already satisfactory performances. This is why the 7/8 or 223/255 code of CCSDS is the only to be a regular one.

Definition of CCSDS LDPC (n=8176, k=7154)

Parity Check Matrix (H)

H is structured as a 2×16 array of 511×511 circulants, where each row of each circulant contains exactly two '1's (positions defined in a table), resulting in a 1022×8176 matrix with rank 1020.

$$H = \begin{bmatrix} A_{1,1} & A_{1,2} & A_{1,3} & A_{1,4} & A_{1,5} & A_{1,6} & A_{1,7} & A_{1,8} & A_{1,9} & A_{1,10} & A_{1,11} & A_{1,12} & A_{1,13} & A_{1,14} & A_{1,15} & A_{1,16} \\ A_{2,1} & A_{2,2} & A_{2,3} & A_{2,4} & A_{2,5} & A_{2,6} & A_{2,7} & A_{2,8} & A_{2,9} & A_{2,10} & A_{2,11} & A_{2,12} & A_{2,13} & A_{2,14} & A_{2,15} & A_{2,16} \end{bmatrix}$$

Derivation Process

The derivation of G from H requires computing the inverse of a matrix in GF(2) to obtain the zi vectors, which are then adjusted to form the first rows of the Bij circulants.

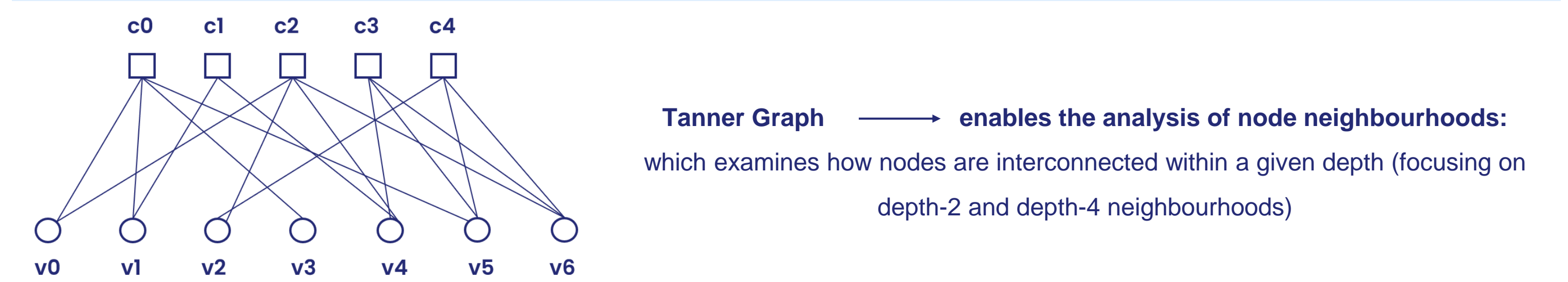
Generator Matrix (G)

G has a quasi-cyclic structure, where the left portion consists of a 7154×7154 identity matrix and the right portion includes two columns of 511×511 circulants.

$$G = \begin{bmatrix} 1 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & B_{1,1} & B_{1,2} \\ 0 & 1 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & B_{2,1} & B_{2,2} \\ 0 & 0 & 1 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & B_{3,1} & B_{3,2} \\ 0 & 0 & 0 & 1 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & B_{4,1} & B_{4,2} \\ 0 & 0 & 0 & 0 & 1 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & B_{5,1} & B_{5,2} \\ 0 & 0 & 0 & 0 & 0 & 1 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & B_{6,1} & B_{6,2} \\ 0 & 0 & 0 & 0 & 0 & 0 & 1 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & B_{7,1} & B_{7,2} \\ 0 & 0 & 0 & 0 & 0 & 0 & 0 & 1 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & B_{8,1} & B_{8,2} \\ 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 1 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & B_{9,1} & B_{9,2} \\ 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 1 & 0 & 0 & 0 & 0 & 0 & 0 & B_{10,1} & B_{10,2} \\ 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 1 & 0 & 0 & 0 & 0 & 0 & B_{11,1} & B_{11,2} \\ 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 1 & 0 & 0 & 0 & 0 & B_{12,1} & B_{12,2} \\ 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 1 & 0 & 0 & 0 & B_{13,1} & B_{13,2} \\ 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 1 & 0 & 0 & B_{14,1} & B_{14,2} \end{bmatrix}$$

Tanner Graphs and node neighbourhoods

Tanner graphs provide a graphical representation of LDPC codes, modelling the **connections** between **variable nodes** and **check nodes** as defined by the parity-check matrix. Understanding the structure of these graphs is essential for analysing decoding performance and optimizing hardware implementations.



Error Patterns Selection (Trapping Sets)

To accurately compute the Frame Error Rate of a codec, an **exhaustive simulation** should ideally be performed, testing all possible error patterns.

$$FER = \frac{\text{Number of error patterns causing decoding failure}}{\text{Total number of error patterns}}$$

Unfeasible: 50 errors on an 8176-bit codeword →

$$\binom{50}{8176} \approx 1.2 \times 10^{116}$$

First Approach: Structured Method for FER Semi-Analytical Estimation

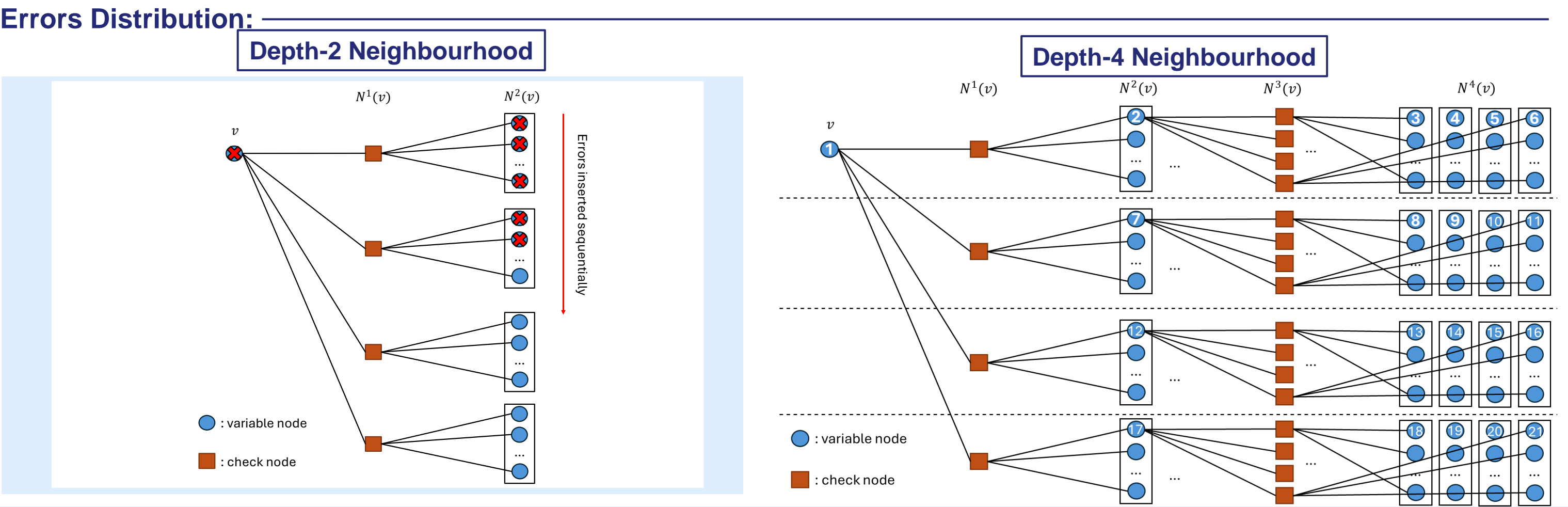
- Identification of the **error patterns most likely to cause decoding failures**: In general, since LDPC is designed to avoid **girth** smaller than 4, we expect that the most critical patterns occur when the errors are filled in paths within a depth-4 neighbourhood.
- Verification via Simulation of the **Threshold** : the minimum number of errors leading to failure.
- Analytical upper bound FER Computation: by comparing the number of pattern groups that lead to failure and the total.
- This analysis provides deeper insights into the properties of the LDPC code.

Second Approach: Monte Carlo Analysis

We performed numerous simulations by randomly injecting errors into codewords. By repeatedly simulating different error patterns, we gathered statistical data that allowed us to approximate the FER.

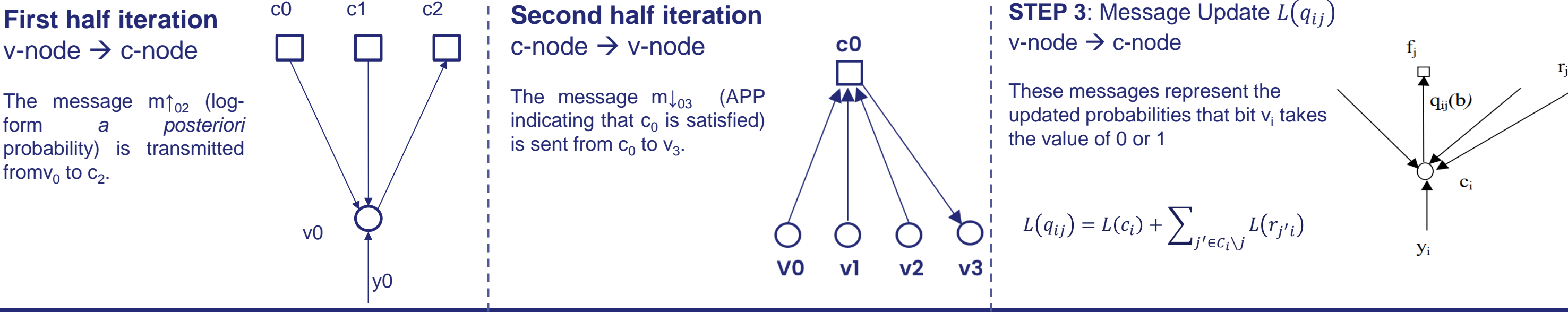
Error insertion strategy

Errors were inserted into different depths of the Tanner graph. Then, errors were spread progressively across 1, 2, 3, and 4 neighborhoods

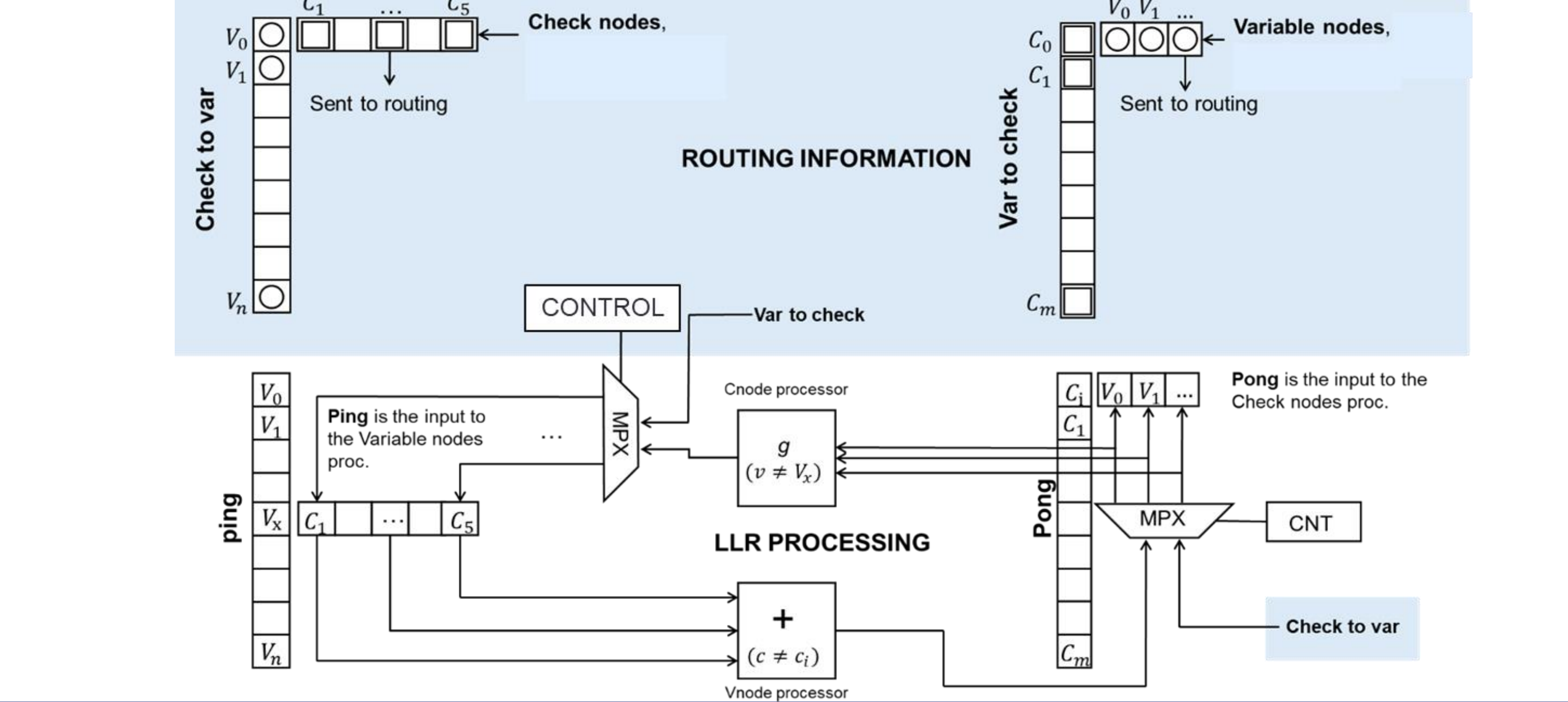


Belief Propagation for LDPC

- An **iterative approach** based on the Tanner graph of the code is used.
- The **variable nodes** represent the transmitted code bits that need to be estimated, while the **check nodes** represent the equations or parity constraints defined by the code.
- The **edges** represent the connections between variables and constraints, along which messages are exchanged.



At the end of a **max number of iterations** or upon reaching a **stopping criterion**, the decoder computes the final LLR to make decisions on the bits v_i .



Code Threshold and Trapping Sets Impact

To evaluate the performance of the LDPC decoder, we analyse the **Frame Error Rate** → $FER = \frac{N_{err}}{N_{tot}}$
where:
• N_{err} represents the number of error patterns that cause decoding failure
• N_{tot} is the total number of possible error patterns: $N_{tot} = \binom{n}{k} = \binom{8176}{k}$

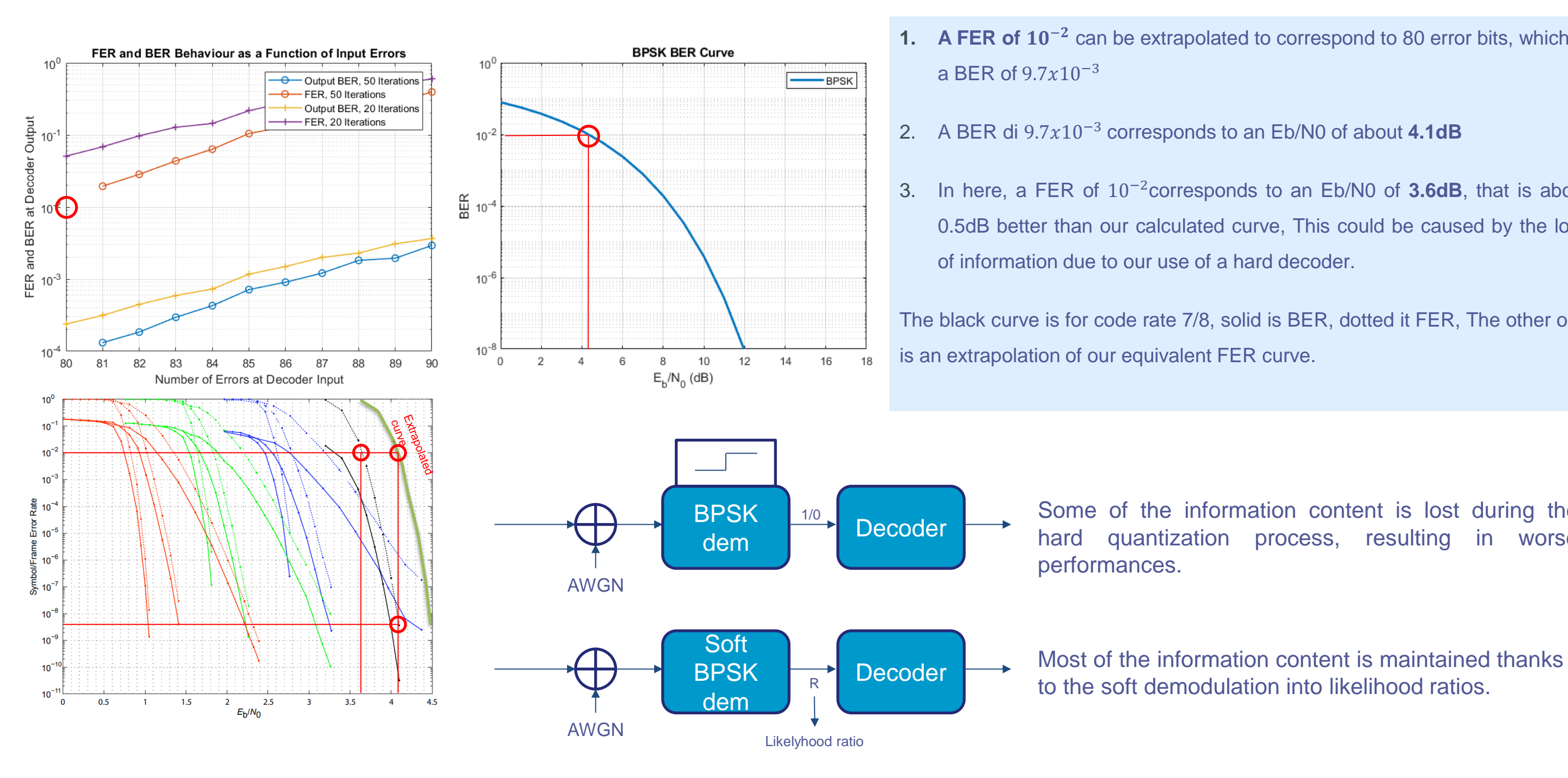
ERROR CASE	62	63	64	65	66	67	68	69	70
1	✓	✓	✓	✓	✓	✓	✓	✓	✓
2	✓	✓	✓	✓	✓	✓	✓	✓	✓
3	✓	✓	✓	✓	✓	✓	✓	✓	✓
4	✓	✓	✓	✓	✓	✓	✓	✓	✓
5	✓	✓	✓	✓	✓	✓	✓	✓	✓
6	✓	✓	✓	✓	✓	✓	✓	✓	✓
7	✓	✓	✓	✓	✓	✓	✓	✓	✓
8	✓	✓	✓	✓	✓	✓	✓	✓	✓
9	✓	✓	✓	✓	✓	✓	✓	✓	✓
10	✓	✓	✓	✓	✓	✓	✓	✓	✓

With this simulation, we observe that the decoder starts failing at **66 errors** and we can see which patterns cause decoding failures.

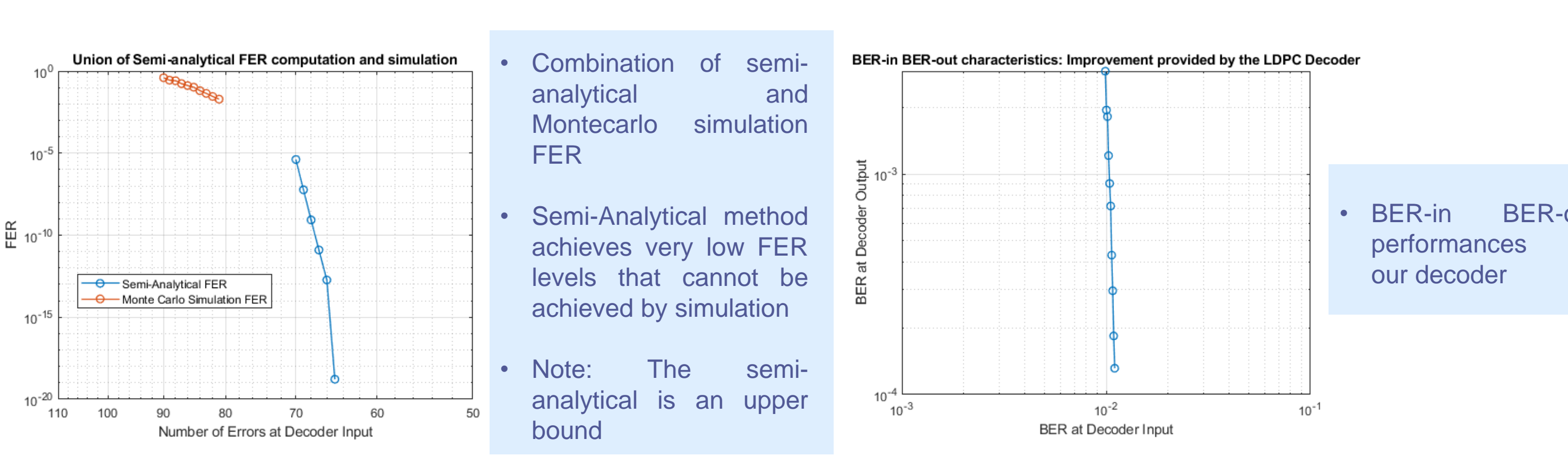
For each scenario, we define a variable representing the **total number of error patterns** with a specific distribution.

However, we consider only the **first occurrence** where a specific error pattern determines the **threshold** beyond which the decoder fails. This is because, once a given pattern causes failure at a certain number of errors, adding more errors will only require placing the new error in any other position among the variable nodes.

FER as a function of BER in (agreement with reference)



Results



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