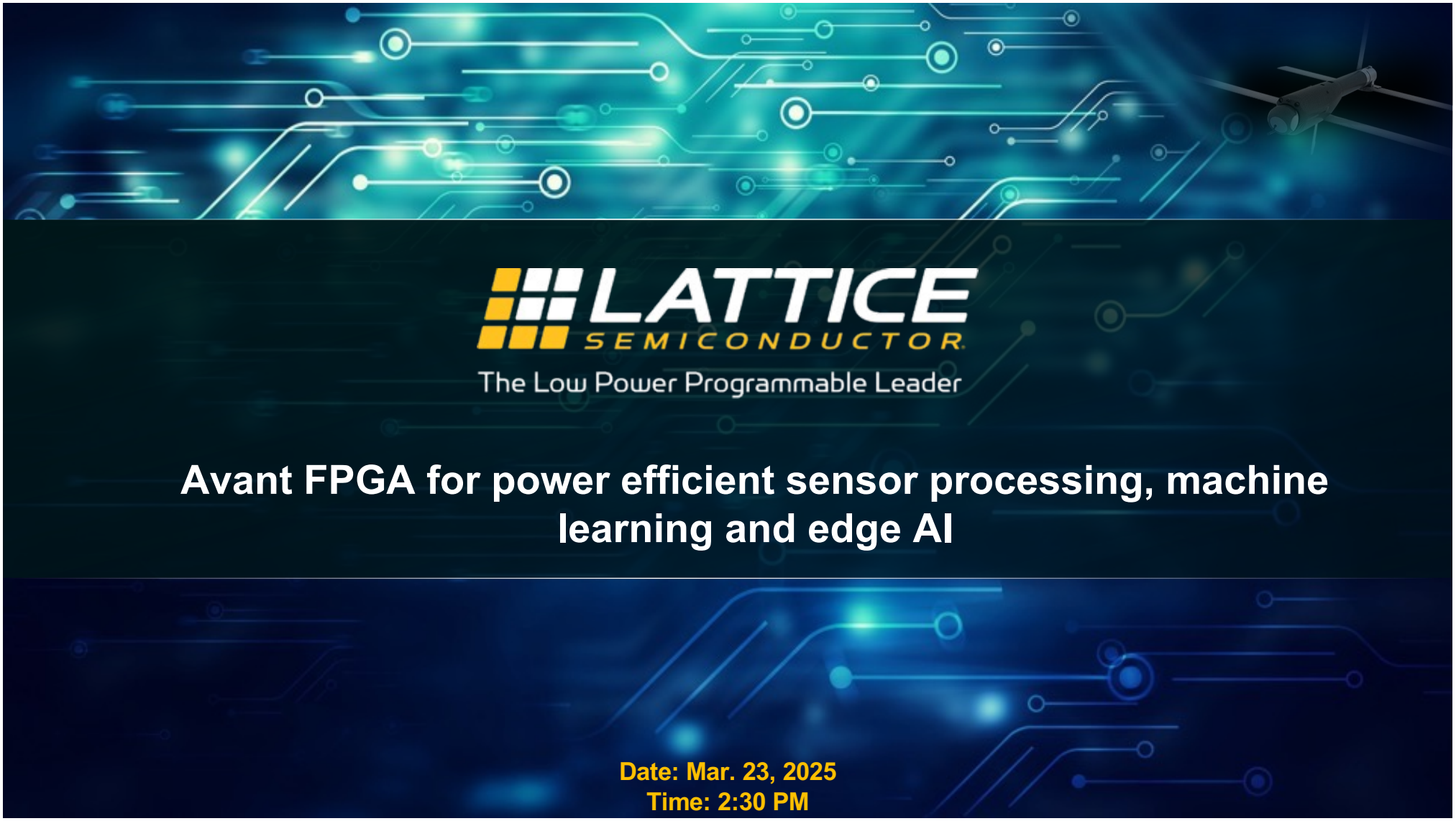


Avant FPGA for power efficient sensor processing, machine learning and edge AI

Date: Mar. 23, 2025
Time: 2:30 PM

Lattice Value in Aerospace & Defense

LATTICE NEXUS™

- Logic density of 17K to 100K LCs
- Max power from 100mW-1W
- 10Gb Serdes, PCIe, USB & DPHY
- SRAM based & Non-volatile options

LATTICE AVANT™

- Logic Density of 260K to 630K SLCs
- Max power from 1W-10W
- 25Gb Serdes, DDR4/5 interfaces
- Hardened Security Engine

LOWER POWER | **HIGH RELIABILITY** | **SMALLER SIZE**

Hardware Security | Enhanced Reliability | Product Longevity | Safety | SWAP-C Optimized | Extended Temperature | Ruggedized Packaging

New Features, Supply Chain Resilience and Fast Cadence of Solutions

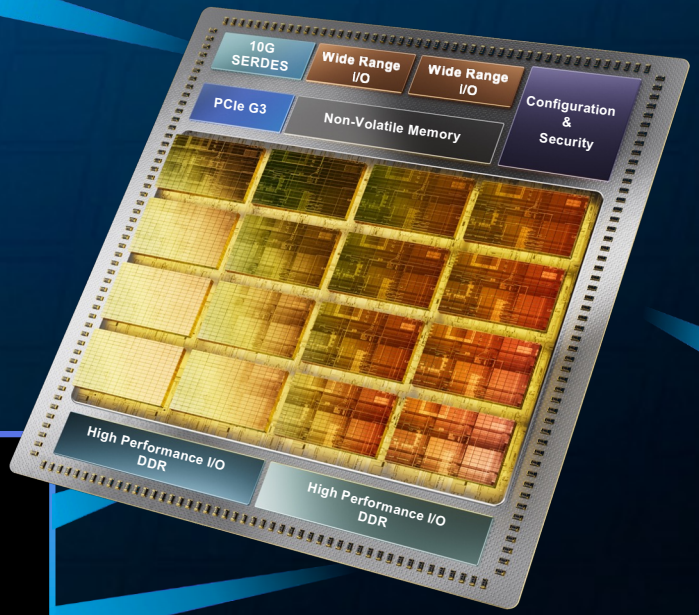
Lattice Nexus Platform Capabilities

HIGH BANDWIDTH INTERFACES

- Multi-protocol Serdes up to 10G
- Supports 10GE, PCIe Gen 3, DP/eDP, SLVS-EC, CoaXPress
- USB 3.2/2.0, MIPI DPHY, CPHY

SECURITY BLOCK

- Bitstream encryption
- Bitstream authentication
- Hashing algorithms – SHA, HMAC
- True Random Number Generator
- AES Encryption



LOW POWER FPGA FABRIC

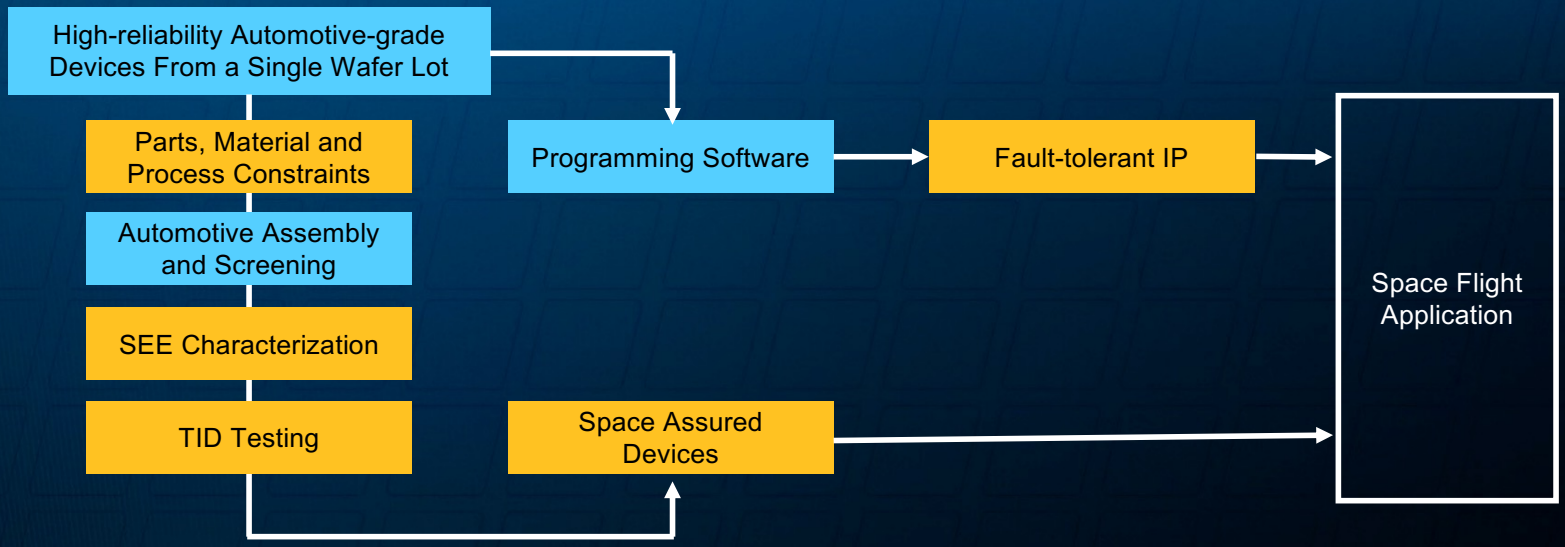
- Built on 28nm FDSOI technology
- Up to 100K logic cells
- SEU resilience
- Ultrafast boot time
- Hardened SED/C Scrubber
- Always-on Options

FAST & FLEXIBLE I/O

- LVCMOS 0.9 to 3.3V
- LVDS / subLVDS up to 1.5Gbps
- SGMII, LVDS 7:1
- DDR3, LPDDR3/4

LATTICE SEMICONDUCTOR

Commercially Developed Technology – Flight Heritage



Lattice Product	Lattice OPN
Certus-NX	LFD2NX-40-7BG256A
CertusPro-NX	LFCPNX-100-8BBG484A

Frontgrade Product	Frontgrade OPN
Certus-NX-RT	UTC24C407
CertusPro-NX-RT	UTC24CP1008

LATTICE SEMICONDUCTOR

- Based on Rad Tolerant 28nm FDSOI technology
- Design and manufacture commercial devices
- Specially built FPGA lots for radiation testing

FRONTGRADE

- Tightly coupled interaction with Lattice manufacturing & source
- Radiation assurance, SnPb
- Augment SW with fault-tolerant IP libraries
- Device traceability

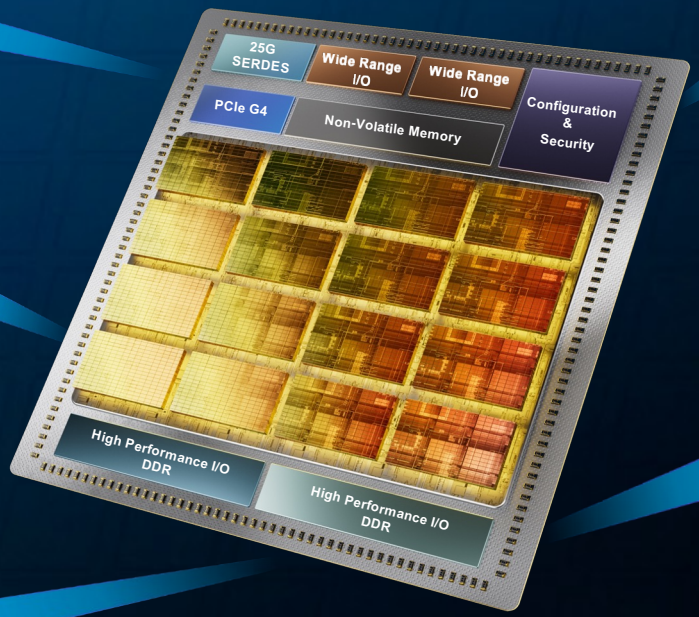
LATTICE SEMICONDUCTOR

Lattice Avant Platform Capabilities

High Bandwidth SERDES
- Multi-protocol PHY Layer
- Hardened Link Layer

Low power FPGA Fabric
- Up to 630K system logic cells
- 36Mb Internal Memory
- 1800 DSPs with 8x8 Support
- Hardened SED/C Scrubber

External Memory Support
- DDR5, DDR4 & LPDDR4, DDR3L
- Hardened DDR PHY
- MRAM
- ECC



Best-in-Class Security
- Post Quantum Ready
- AES256-GCM, ECC & RSA
- Anti-tamper & PUF / Unique ID
- Enhanced SCA Protection
- Rapid Secure Configuration

Fast & Flexible Programmable I/O
- LVCMOS 0.9 to 3.3V
- 1.8 Gbps MIPI D-PHY
- 1.6 Gbps LVDS
- SGMII, LVDS 7:1

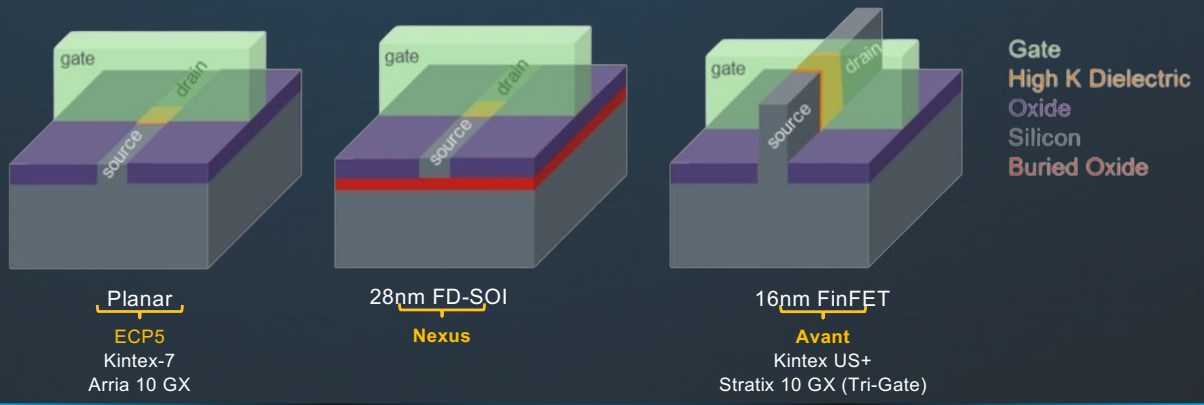
Note: Non-volatile memory as an option

LATTICE SEMICONDUCTOR

Multi-Layered Approach to Creating Rad Tolerant FPGAs

RESILIENCE

Advanced Nodes: Smaller Cross Sections but Higher Probability of SEL & MBU



Radiation Tolerance

Parameter	Description	CertusPro (28nm)	Avant (16nm)	Units
SEL	Heavy Ion Single Event Latch-up Immunity	80	80	MeV-cm2/mg
SEU CRAM	Single Event Upset in Configuration RAM	2.5E-8	4E-8	Events/bit/day [1]
TID	Total Ionizing Dose	>100K	>100K	kRad (si)

Process Technology

- Commercial Scale
- Smaller Critical Active Region Decreases Probability of Single Event Upsets

IC Design

- Proven Foundry Design Rules
- Low Power, No Over-Voltage
- Thoughtful Memory Frame Architecture

Engagement

- Leverage Strength of Ecosystem
- Transparent and collaborative with Radiation Test Consortium
- Lattice + Industry + Agencies + Academia

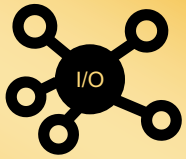
LATTICE SEMICONDUCTOR

Sensors & Solutions

Fusion of VISION, LIDAR and RADAR with Machine Learning

Sensor Opportunities and Challenges

Sensors Are Diverse



Sensor Interface & Aggregation

- Networking
- Bandwidth scaling
- Parallelism

Data quality matters

Sensor Fusing and Preprocessing

- Deterministic
- Synchronous
- Provenance & Security

Fusion & collaboration

Vision and AI Processing

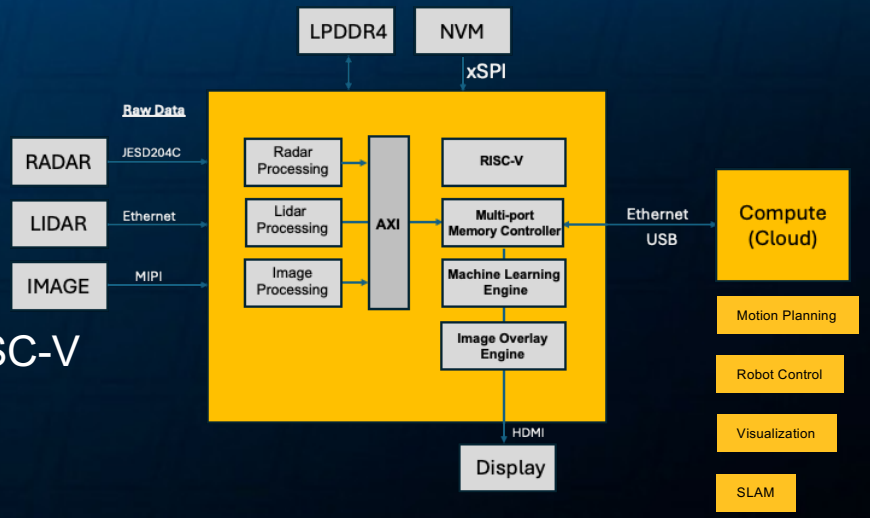
- Collaborative Algorithms
- Hard vs. Soft
- Real-Time

Conventional and AI Algorithms Co-exist to Propel Software Defined Sensors

LATTICE SEMICONDUCTOR

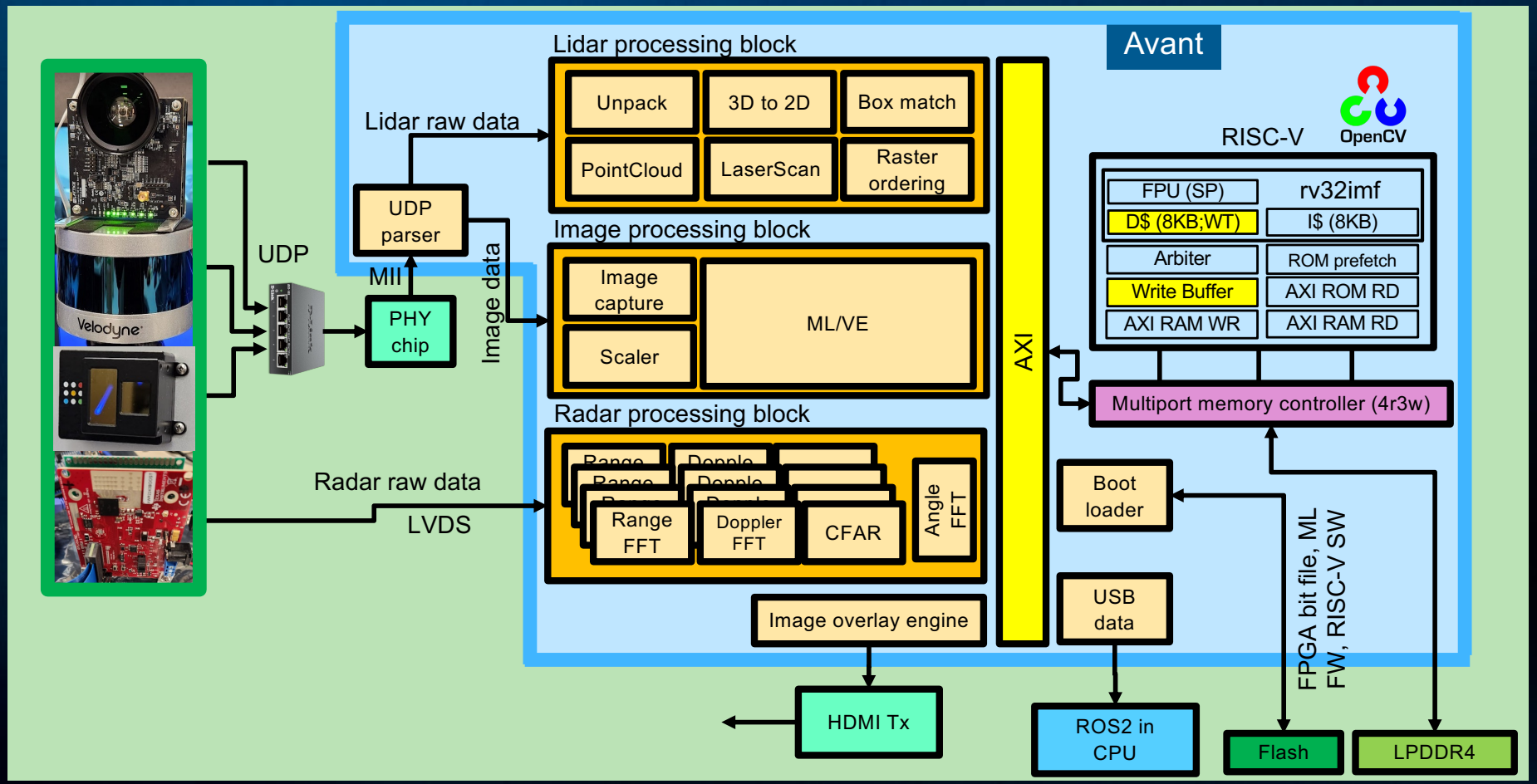
Sensor Fusion & Machine Learning

- **Lattice Avant FPGA**
  - Sensor Fusion of Vision, Lidar and Radar
  - Leverage onboard DSP, memory
  - Interface & synchronization sensors
  - On-board Processing & collaboration with built-in RISC-V
  - Total power less than 1W
  - Open source, Low latency, Low Power Open source



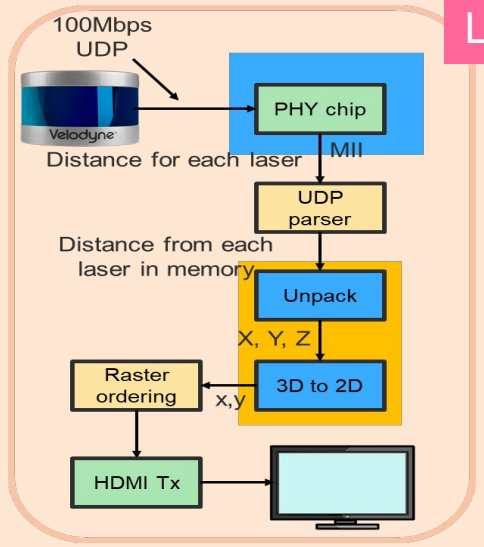
Type of Sensor	Sensor Interface	System Interface to Host
Vision	MIPI CSI-2, SLVS-EC	GigE Vision, USB Vision, CAN, GMSL, Ethernet, PCIe, USB, I2C, SPI
Radar	MIPI CSI-2, LVDS, JESD204C	Ethernet, PCIe, USB, SPI
Lidar	Ethernet	Ethernet, PCIe, USB
Position	GPIO	Ethernet, Industrial Ethernet, PCIe, USB
IMU, Others	I2C, SPI, UART	Ethernet, PCIe, USB, I2C, SPI, UART

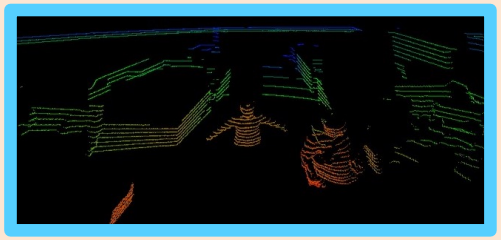
Hardware Overview

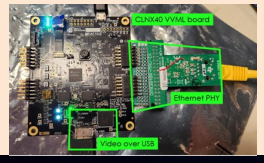


Software Overview

Lidar

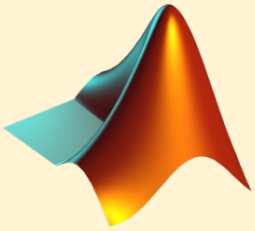






CLNX40,
CNX40,
CPNX, Avant-E

Module Gen

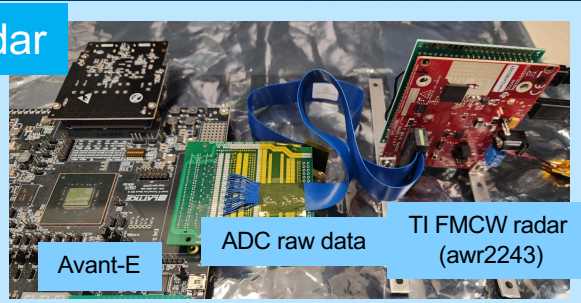


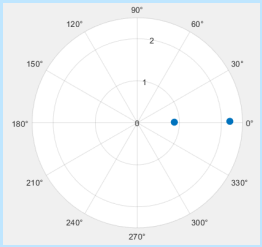
open source HLS

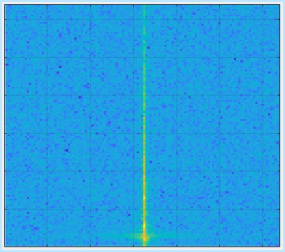
OpenCV

Sim, IPs

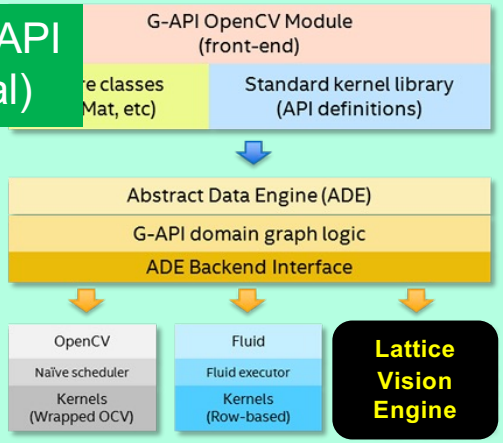
Radar







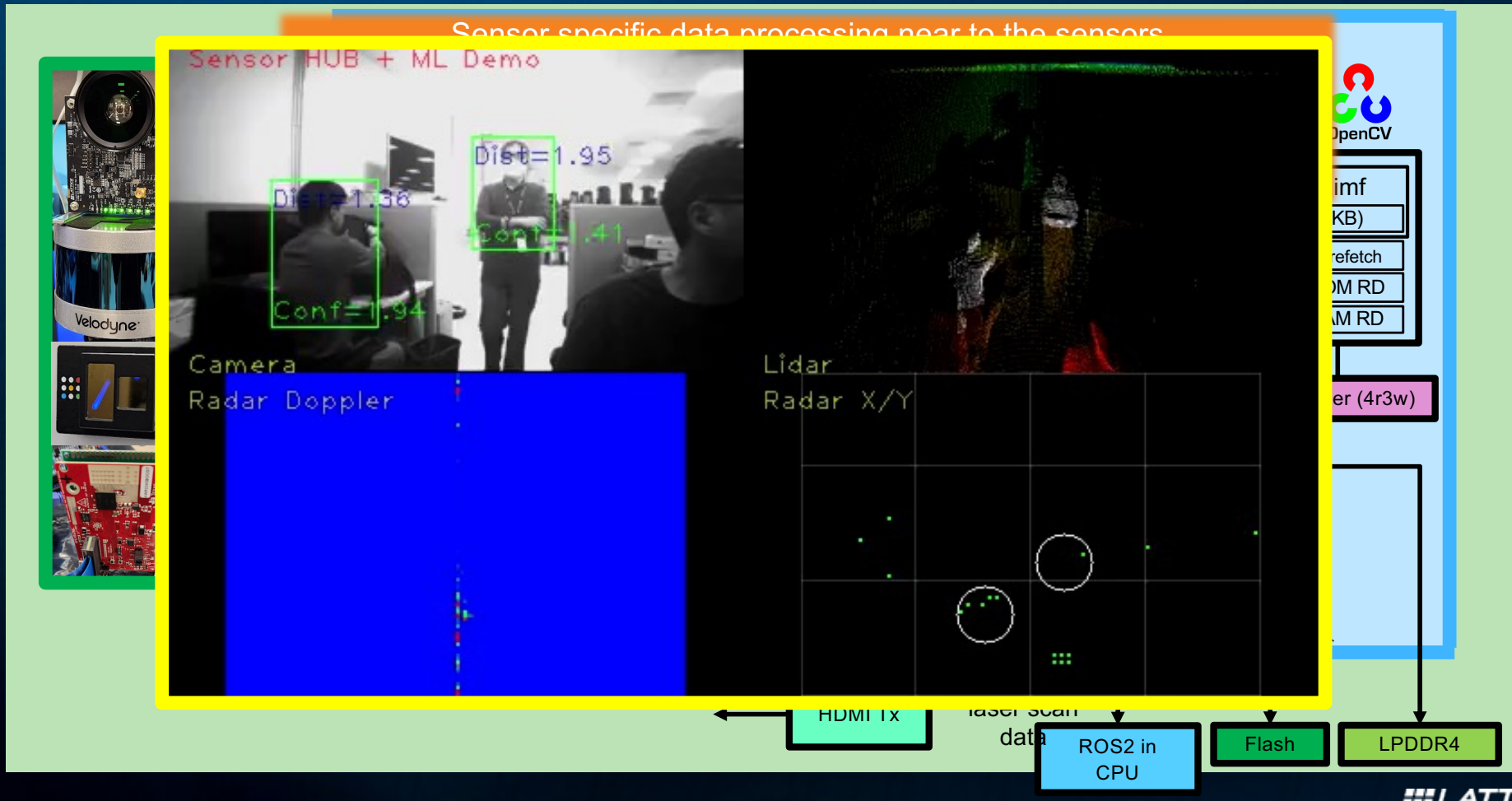
OpenCV G-API
(bare-metal)



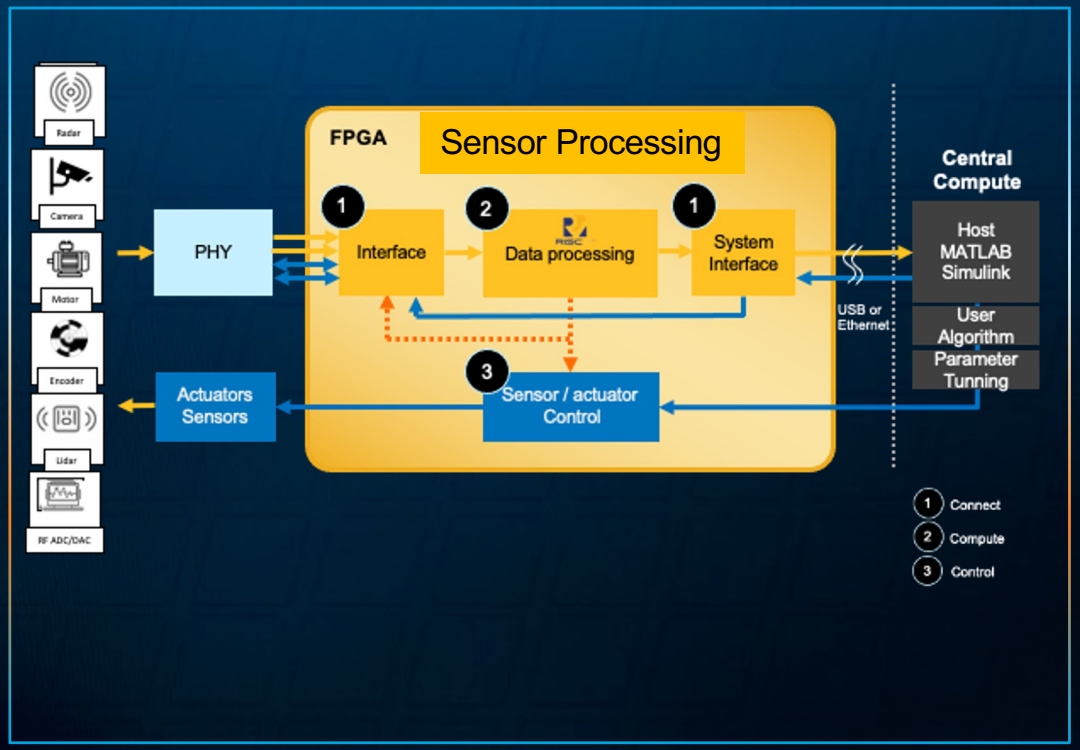
Ease of use (VE)

LATTICE SEMICONDUCTOR

Fusion of VISION, LIDAR and RADAR with Machine Learning



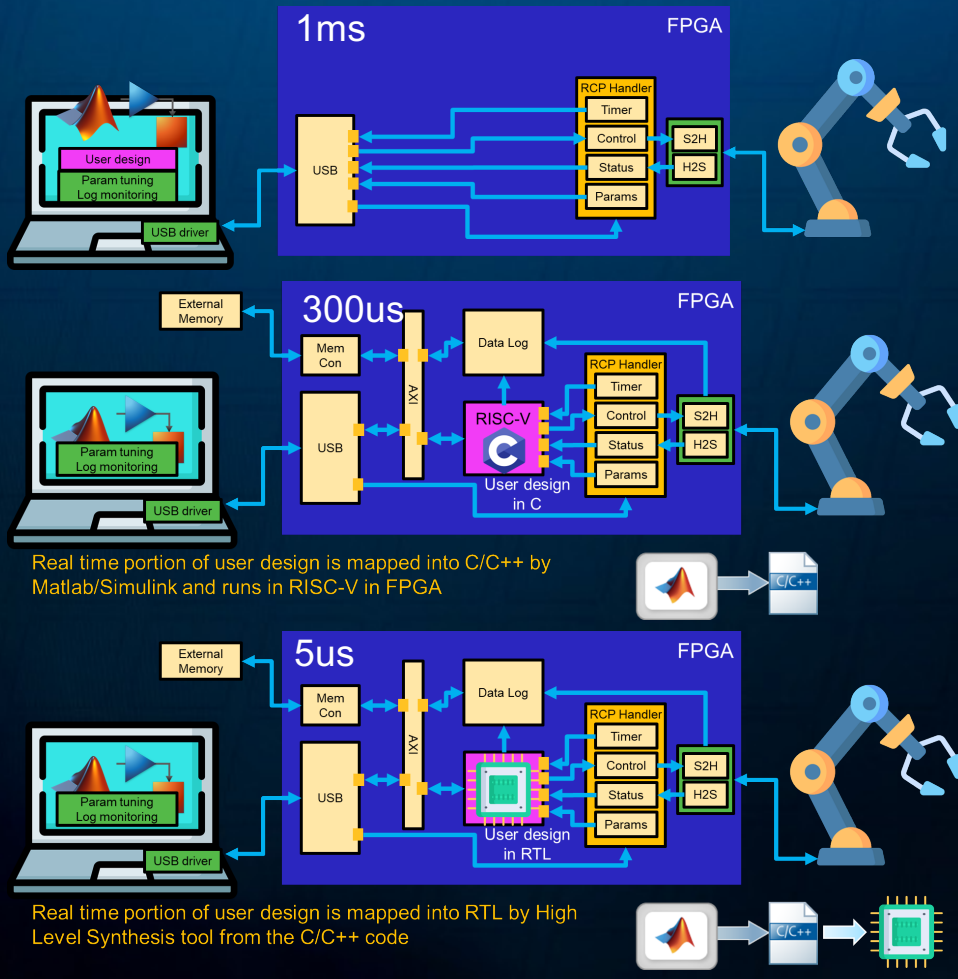
Hardware in the Loop to Develop and Optimize Algorithms

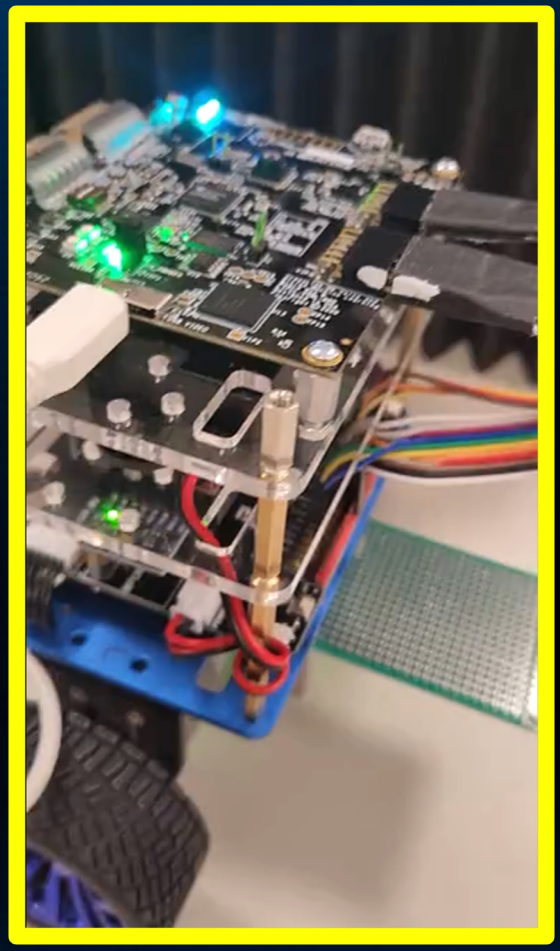


- Implement, simulate and validate sensor specific data processing near sensor
- Fusion of sensors that complement each other
- Open source, less than 1us latency and ultra low power
- Transfer meta data to CPU /GPU over high bandwidth communications

LATTICE SEMICONDUCTOR

Hardware-In-The-Loop Design/Verification Flow

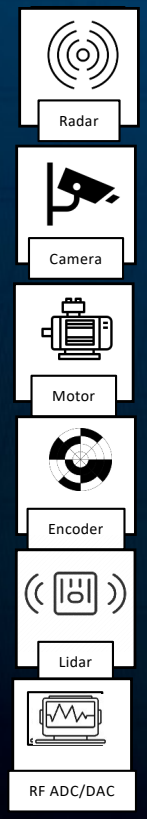


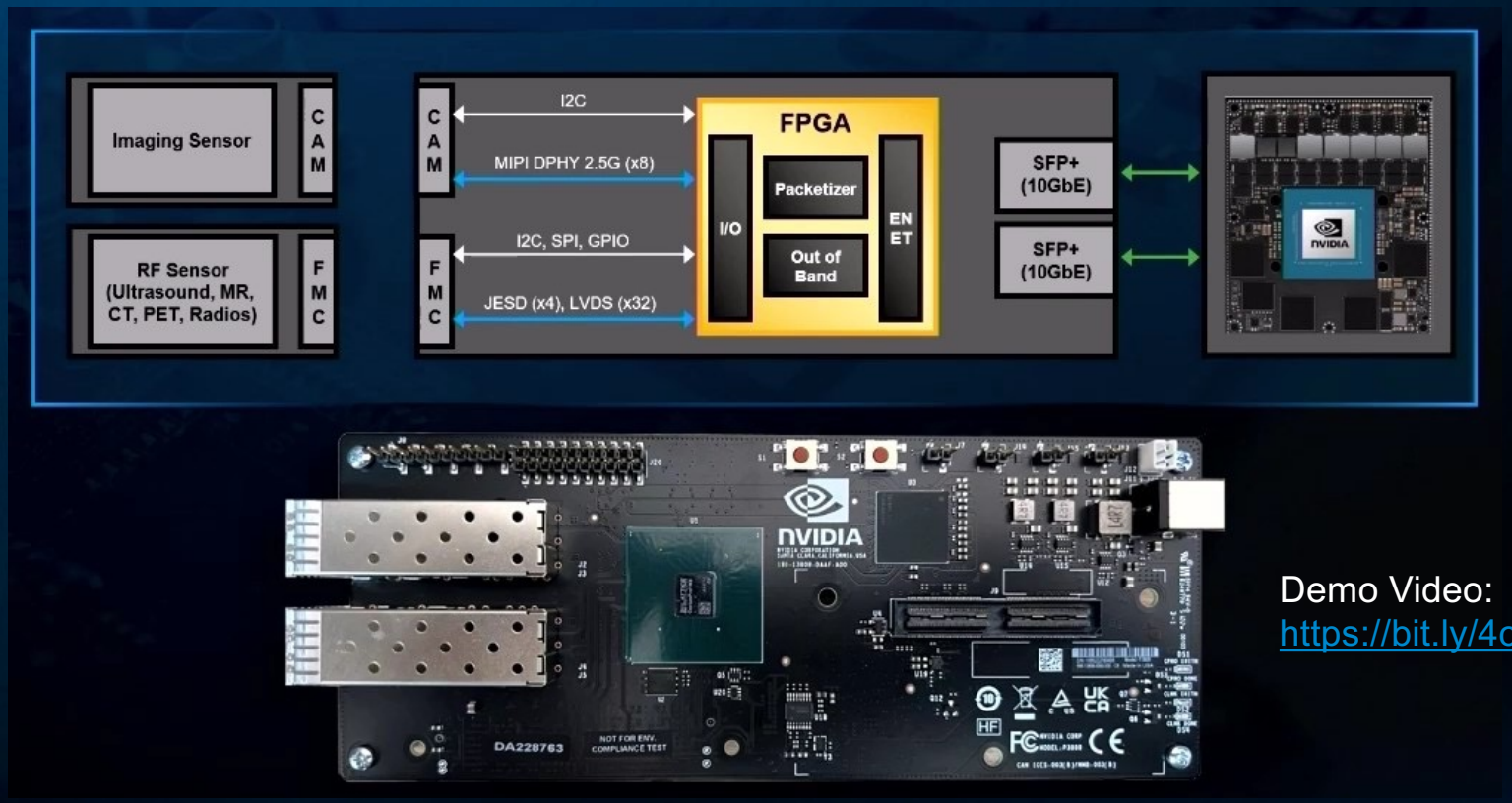


LATTICE SEMICONDUCTOR

Sensor Fusion to Higher Level Processing

- Open source, scalable, low latency and high performance | EA now, broad availability in Q4 2024





Demo Video:
https://bit.ly/4cNPVzG