NanoXplore SEFUW

- March 2025

NanoXplore

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Company Overview

- French Based Company
- 140+ Employees with more than 90% R&D Engineers
- 3 different products offering
  - High reliable SoC FPGA
  - ASIC design services
  - Silicon IPs
- ITAR Free Technology
- Focus on Space & Defense markets

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Recent Acquisition of Dolphin ASIC

- Better address European sovereign markets like Defense and Space
- Very strong track record in delivering complex ASIC
- 30 years of ASIC delivery to defense market
- STMicroelectronics Foundry partner
- STMicroelectronics OSAT partner for Testing and Packaging

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Product Strategy

Main Products Offerings

FPGA

- SoC FPGA and FPGA
- Only European solution
- Focus on key differentiators
- Focus on Space, Defence and Avionics markets

IPs

- Silicon proven IPs in 28nm FD-SOI and 7nm FinFET
- DDR Phy
- eFPGA
- SSTL I/Os
- PLL
- Rad-hard standard cells libraries

ASIC

- NXDS offers Turnkey Service for complex ICs
- Restricted area for secured design environment
- Strong expertise in FD-SOI
- ARM partner

Key Differentiators

- Radiation Hardened
- Trusted / Security
- European Supply chain

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Rad-Hard FPGA Portfolio Overview

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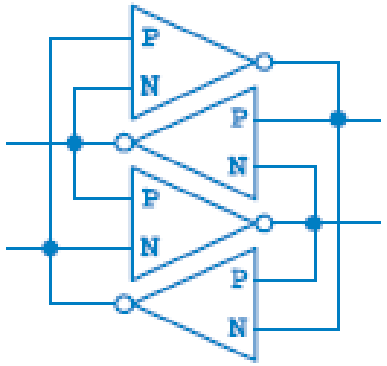
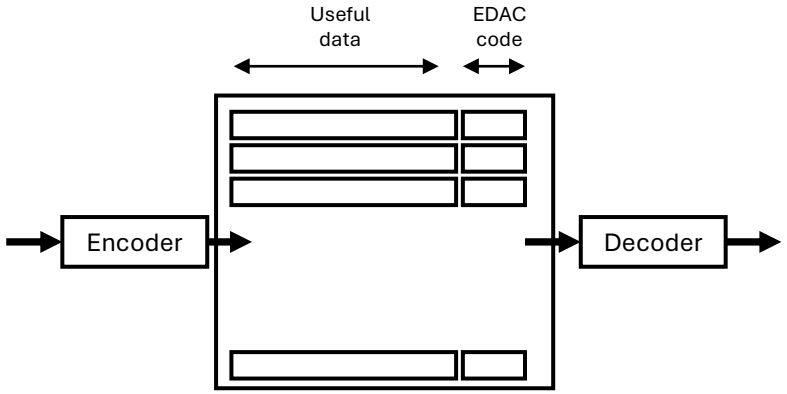
Rad-Hard FPGA Offering

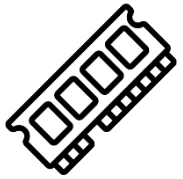
SEE Immune

Structure DICE

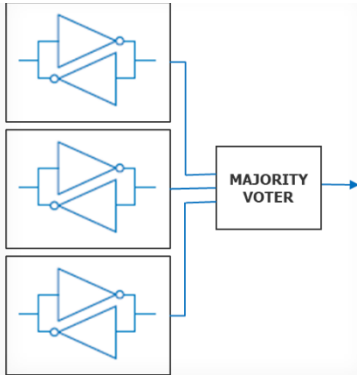




Memory EDAC



Critical Register TMR



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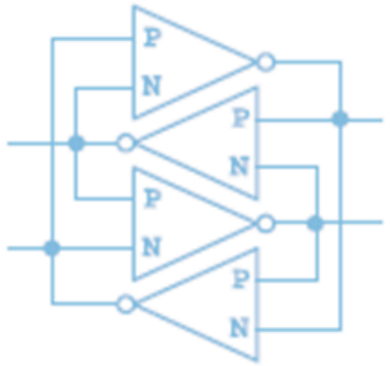
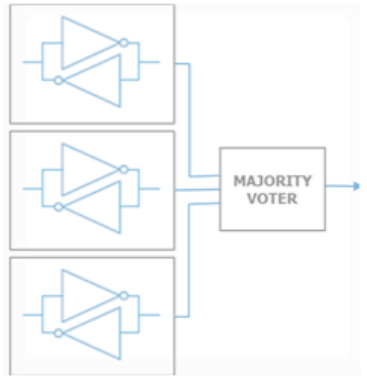
Rad-Hard FPGA Offering

SEE Immune

Structure DICE



Critical Register TMR



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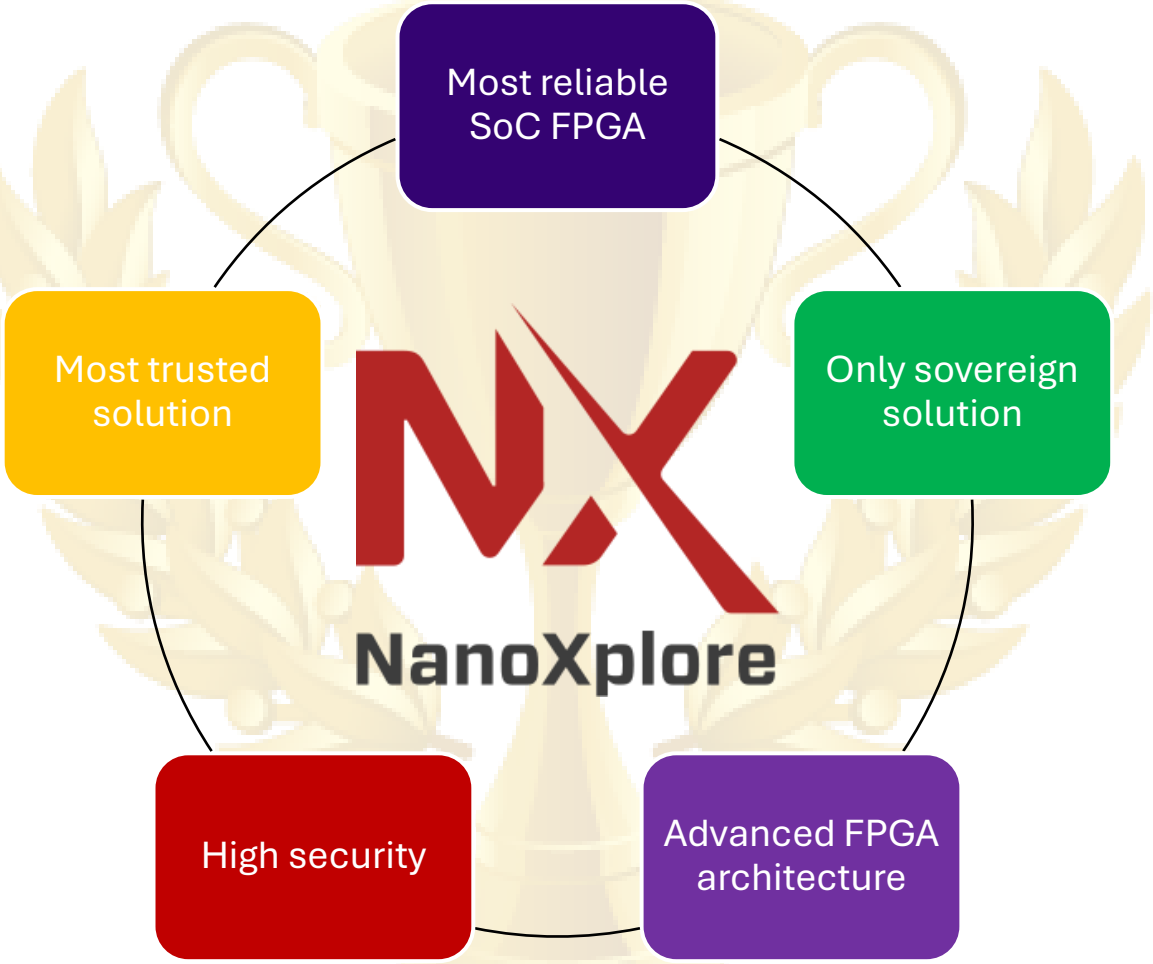
NX Key Differentiators



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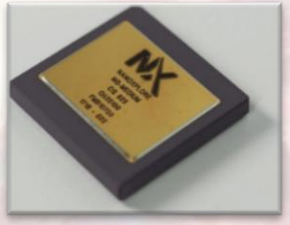
NX Products Overview



NG medium

65 nm

Low-End FPGA

- 35kLUTs/32kDFFs
- 3Mb RAM
- 112 DSP
- No HSSL
- No Hard IP Processor

- Companion chip

ESCC9000 qualified

ultra 300

28 nm

Mid-End FPGA

- 290kLUTs/273kDFFs
- 21Mb RAM
- 896 DSP
- 16x HSSL 12G
- ADC/DAC

- Payload
- Platform
- Sensor control
- Power control loop

NG ultra

28 nm

High-End FPGA

- 537kLUTs/505kDFFs
- 32Mb RAM
- 1344 DSP
- 32x HSSL 12G
- Quad-core ARM-R52 (SoC)

- Payload
- Platform

65 nm → 28 nm

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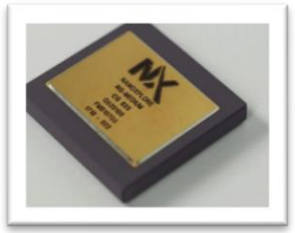
Radiation Testing Overview

NG medium

65 nm



Heavy Ions	✓
Protons	✓
TID	✓
Latchup	✓
ESCC	✓

NG ultra

28nm – FDSOI

Heavy Ions	✓ (still HSSL)
Protons	✓ (PS Only)
TID	✓
Latchup	✓
ESCC	■ 2025

ultra 300

28nm – FDSOI

Heavy Ions	■ 2026
Protons	■ 2026
TID	■ 2026
Latchup	■ 2026
ESCC	■ 2027

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NG MEDIUM - Flight Heritage

One of our components is on space !

Hera

Detailed post-impact survey of the target asteroid, Dimorphos

DORn

Detection of Outgassing RadoN on the moon

SVOM

Space Variable Objects Monitor. Study the gamma-ray bursts from explosion of stars (LEO)

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Rad-Hard FPGA Portfolio Overview

NG-ULTRA Update

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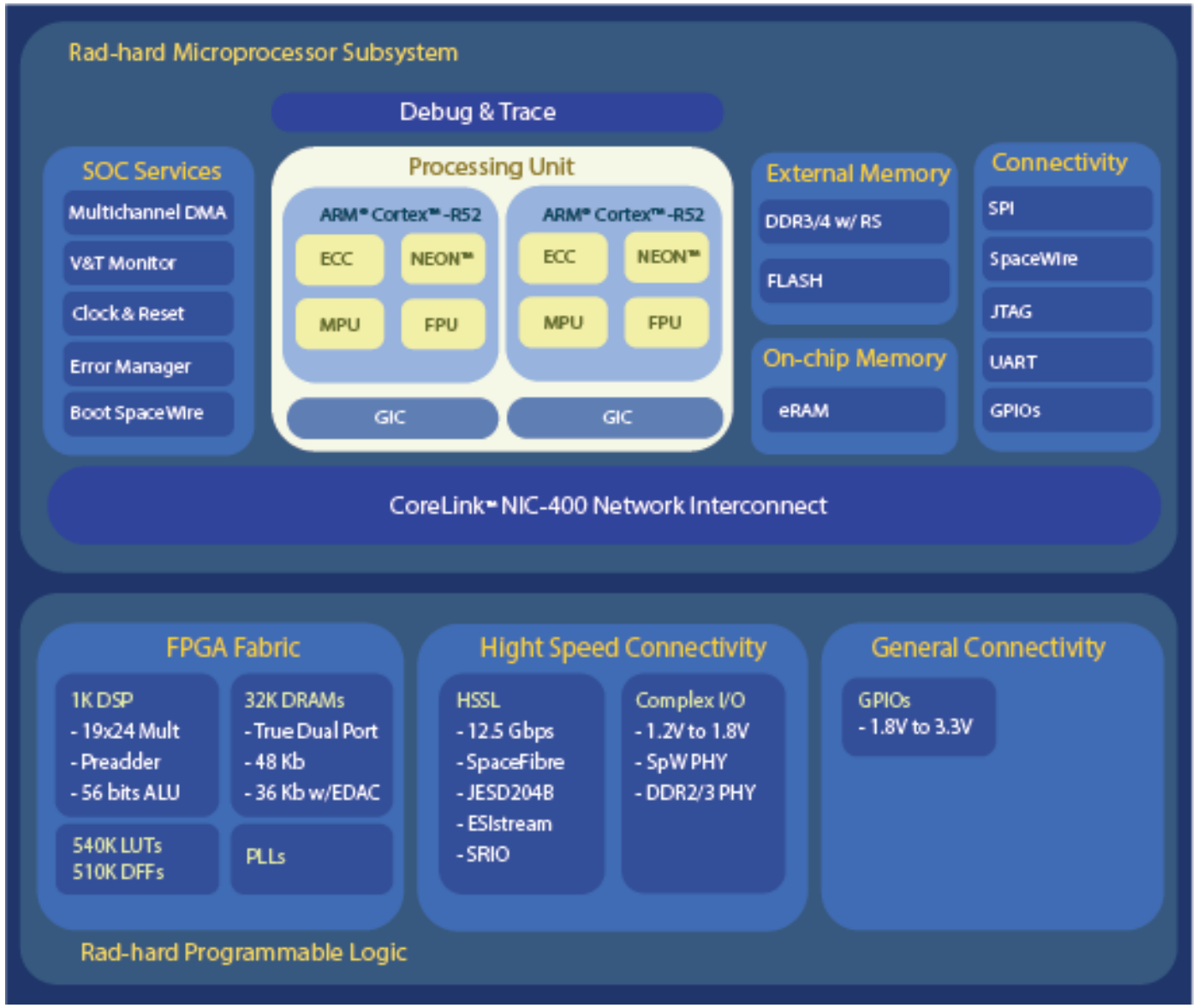
NG ULTRA – Overview



- Dual SoC component :
  - Quad Cortex-R52 @600MHz
  - 500K LUTs FPGA Fabric
- 28nm technology
- SEE Immune
- Sovereign supply chain
- First flight models already delivered
- 2 qualifications grades :
  - ESCC9030 -> Class 1
  - JEDEC -> New Space

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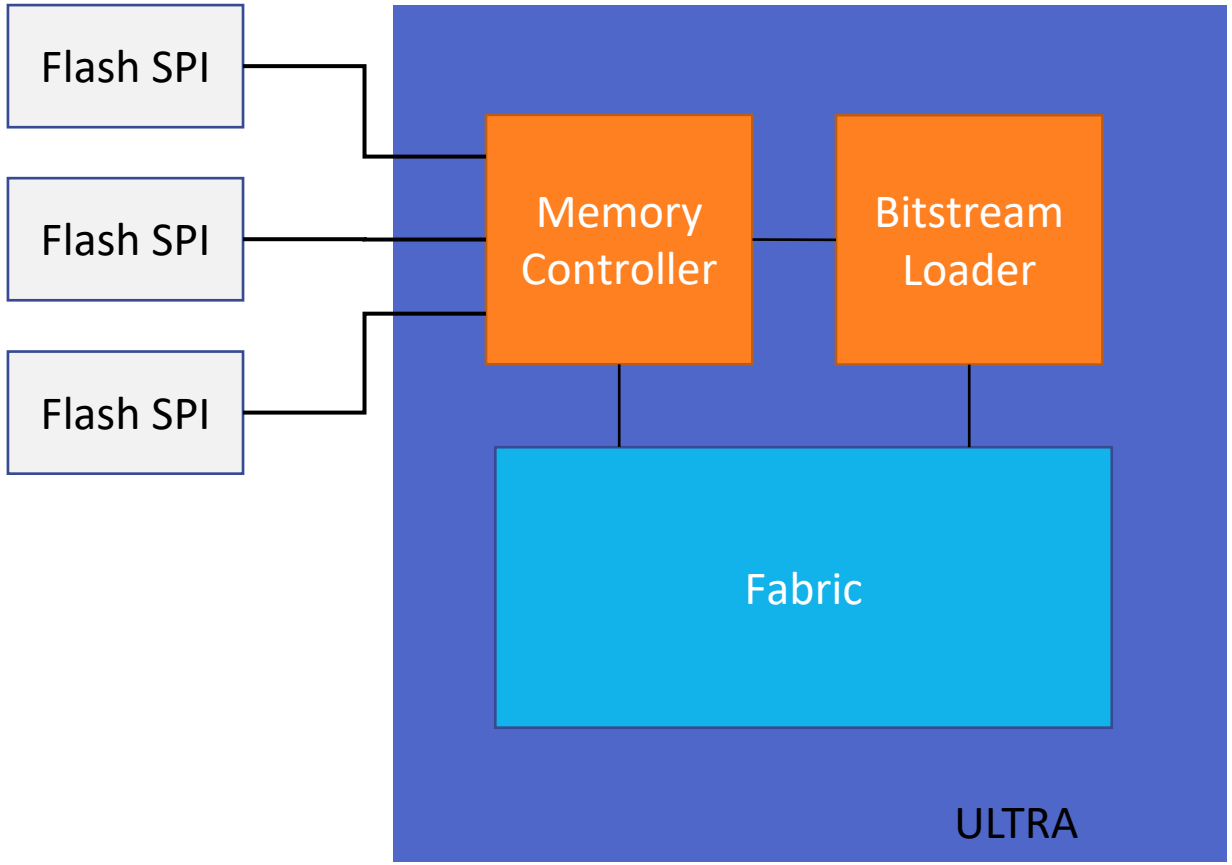
ULTRA – Boot loader



- SPI interface
- Internal TMR Mode
- Multiple bitstream management

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Test Radiation Results

Test	Number of Tested Samples	Total Fluence All Samples	Result
CRAM	3	3.96E+07	Immunity
DPRAM	2	1.22E+07	Immunity with ECC enabled
WSR	2	2.03E+07	Immunity
PLL(1)	2	1.72E+07	Very few events
RF	2	2.10E+07	Immunity
DSP	2	6.10E+07	Rare events only at high LET
IO	2	5.84E+07	Rare events only at high LET
HSSL TX	2	3.81E+07	Very few events
BSM Load	2	2.00E+07	Immunity

SEE Immune
SEL Immune
TID (50krad)

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NG-ULTRA Software eco-system - BSP

NG-Ultra BSP Welcome guide

Introduction

The Board Support Package (BSP) is a bare-metal environment containing:

- **drivers** for the NG-Ultra devkit,
- **utils** to abstract hardware capabilities & test
- sample **applications** on board.
- the **nxbuilder** build system

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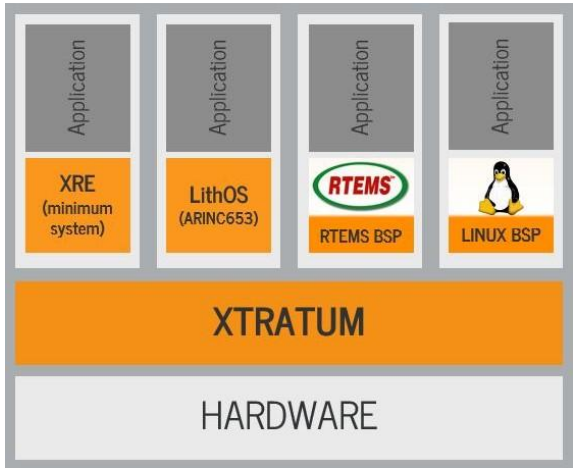
NG-ULTRA OSs

- Xtratum by Fentiss:
  - XNG Hypervisor
  - **RTEMS6** QDP BSP as partition
  - Guest Linux
  - Baremetal as partition
- PikeOS for MPU by SysGO
- Zephyr OS (POC)



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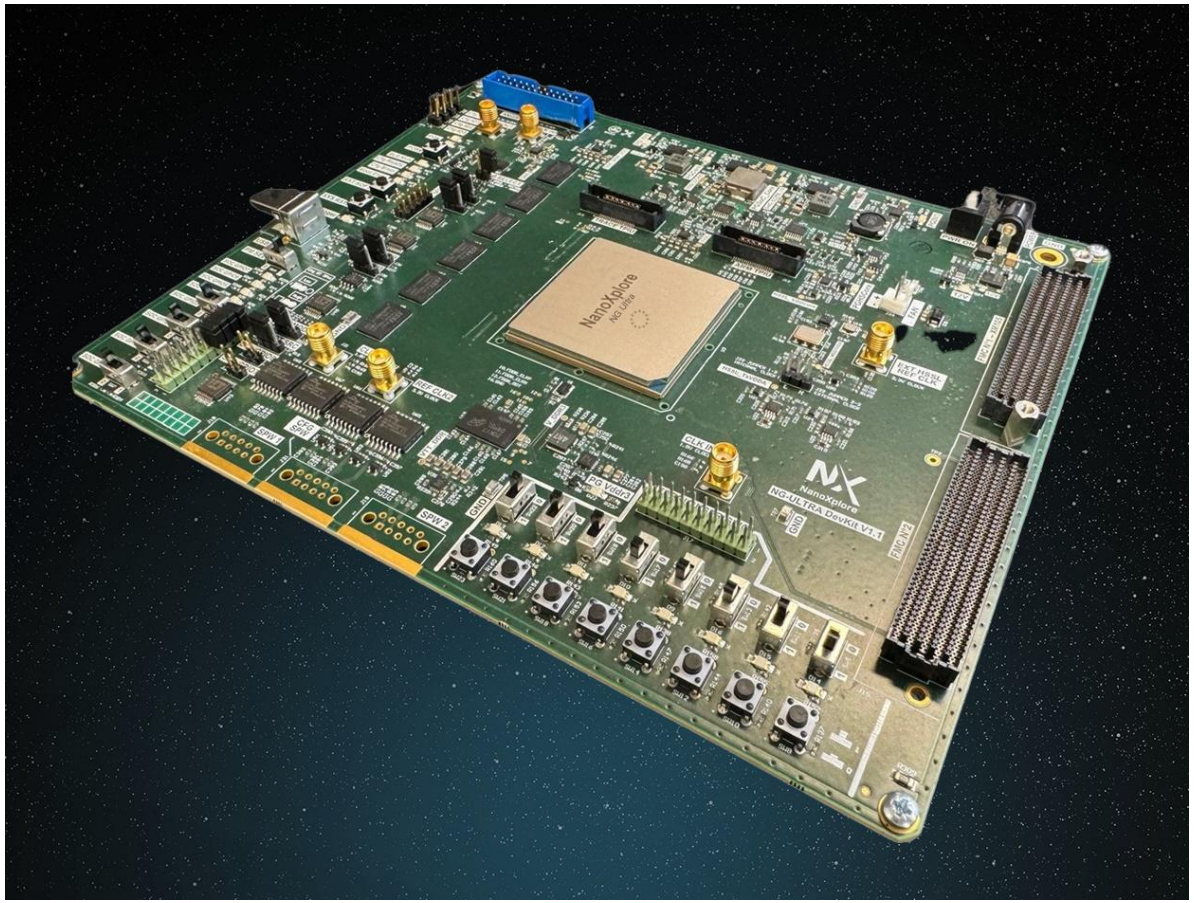
NG ULTRA - Milestones

- Prototype : available
- Evaluation kit : available
- FM (without HSSL) : available
- ESCC 9030 qualification : Q2 2025
- FM with HSSL : Q2 2026



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Rad-Hard FPGA Portfolio Overview

ULTRA300 Update

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ULTRA 300 – Overview

Device		Details	NX2H300TSA
Capacity - ASIC Gates	Rad Hard FPGA		**4 000 000**
Logic Modules		11x Tiles + 7CGBs	
Register		384DFF on 11rows	**273 408**
LUT-4		408LUT on 11rows	**290 496**
Carry		96CY on 11rows	**68 352**
Embedded RAM			**22Mb**
DPRAM		448BRAM * 48Kb	**21 504**
Core Register File		On 11 rows	**1 424**
Core Register File Bits		32*18bits	**807K Hardened**
Clocks / PLL			**50 / 6**
Additional Features	Rad Hard SOC		
SpaceWire PHY (8 IOBs)		2x/Complex IOBank	**20**
DDR3/4 PHY (11IOBs)		2x/Complex IOBank	**20**
DSP Blocks		From 7 rows	**896**
SpaceWire link I/F 430Mbps		CODEC	**1**
SERDES Tx/Rx 12,5Gbps (supporting several protocols such as Space Fibre)		4 Quad HSSL 12,5Gbps	**16**
Hard IP Processor core / SoC			**NO**
ADC		12-bit ADC, 10Msps	**1**
DAC		13-bit DAC, 10Msps	**1**
Design Security			**YES**
Inputs / Outputs	I/O		**547 I/Os**
Complex I/O bank		VIO 1,2 – 1,5 – 1,8V	**10 x 34 I/Os**
Simple I/O bank		VIO 1,8 – 2,5 – 3,3V	**6 x 24 I/Os + 1 x 16 I/Os**
Packages - User I/Os	PKG		
FF484 organic		27*27 mm / 1 mm	**239 I/Os (TBC)**
FF1152 organic		35*35 mm / 1 mm	**547 I/Os (TBC)**

- SEE immune
- HSSL @ 12 Gbps, compatible with SpaceFibre, JESD204B, ESIstream, SRIO
- 12 bits ADC and 10 bits DAC
- Packaging: BGA 484 and BGA 1152
- Same technology as NG-ULTRA platform
  - Radiation / Library / Testing / Supply Chain

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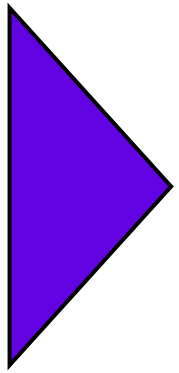
ULTRA 300 – Power Consumption

- Illustrative power consumption of ULTRA300 based on the following **resource intensive** design:
- DFF 107k
- LUT 250k
- RAM 250
- Register file 232
- Clock 50MHz



- Power consumption by rails @Tj 85°C
- 1V Fabric dynamic = 0,7W
- 1V Fabric static = 2,4W
- 1V8 IO = 0,1W
- 3V3 IO = 0,1W
- **Total = 3,3W**

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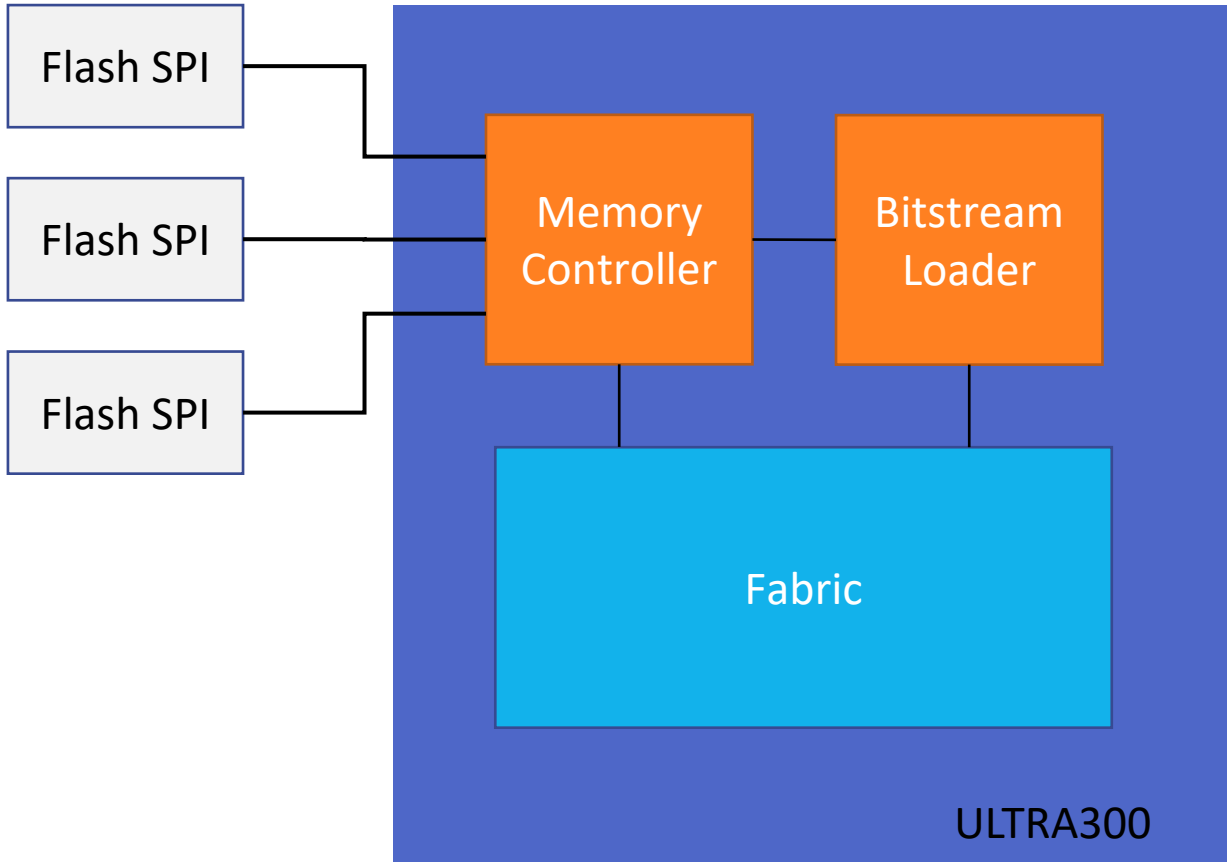
ULTRA 300 – Boot loader



- QSPI interface
- Internal TMR Mode
- Multiple bitstream management

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ULTRA 300 – Milestones

- IMPULSE: available
- Engineering samples : available
- Evaluation kit : Q2 2025
- Prototypes : Q4 2025
- FM : Q2/Q3 2026
- ESCC 9030 qualification : Q1 2027

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New Space Markets

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New Space Markets

Reliability and cheap

Flexibility

- Same die / package footprint
- Various screening to address all space missions requirements

Economy

- Less screening testing
- 5-10x price reduction vs. class 1

No compromise

- Same die to reach the same radiation performance
- Same supply chain

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NG Ultra Family

Space qualified FPGA

NG ultra RH

- ESCC9030
- SnPb Organic BGA 1760
- Fully Immune
- Space Grade Capacitors
- Space Class 1

New Space COTS FPGA

NG ultra JEDEC

- JEDEC
- Leadfree Organic BGA 1760
- Fully Immune
- General Purpose Capacitors
- Space Constellations, Avionics, Military & Defense

NG ultra COTS	NG ultra ESCC9030
~~External VI~~	External VI
FT 1 Temp (Hot)	FT 3 Temp
~~Burn In~~	Burn In
~~FT 3 Temp~~	FT 3 Temp
Optical VI	Optical VI
~~External VI~~	External VI
~~Solderability~~	Solderability
Baking	Baking

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NG Ultra 300 Family

Space qualified FPGA

ultra 300 RH

ESCC9030

SnPb Organic BGA 484 & 1152

Fully Immune

Space Grade Capacitors

Space : Class 1 & Class 2

New space COTS FPGA

ultra 300 JEDEC

JEDEC

Leadfree Organic BGA 484 & 1152

Fully Immune

General Purpose Capacitors

Space Constellations, Avionics, Military & Defense

Ultra 300 COTS	Ultra 300 ESCC9030
~~External VI~~	External VI
FT 1 Temp (Hot)	FT 3 Temp
~~Burn In~~	Burn In
~~FT 3 Temp~~	FT 3 Temp
Optical VI	Optical VI
~~External VI~~	External VI
~~Solderability~~	Solderability
Baking	Baking

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SoC FPGA Roadmap

- New SoC FPGA in 28nm FD-SOI
  - Fabric performance x50%
  - Linux in Space
  - State of the art boot secured
- Chiplet FPGA
- 7nm FinFET
- …

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NX Design Suite tools

Impulse

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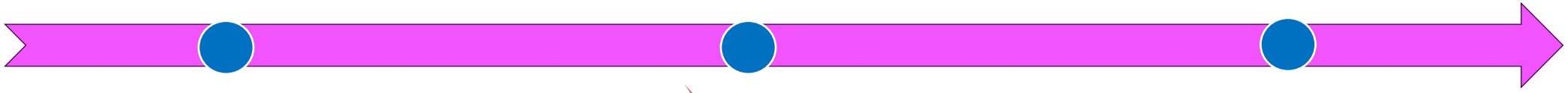
Software Engineering Approach



nanoxmap

- ✓ “Hello world”
- ✓ Feasibility
- ✓ Solved Synthesis & Routability problems

nXmap 3

- ✓ Scalability – Large matrix support
- ✓ Better memory handling
- ✓ Better Synthesis & Routability

Impulse

- ✓ Ease of use
- ✓ Interface rethink to be user friendly
- ✓ Better Synthesis & Routability
- ✓ Advanced tools & reporting

Achievements

- ✓ Knight Rider on NG-MEDIUM
- ✓ First deployment on end-users

- ✓ NG-ULTRA support
- ✓ Multiple design closures on NG-MEDIUM

- ✓ ULTRA300 support
- ✓ Big design closure on NG-ULTRA
- ✓ Over 100 end users

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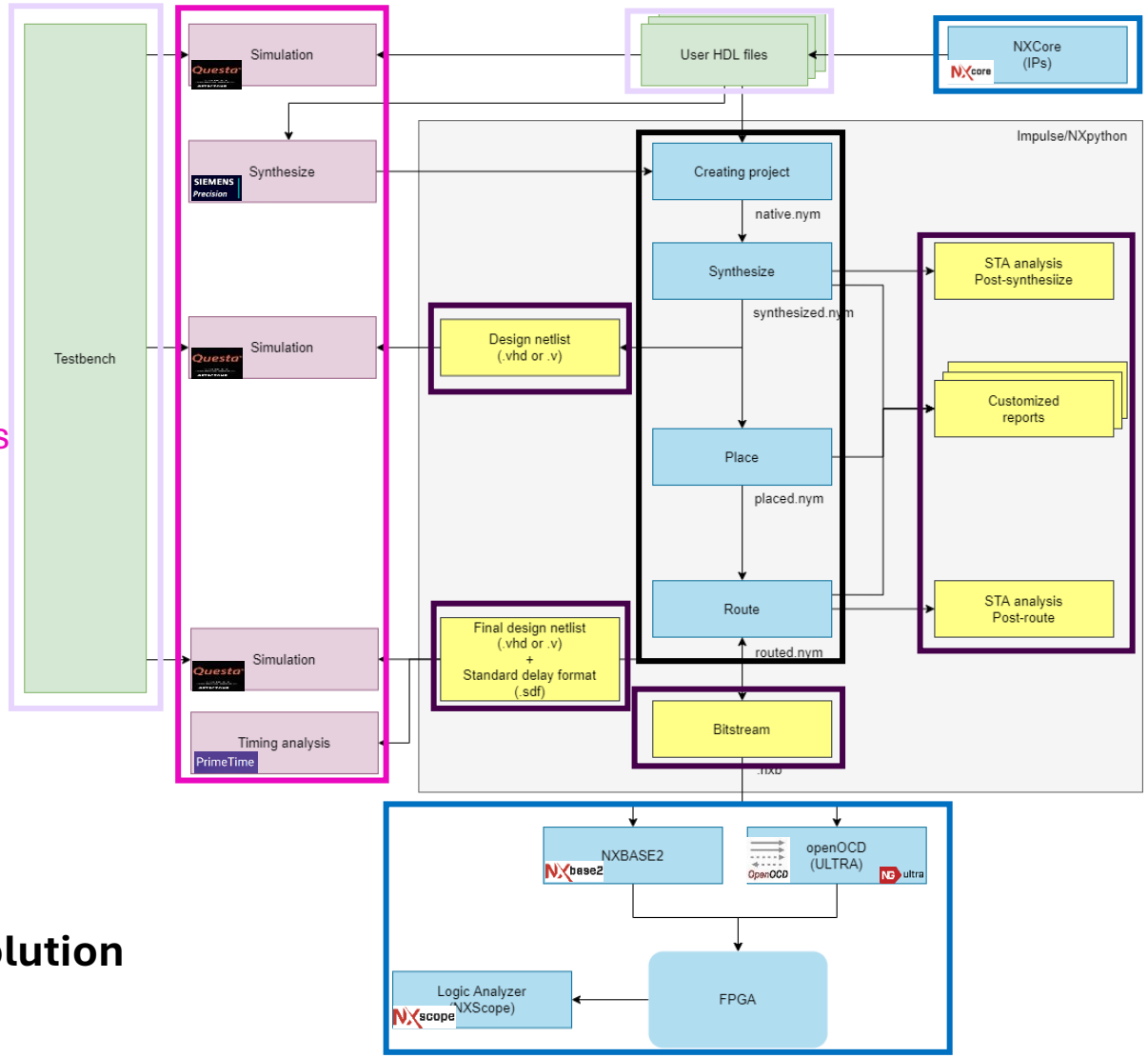
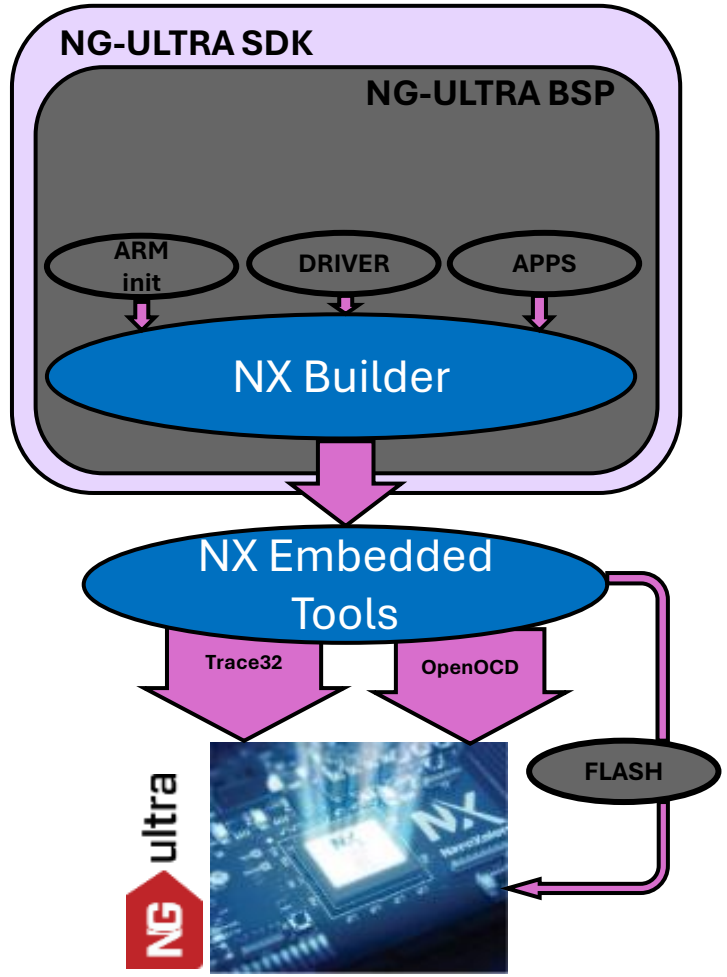
NX Design suite tools - Overview

User Resources
NX Tools
NX Output Files
Third-Party Tools





Complete solution

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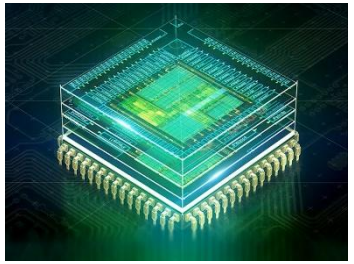
Our partners

Synthesis Tool

SIEMENS

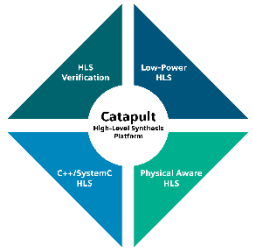
Siemens Precision HI-REL



High Level Synthesis

SIEMENS

Siemens Catapult



MathWorks®

HDL Coder

POLITECNICO MILANO 1863

Bambu

Debugging Tools

LAUTERBACH DEVELOPMENT TOOLS

TRACE32

OpenOCD

OpenOCD

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SOFT IP 25.1 (June 2025)

IP	Version
DMA	Release 25.1
Datamover MM2S	Release 25.1
Datamover S2MM	Release 25.1
Axi Scaler	Release 25.1
Axi Stream CDC/FIFO	Release 25.1
JESD TX	Release 25.1
FFT 8K	Release 25.1

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SOFT IP 25.3 (Dec 2025)

IP	Version
Controller DDR2	Release 25.3
Bridge APB to AXI4 lite	Release 25.3
JESD RX	Release 25.3
Spi shooter v3	Release 25.3
SPI stream	Release 25.3
JTAG to Stream	Release 25.3
AXI Stream Data FIFO	Release 25.3
AXI Stream data converter	Release 25.3
Esistream multi lane	Release 25.3
FFT 16K	Release 25.3

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Configuration memory

ISSI 128 mb

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Configuration memory

- NX has contracted ALTER TECHNOLOGY to select and upscreen a Non-Volatile Memory for configuration memory:
- IS25LP128 datasheet Rev.L8 - IS25LP128-JBLA3 - 8-pin SOIC 208mil
- 128mb
- TID > 30krads(Si), SEL immune & SEE cross-section
- Class 2 screening
- No export constraints
- Final report qualification report April 2025

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