

FPGA-based Time-to-digital Converter with steady-calibration through single-photon statistics for harsh environments

Andrea Stanco^{1,2,3,*}, Matías R. Bolaños Wagner¹, Daniele Vogrig¹,
Paolo Villaresi^{1,2,3}, and Giuseppe Vallone^{1,2,3}

¹ Dipartimento di Ingegneria dell'Informazione, Università degli Studi di Padova, 35131, Padova, Italy

² Padua Quantum Technologies Research Center, Università degli Studi di Padova, via Gradenigo 6B, IT-35131 Padova, Italy

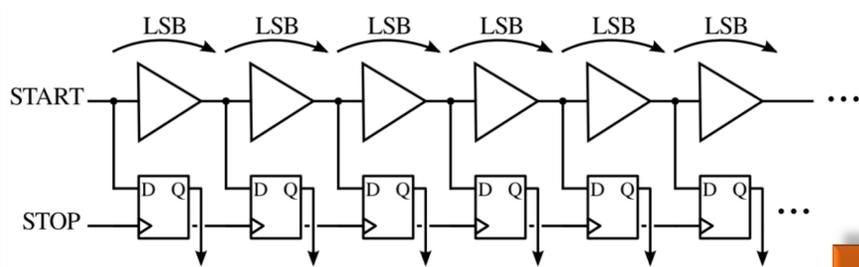
³ Istituto Nazionale di Fisica Nucleare (INFN) - sezione di Padova, Italy



SUMMARY

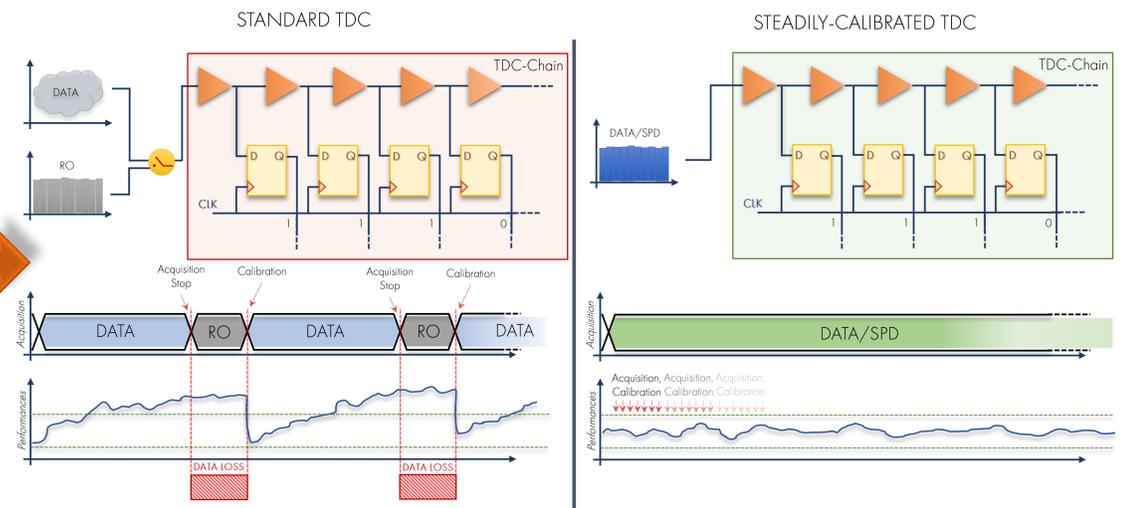
We present an FPGA-based TDC, called MARTY, that exploits the statistics of single-photon detection to provide the proper input distribution to guarantee bin calibrations during the signal acquisition without any TDC stop or data loss. TDCs usually integrate a ring-oscillator to provide the statistics for the calibration, which requires the data acquisition to be stop. Our configuration, called “steady calibration”, allows to combine the acquisition and the calibration. The advantage is not only the removal of data loss but also an improvement in the performances of the TDC (i.e., its jitter) as the calibration is carried out at every event. This application is particularly well-suited for Satellite Quantum Communications where single-photon detectors (SPDs) are part of a setup in a harsh environment. As a matter of fact, temperature has a direct effect on the jitter of tapped delay-line TDC. The system was implemented on a Zynq7020 and successfully tested between 5° and 85° [1]. It was also integrated in a Quantum Communication system.

TIME TAGGER TECHNOLOGY



1. Input signal propagates through a chain of delay elements
 2. Propagation through a single delay element takes (a small amount of) time [1]
 3. Stop signal activates flip-flops, capturing the current state of the delay line.
 4. A decoding stage is needed to transform the thermometer code into binary.
- This can be combined with a coarse clock counter on an FPGA to create an FPGA-based TDC. MARTY was implemented on a Zynq7020 and exploits the SoC versatility presented in [2].

STANDARD CALIBRATION AND THE «STEADY-CALIBRATION»

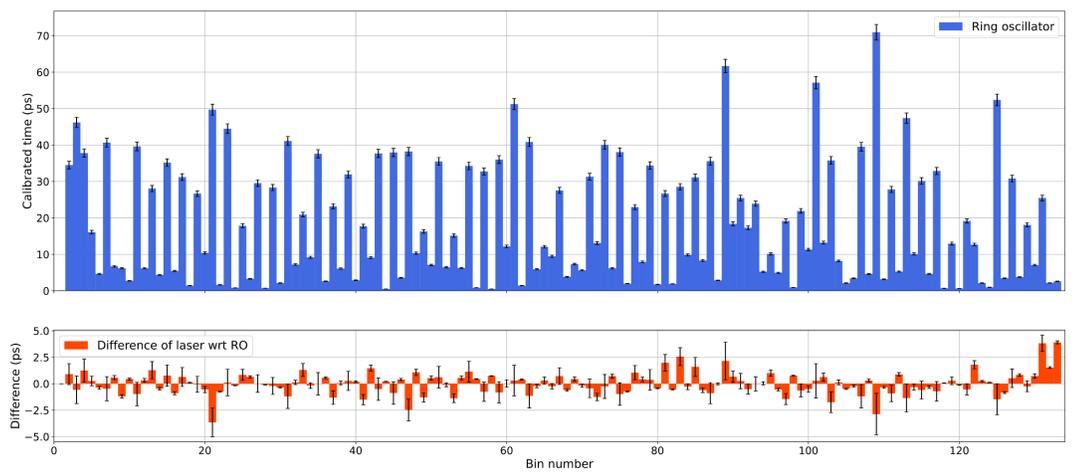


STANDARD CALIBRATION

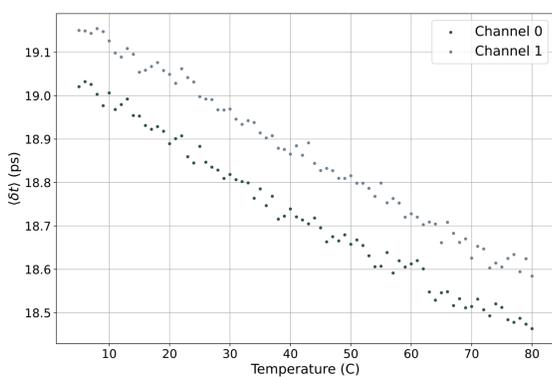
- A **uniformly distributed** signal is sent to the TDC (RO)
- The number of events detected in bin i is proportional to the **propagation time** for that bin $\delta t_i = \frac{w_i}{\sum_j w_j} \tau_{sample}$
- We can derive the **calibrated time** for bin i as $t_i^{(c)} = \frac{1}{2} \delta t_i + \sum_{i < j} \delta t_j$

STANDARD CALIBRATION

- We replace RO with a **single photon detector** detecting a **quantum source**
- Source and TDC's clocks are **not related**, thus satisfying uniformly distributed signal.
- Each new event gets added to the code density histogram, removing the first event from the list \rightarrow re-calculate $t_i^{(c)}$.

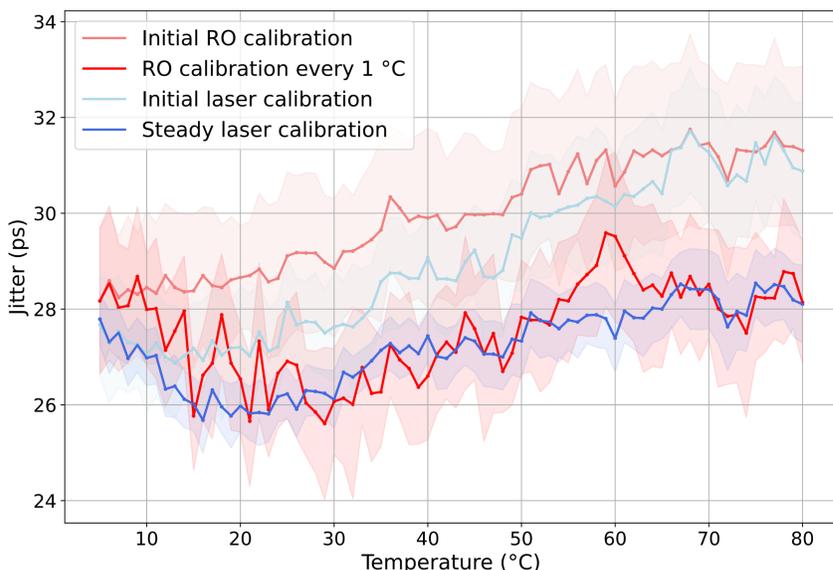


TEMPERATURE TEST



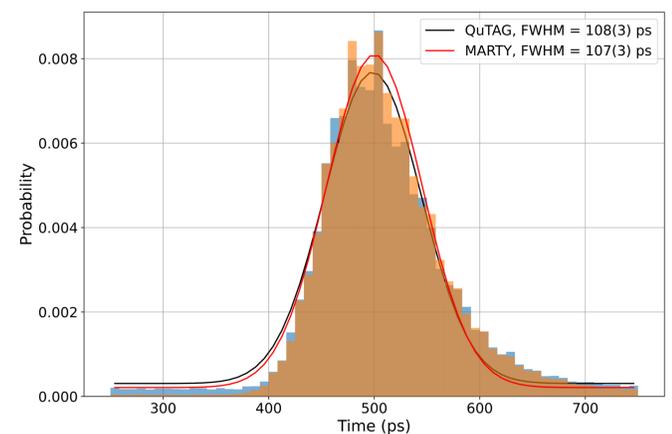
To test continuous calibration, the data was calibrated

1. Using the calibration curve with the RO at 5°C (light orange).
 2. Using the first time-tag registered with the single photon detector at 5°C (light blue).
 3. Using the calibration curve for each temperature (red).
 4. Steady calibration (blue).
- System was tested under temperature changes
A combination of a Peltier cell placed on top of the chip, and a RAL 9006 climatic chamber by Angelatoni Test Technologies were used to control the temperature from 5°C to 80°C



QUANTUM KEY DISTRIBUTION TEST

- The device was also tested in a real-application scenario in a real Quantum Key Distribution setup [3].
- Tested sending a standard 'HVDD' sequence.
- Compared with a commercial Time tagger device (QuTAG by QuTools), using 4 PMD-IR detectors by MPD. With a non-optimized polarization encoded QKD source, both time-taggers obtained an average of 2.2% QBER (10 minute measurement).



REFERENCES

- [1] M. R. Bolaños W. et al., A time-to-digital converter with steady calibration through single-photon detection, pre-print doi.org/10.48550/arXiv.2406.01293
- [2] A. Stanco et al., Versatile and concurrent FPGA-based architecture for practical quantum communication systems, IEEE Transactions on Quantum Engineering, vol. 3, pp. 1-8, Art no. 6000108 (2022).
- [3] F. Berra, et al., Modular source for near-infrared quantum communication, EPJ Quantum Technology, vol. 10.

