RÉPUBLIQUE FRANÇAISE
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cnes
CENTRE NATIONAL D'ÉTUDES SPATIALES

IP DEVELOPMENTS

SEFUW – ESTEC

2025/03/25-27

SOMMAIRE

01 CNES IP strategy

02 LGMi roadmap

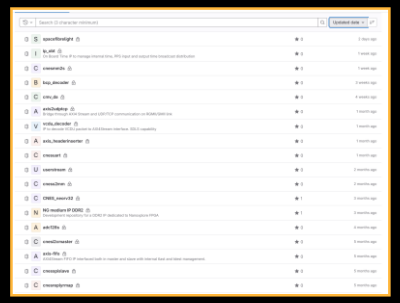
03 DDR2 controller

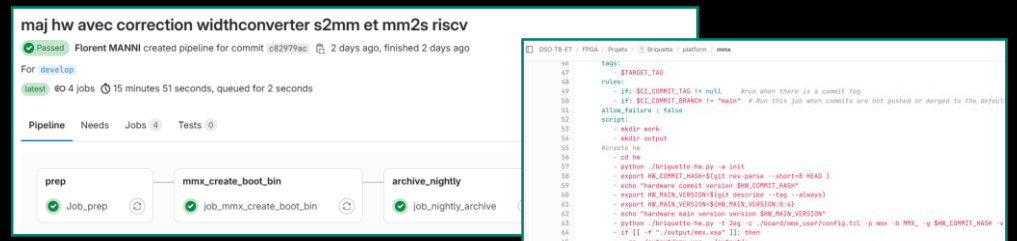
01

CNES IP DEVELOPMENT STRATEGY

IP MANAGEMENT WORKFLOW

IP DEVELOPMENT STRATEGY



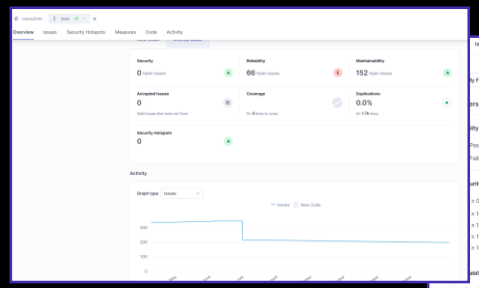


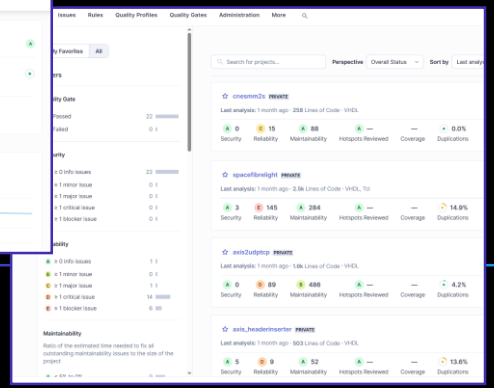
Version control
(GIT + Gitlab)

Automation V1
(Python + Gitlab-ci)

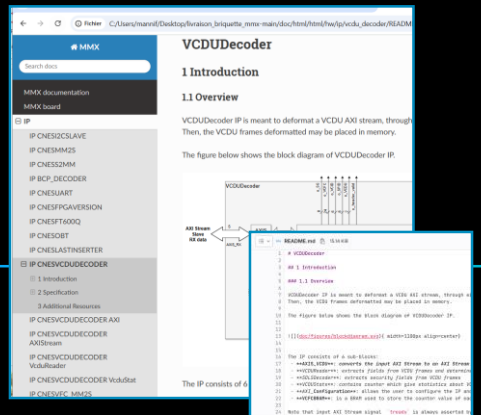
HW in the loop
(docker + HW boards)

Code quality
(Sonarqube + Linty-service bugfinder)

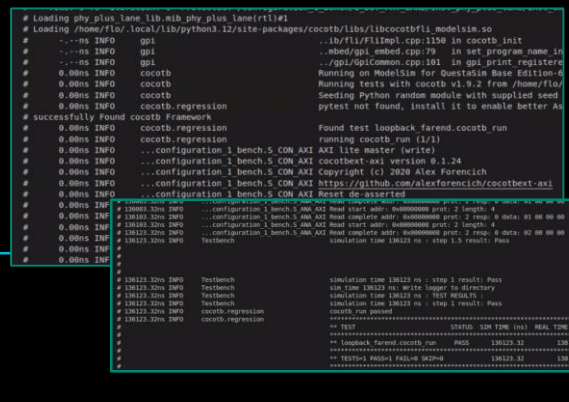




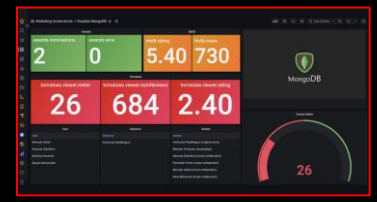
Documentation
(Markdown + Sphinx)



Tests
(Cocotb)



Automation V2
(Dashboard Graphana)



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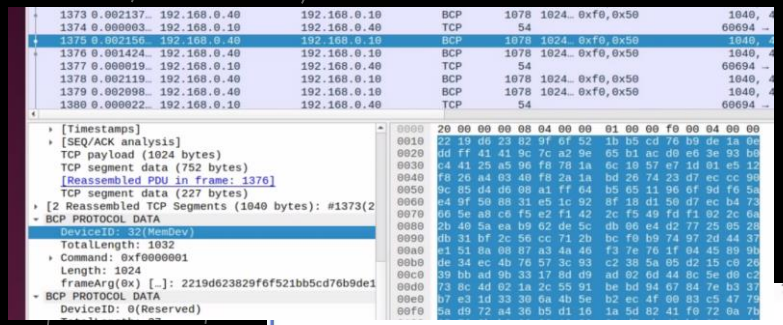
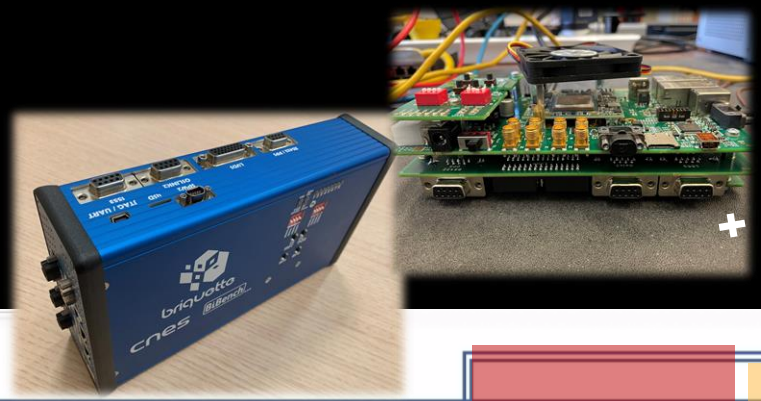
IP USE CASE (GROUND APPLICATION): BRIQUETTE





+ SW (drivers +BSP)

PC

Ethernet TM/TC

µP

Spacewire

Spacewire

RISCV + Spacewire

RISCV + SPI

OBC OR PAYLOAD

Xilinx FIFO

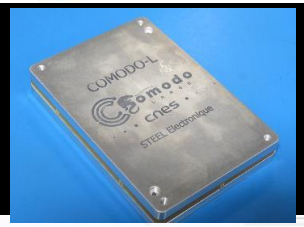
Xilinx Interconnect

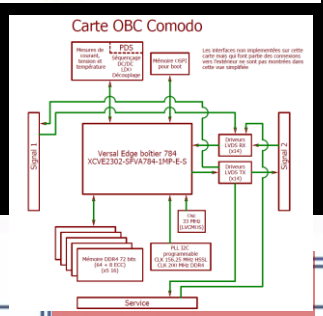
AXIfull AXIstream

Data flux router

IP USE CASE (FLIGHT APPLICATION): COMODO

Comodo LARGE | Comodo ULTRA | Comodo VERSAL





+ SW (XNG + kosmos)

KOSMOS Flight software

TM/TC

TM/TC

NanoXplore
ARM µP
RiscV

FIFO

Interconnect

Spacewire

SPI,I2C...

Spacewire
RiscV

Spacefibre

PAYLOAD

NX HSSL

FPGA Reference Design

SPACEFIBRELIGHT IP

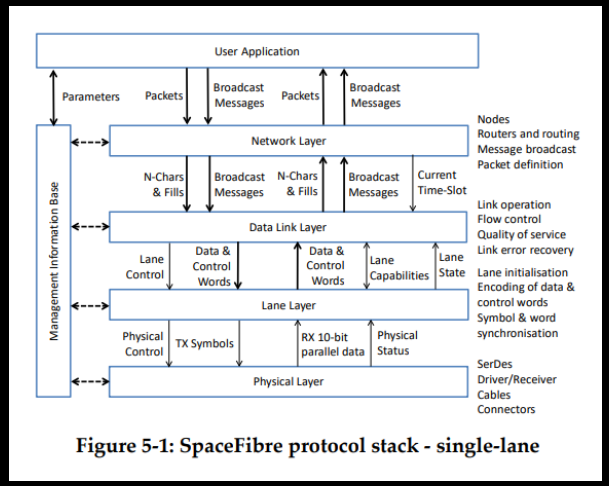
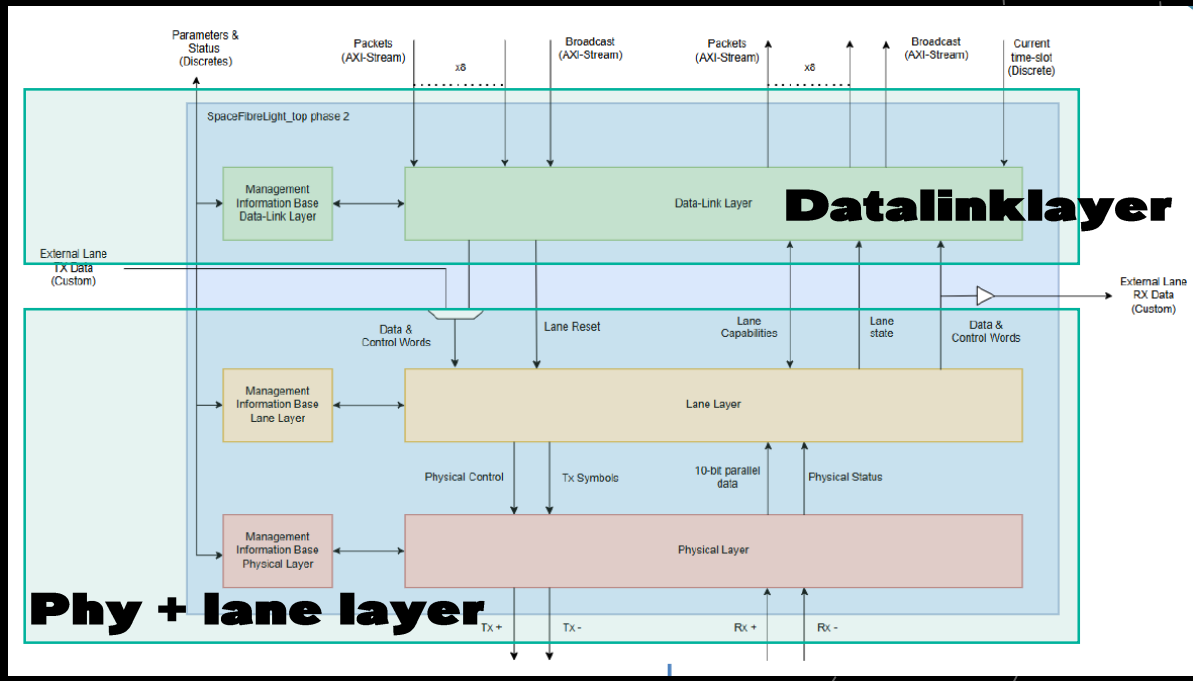


Figure 5-1: SpaceFibre protocol stack - single-lane

Rationale:

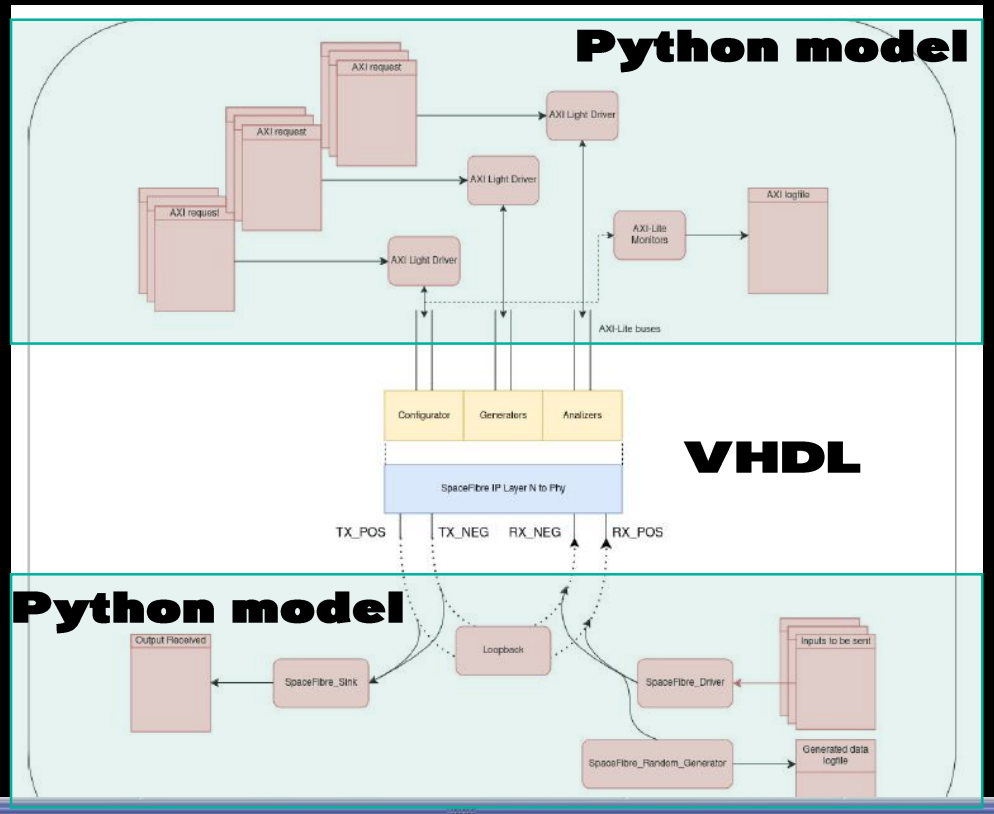
- Provide a Spacewire light open source IP for spacefibre standard
- Be easy to understand and easy to maintain
- Compatible with the standard but not fully compliant to it:
  - No QoS (round robin access to virtual channels and broadcast)
  - No multilane support
  - No scramling
  - No error recovery buffer (link reset strategy)
  - No routing (node to node mode only)
- Compatible Xilinx Versal and NanoXplore Ngultra / Ultra300
- Opensource

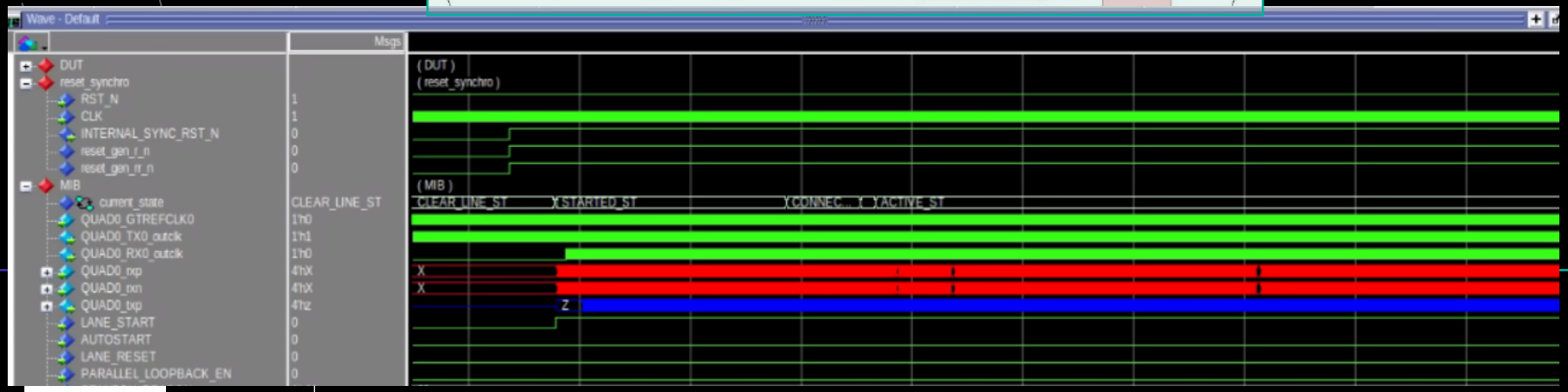


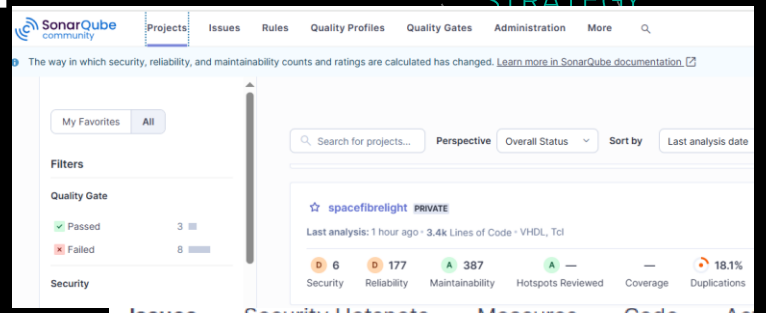
Developped by Advans – Elsys Design under CNES R&D contract

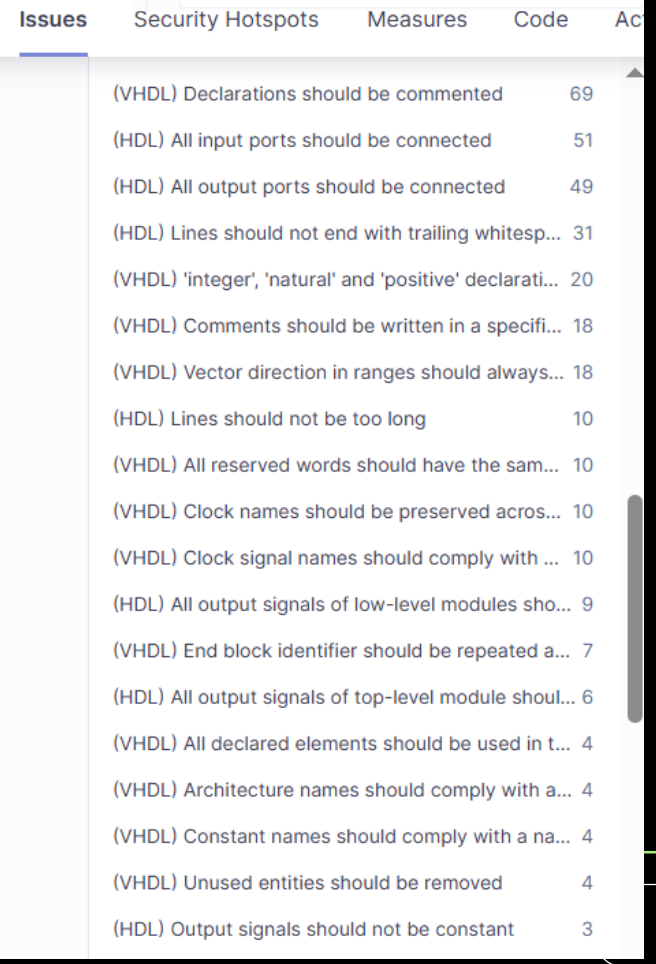
SPACEFIBRELIGHT IP VERIFICATION

Cocotb testbench infrastrucuture









SEFUW 2025

A Roadmap for NanoXplore Platforms

LGM GROUP INTRODUCTION

MANAGEMENT AND ENGINEERING OF COMPLEX PROJECTS AND SUPPORT

- MAINTENANCE AND SUPPORT ENGINEERING
- SYSTEMS ENGINEERING & RAMST
- ORGANISATIONS AND PROGRAM PERFORMANCE
- DIGITALISATION, DATA & INFORMATION TECHNOLOGY

ELECTRONIC ENGINEERING AND PRODUCTION

- **CRITICAL ELECTRONICS** EQUIPMENT
- **RADIOFREQUENCY** AND **MICROWAVES**
- **FPGA** AND **SOFTWARE** SOLUTIONS
- MICROELECTRONICS
- EMBEDDED NETWORKS
- TEST BENCHES

LGM : A GROWING PLAYER IN THE SPACE INDUSTRY

2000
ILS studies for ground station

2003
ILS Studies for M51

2008
1st ESA contract

2009
LGM ISS ground segment A5

2016
EGSE :for SODERN IVV for TAS Belgium

2017
Opening for LGM In Guyana
Start R&T in electronics

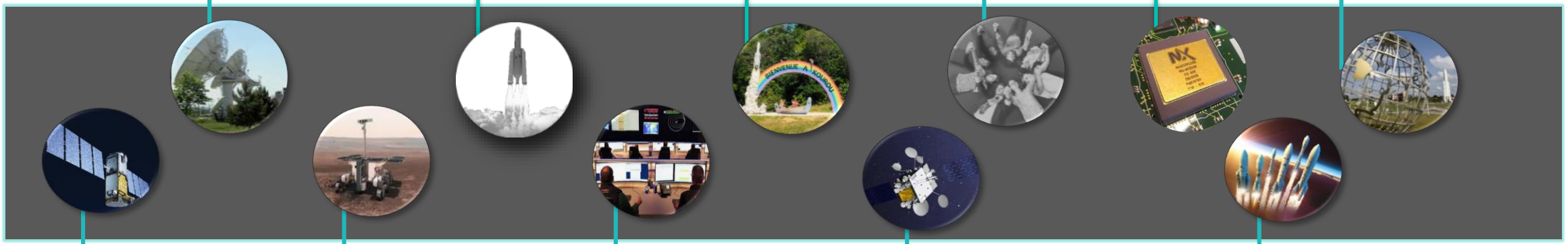
2018
LGM is collaborating with AIRBUS and THALES to develop the system support for SYRACUSE 4 (S3000L / S1000D)

2019
International referencing for ILS and RAMS

2020
Start R&T for NX FPGA

2021
RF test benches for THALES and AD&S

2022
Digitalisation of CSG



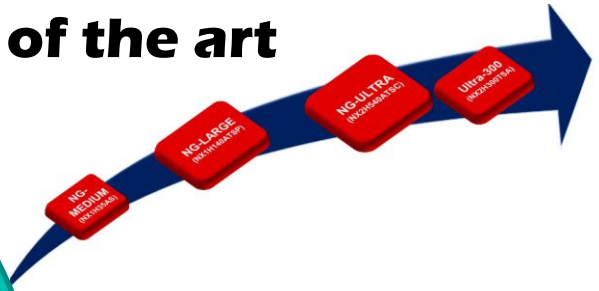
R&T STRATEGY ON NANOXPLORE SOLUTIONS

R&T roadmap

Invest on HW platforms

ECOSYSTEM
of
EXPERTISES & BUILDING BLOCKS to
HELP YOU
to **adopt NanoXplore**
solutions and **facilitate** their use

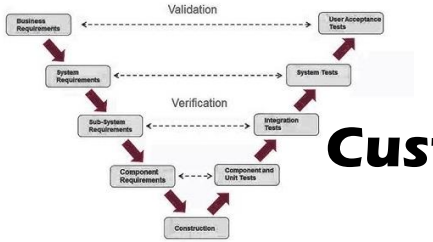
State of the art



Train more FPGA/SoC specialists to NX

Reinforce partnerships

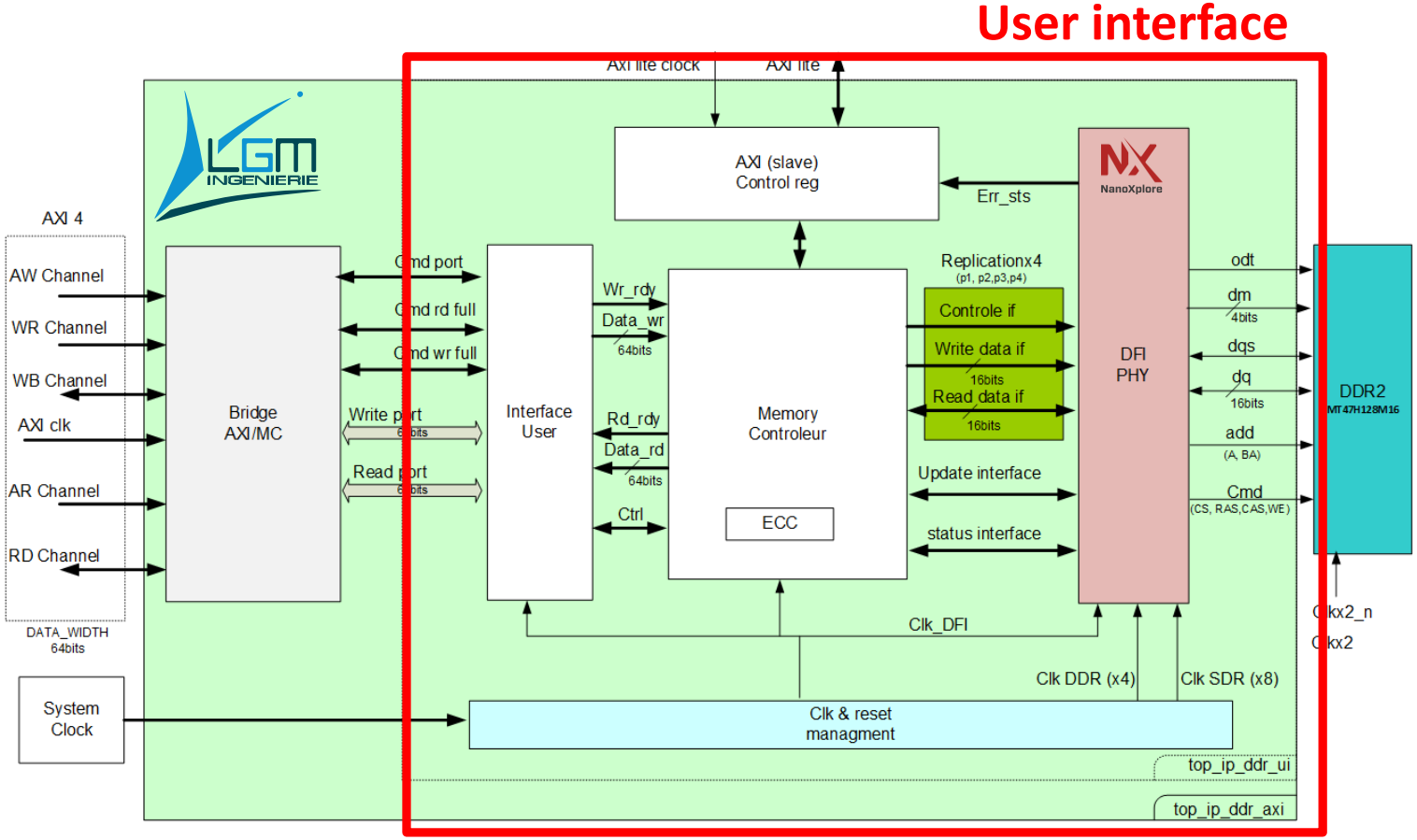
NanoXplore cnes

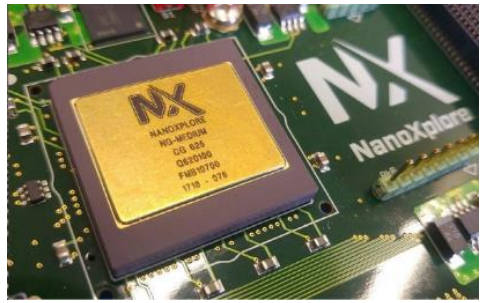


Custom solutions

DDR2 controller IP core

DDR2 IP CORE ALREADY AVAILABLE





- **Available for free** on NanoXplore Design Suite for **NG-MEDIUM**
- Stand alone "**User interface**" for light implementation => **available on request**

DDR2 IP CORE MAIN CHARACTERISTICS

GENERIC & ADAPTATIVE

- **AXI-4** interface for data path
- **AXI-Lite** interface for command and control
- **SECDED** with a 32/39 ECC implementation
- Generate **Error Correction statistics**
- Implements **JEDEC** parameters to support all standard memory chip
- **MR and EMR auto refresh** capabilities
- **Up to 64 bits** configuration
- **4 rank** support / **8 bank** support
- Supports **CAS** Latency between **2 and 6**
- Supports **Additive Latency** between **0 and 4**
- Total Write latency up to 8 (CAL+AL)

- **Compliant to** ECSS-Q-ST-60-02C adapted by CNES
- Fully tested on **Micron DDR2** **MT47H128M16RT**
- Fully simulated on **ISSI DDR2** **IS46DR16128C**
- Fully **automatized tests** (physical and simulation)
- **More than 50 tests scenarios**
- **UVVM methodology including OSVVM** library for **random** generation
- **100% code coverage** on branches and statements
- Tested at **250 MT/s**

DDR2 controller IP core

«SPACE READY»VERSION NOW AVAILABLE

Write back

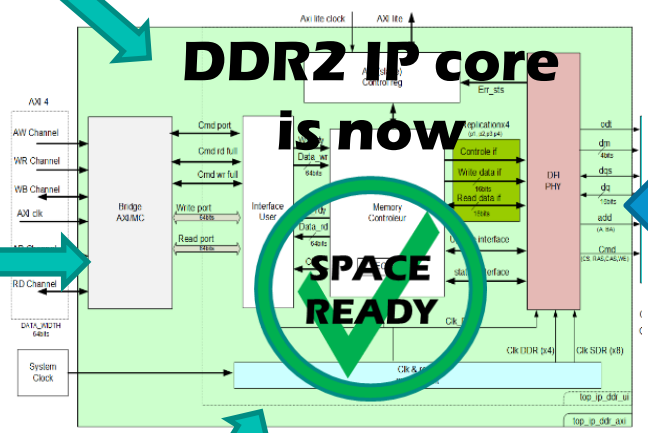
Performs an automatic write command when a read error is detected

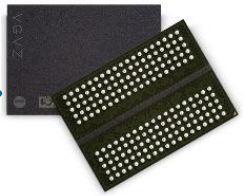
Scrubbing

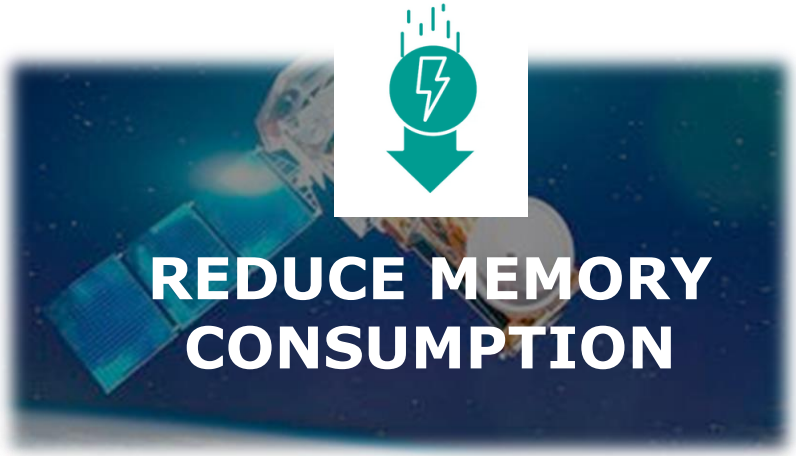
Performs automatic read and integrity checks at programmable intervals

Power-down

Reduce the static power **from 30%** compare to standby mode

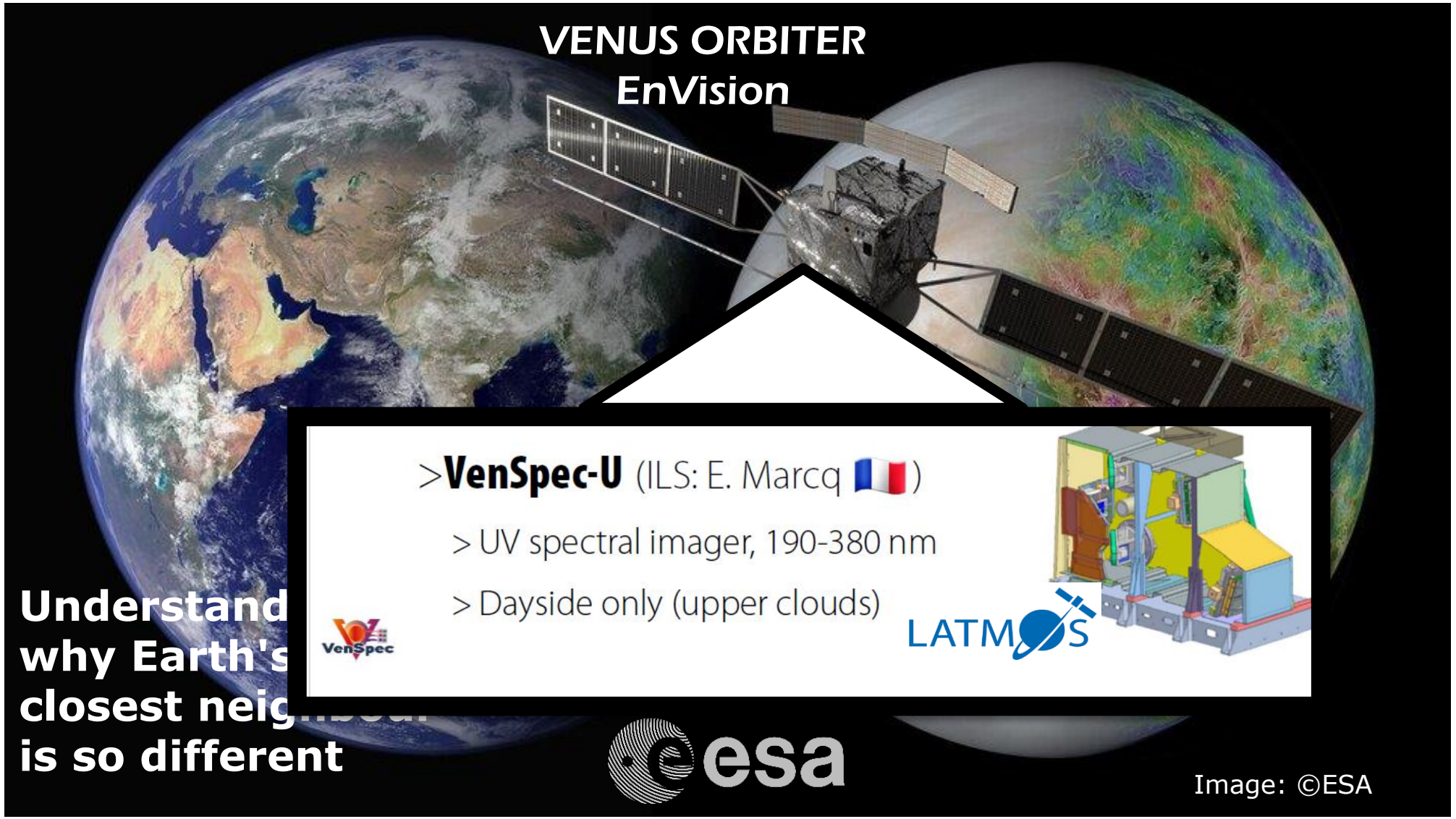




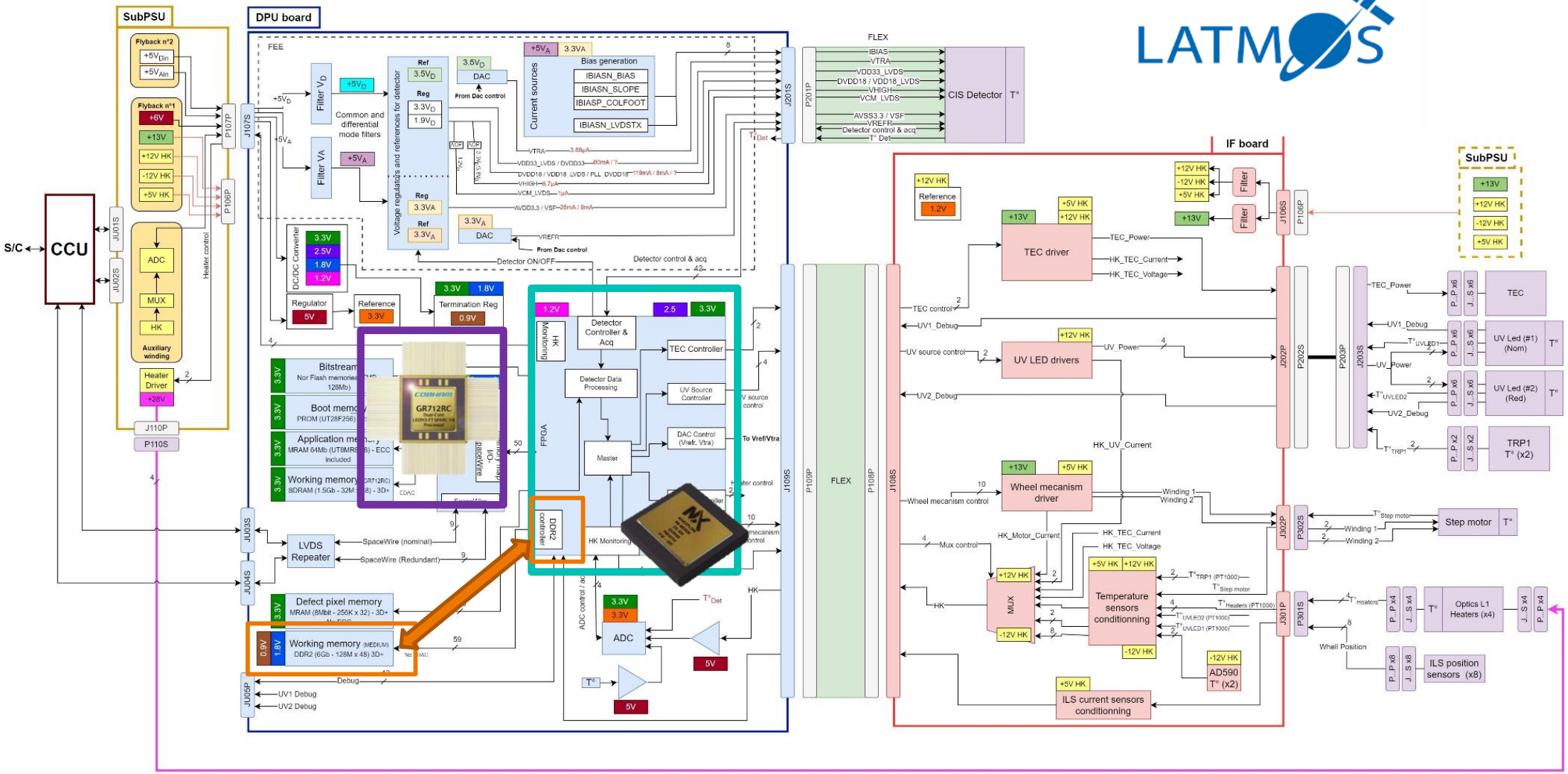


« *Use case* »
DDR2 controller IP core on VENUS EnVision Orbiter

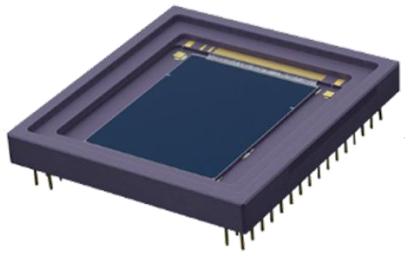
DDR2 CONTROLLER IP CORE : FLYING TO VENUS !



LATMOS DDR2 USE CASE



LATMOS DDR2 USE CASE



Teledyne Detector

Pixels

Data reception and synchronisation

Real-time traitment (bining, stacking, pixels deviant)

DDR2 Controller

DDR2 memory pictures storage

Post - traitment

Datas

NanoXplore NG-Medium

LGMI Roadmap to NanoXplore solutions

ROADMAP : IP & CUSTOM DESIGN

DDR2 Controller IP
Space-ready version
(NG-MEDIUM)

DDR2 Controller IP
(NG-MEDIUM)

DDR3 Controller IP
(ULTRA 300)

JESD204B & ESISTREAM
implementation
(NG-ULTRA/300)

2024 **2025** **2026** **2027**

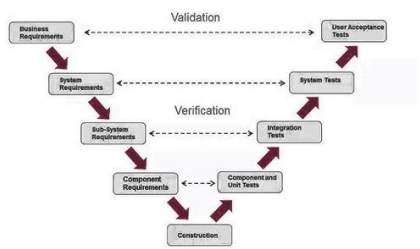
AXI interfaces IPs

DDR3 Controller IP
(NG-ULTRA)

JESD204B & ESISTREAM
evaluation
(NG-ULTRA/300)

Very high speed NVM I/F
& RF algorithm IP

Custom design

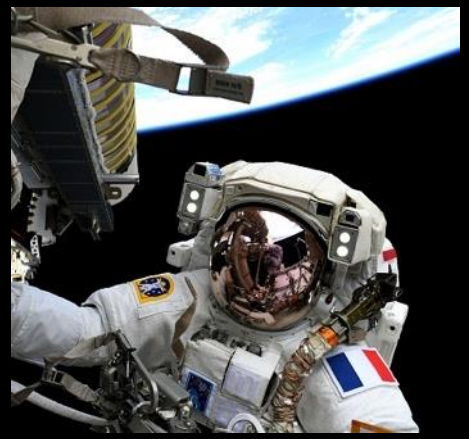


JENSEN HUANG

Nvidia Co-founder and CEO

OPEN COLLABORATION AND PARTNERSHIP ARE THE KEYS TO DRIVING PROGRESS AND INNOVATION

THANK YOU!







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