SEFUW: SpacE FPGA Users Workshop, 6th Edition

Wednesday 26 March 2025

Verification Flow - Einstein (16:00 - 17:15)

time	[id] title	presenter
16:00	[9] Get the right FPGA quality through efficient verification and Requirements Tracking	TALLAKSEN, Espen
16:25	[30] Towards a Formal Verification Methodology for Digital Electronics in the space sector	Prof. GUZMÁN-MIRANDA, Hipólito
16:50	[21] Why Your Team Should be using VHDL + OSVVM for Verification	LEWIS, Jim