



# Current 3U ADHA Module developments at EIDEL

ADCSS 2024 - ESTEC

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# ■ ABOUT EIDEL

Founded 1966 by Erik Olsson in his garage in Eidsvoll, Norway

2024: Employees: 46 (13% PhD).

Turnover 2023: 7.2 MEUR, result before tax 480 kEUR.

Offices at Eidsvoll and Lillestrøm, Norway

## TYPICAL CUSTOMER SCENARIOS & NEEDS

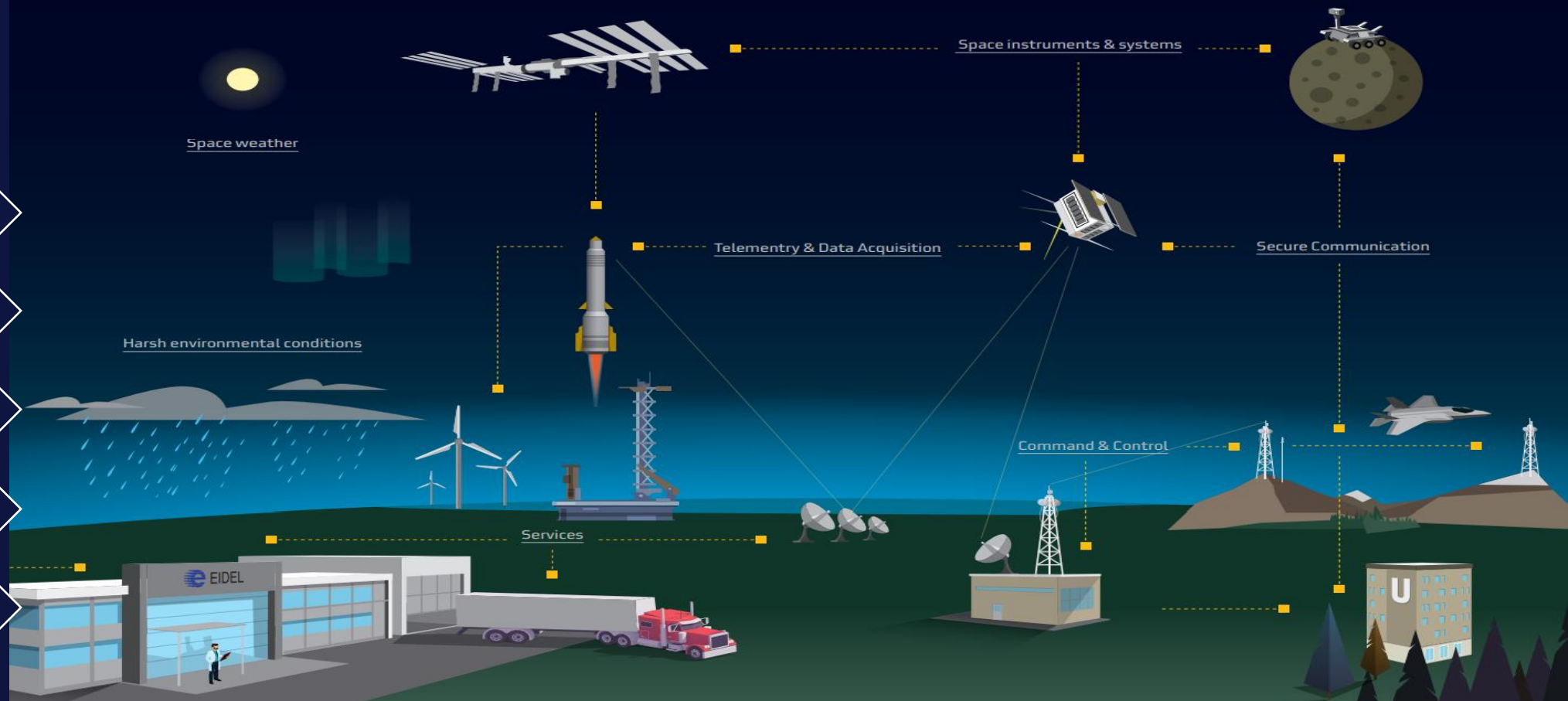
REMOTE LOCATIONS

UNMANNED ASSETS

HARSH ENVIRONMENTS

HIGH PRECISION MEASUREMENTS

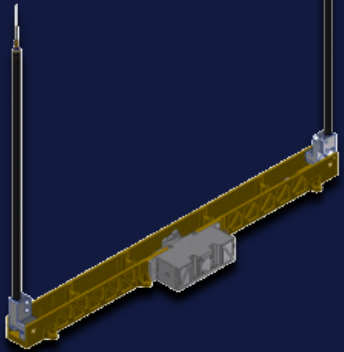
HIGH SECURITY NEEDS



# ■ PRODUCTS, SYSTEMS & SERVICES

## SPACE INSTRUMENTS PAYLOADS & SUB-SYSTEMS

**m-NLP**  
multi-Needle  
Langmuir Probe

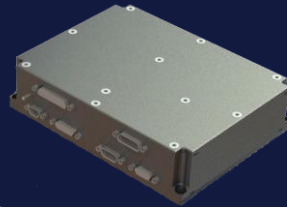


**ERIU**  
EIDEL Remote  
Interface Unit

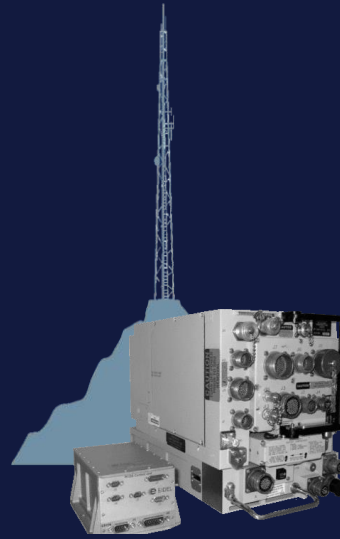


## SECURE COMMUNICATION

**SSL**  
Secure Satellite Link

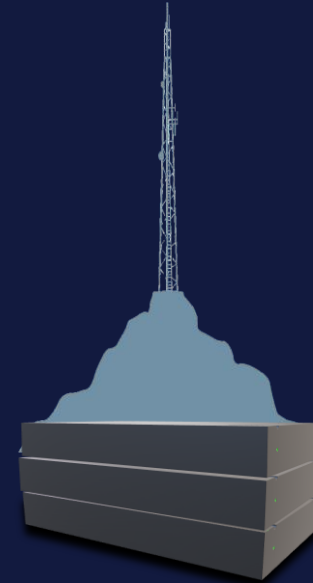


**RCDS®**  
Remote Crypto  
Distribution System



## COMMAND & CONTROL

**RCS**  
Radio Control System



## TELEMETRY & DATA ACQUISITION

**EDDAS**  
EIDEL Distributed  
Data Acquisition System



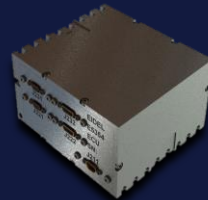
**MSS**  
Miniaturized Sun Sensor



**USLP**  
Unified Space Link  
Protocol  
Encoder/Decoder



**SDL**  
Secure Data Link



## ■ ADHA DEVELOPMENT GOALS (PRELIMINARY – SOW'S IN PREPARATION)

### EIDEL 3U-ADHA PCM (SBC)

#### Payload Controller Module

Continuation of our activity under ESA Contract No.: 4000128421/19/NL/GLC – CCSDS USLP encoder/decoder development

Current Technical Officer: Marco Rovatti

#### Activity goal:

EM version of the EIDEL 3U-ADHA PCM board (which will be a baseline processing module utilized as other functions as well. E.g. OBC, RIU-Controller, PICU-Controller)

Module will be made ready to interface directly with EIDEL 3U-ADHA PQC Security Module

### EIDEL 3U-ADHA PICU

#### Payload Interface Control Unit

Builds upon the EIDEL Payload Control Unit that supports the multi-Needle Langmuir Probe instrument that operates on the Bartolomeo platform on the ISS

Appointed Technical Officer: Alberto Valverde

#### Activity goal:

EM version of the 3U-ADHA PICU Interface Module, and full requirement set (to SRR) for all envisaged ADHA PICU modules (see separate slides)

## ■ ADHA DEVELOPMENT GOALS (PRELIMINARY – SOW'S IN PREPARATION)

Design scope for EIDEL ADHA modules:

Size: Only 3U-ADHA is currently considered

Lifetime: Minimum 5 years in LEO

Fully compliant with Class Beta (prev. Class III) and/or (depending on mission target) Class IV requirements

- Selection of key components that are available both as COTS and RT
- Screened COTS for non-critical applications for Class IV
- RT components for critical functional for both Class III and IV

# CCSDS USLP PROJECT OVERVIEW

ESA Contract No.: 4000128421/19/NL/GLC

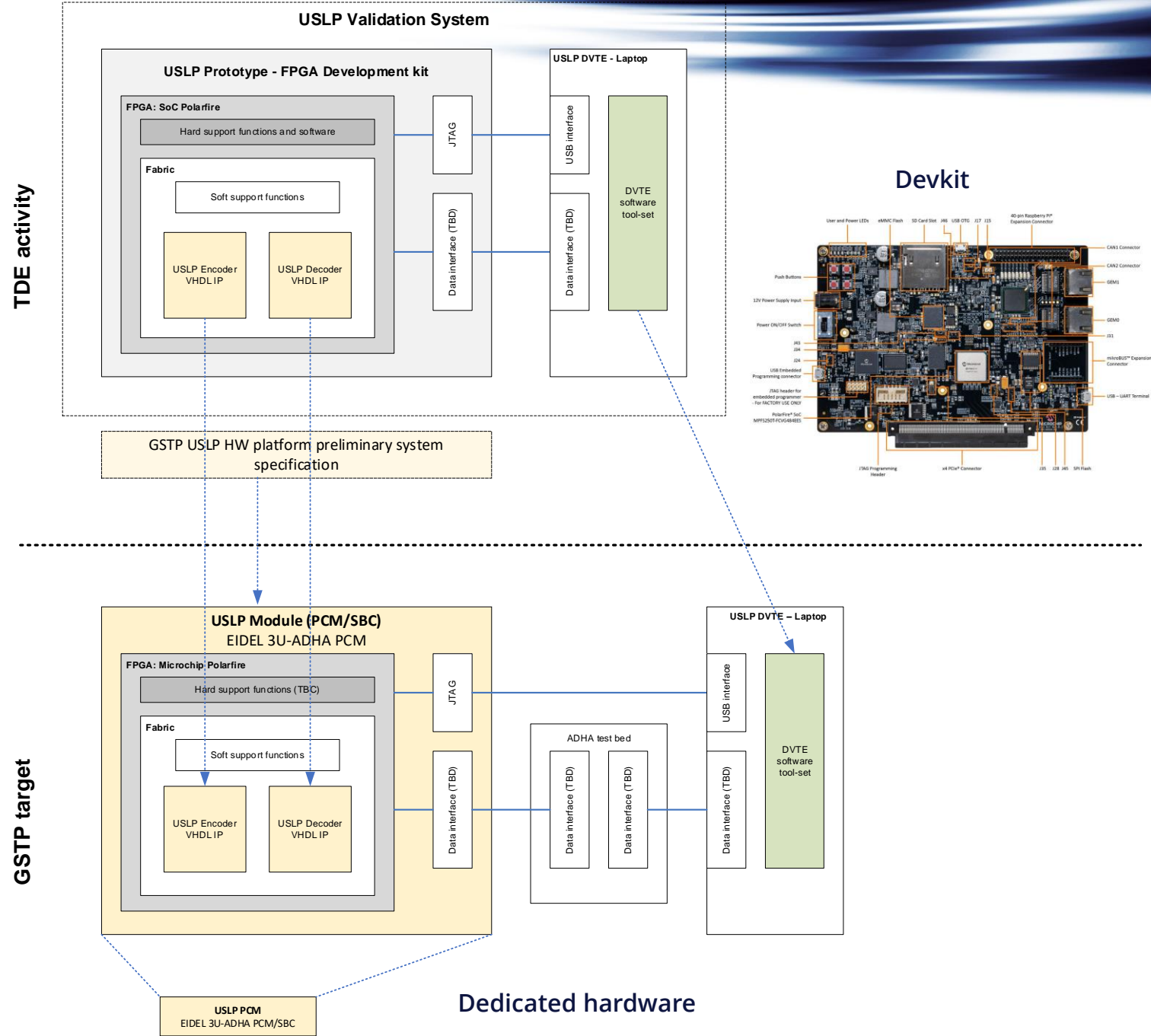
December 2019 – October 2024

## USLP Module (GSTP)

- USLP Module
  - USLP Encoder VHDL IP
  - USLP Decoder VHDL IP
- USLP Module Test bed
  - Test equipment
  - Updated Development, Verification and Test Environment (DVTE)

## USLP Validation System

- USLP Prototype
- USLP Development, Verification and Test Environment (DVTE)

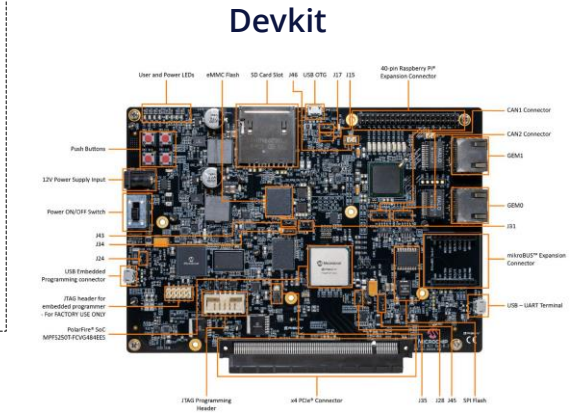
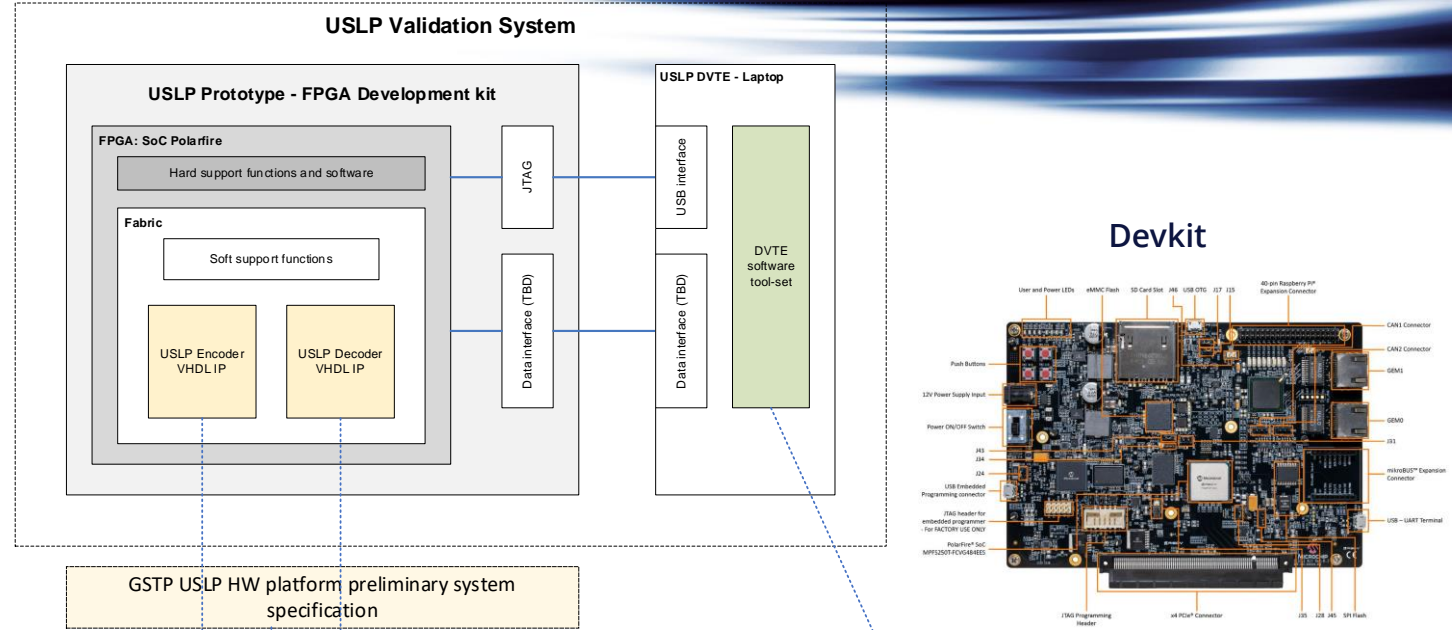


# CCSDS USLP PROJECT OVERVIEW

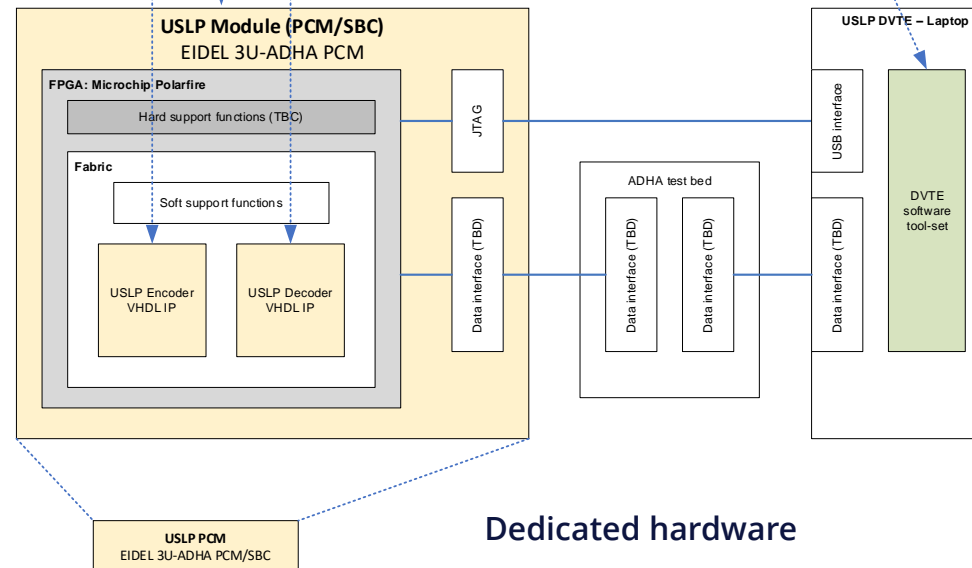
## Why use USLP and the EIDEL-3U-ADHA-PCM?

- Potential for higher bandwidth on TM downlink
- Solves the current issue of available SCIDs
- Larger frame sizes, variable lengths, suitable for satellite to satellite, satellite to moon-base etc, in addition to satellite to ground.
- Integrated commercial PQC-protection (in development by EIDEL), and facilitated for future dedicated EIDEL-ADHA-SM (Security Module) for classified systems and payloads

TDE activity



GSTP target



## ■ CCSDS USLP ENCODER/DECODER PERFORMANCE

Performance numbers on Microchip Polarfire FPGA (MPFS250T - FCVG484EES). FPGA family selected due to availability of RT Polarfire for higher class missions.

	Width	Format	Bits/s	Frames/s	Latency
<b>USLP Encoder IP</b> • 100 MHz system clock	32-bit	7-byte MAPP. One packet per Transfer Frame	<b>0.521 Gbps</b>	<b>3.83 Mfps</b>	<b>440 ns</b>
	32-bit	65526-byte MAPP. One packet per Transfer Frame	<b>3.196 Gbps</b>	<b>6.10 kfps</b>	<b>164 us</b>

	Width	Format	Mbps	Indications/s	Latency
<b>USLP Decoder IP</b> • 100 MHz system clock	32-bit	7-byte MAPP. One packet per Transfer Frame	<b>0.926 Gbps</b>	<b>8.90 Mips</b>	<b>890 ns</b>
	32-bit	65526-byte MAPP. One packet per Transfer Frame	<b>3.198 Gbps</b>	<b>6.10 kips</b>	<b>492 us</b>

32-bit bus width fully verified. 128-bit bus width will increase the bandwidth to more than 10 Gbps.



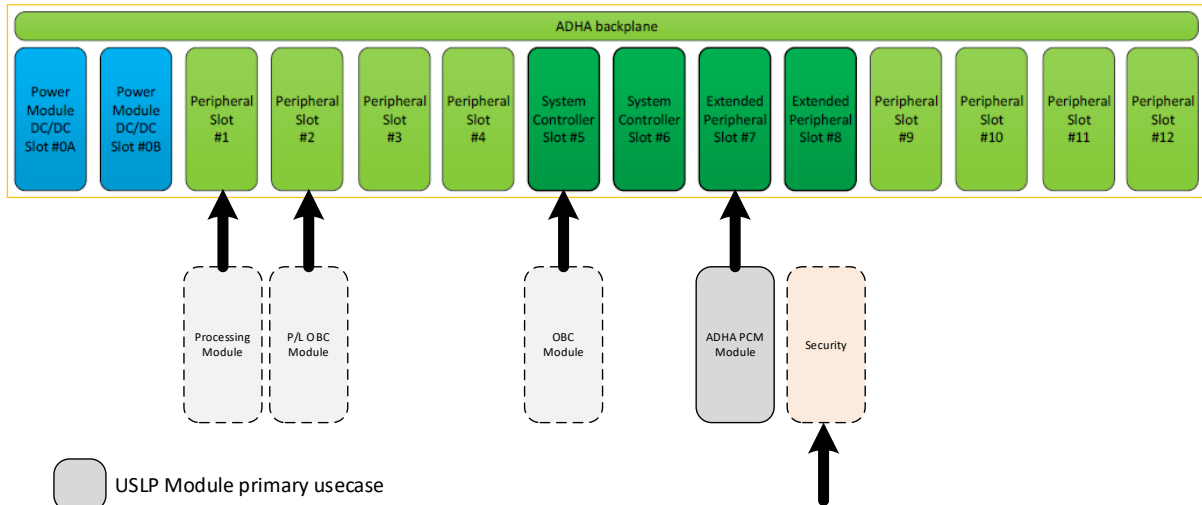
# NEW MULTI-PURPOSE MODULE

## Multi-purpose EIDEL 3U-ADHA Processing Module / PCM / SBC

- PCM (with USLP IPs and optionally SDLS)
- PL Interface Controller/POBC (with USLP IP and optionally SDLS for TM-downlink)
- PF OBC (with USLP IPs and optionally SDLS, module to be further analyzed)
- PF RIU Controller

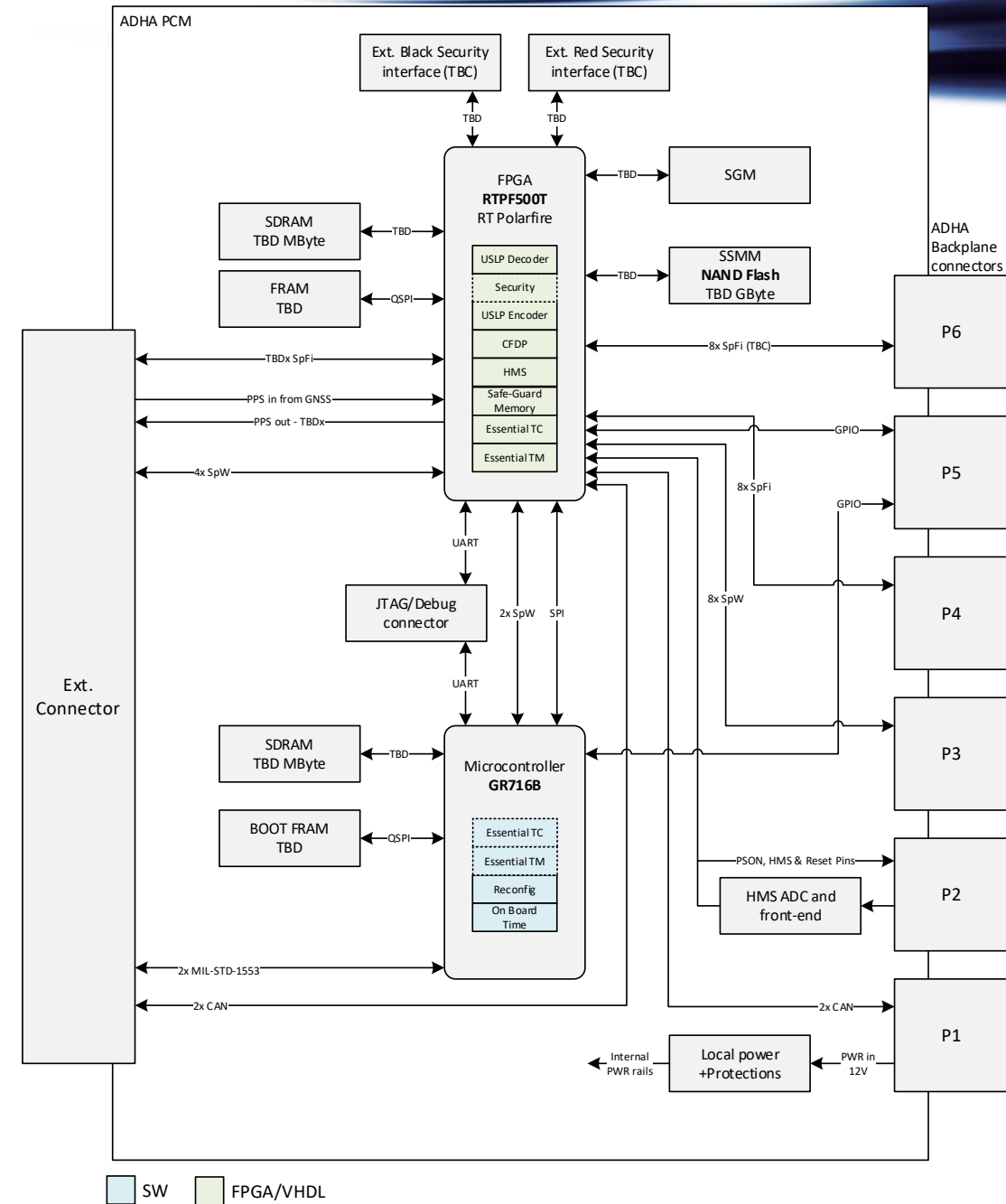
## And EIDEL-ADHA-3U Test bench

- Using USLP DVTE



- USLP Module primary usecase
- USLP Module hardware optional future usecases
- Future Security Module

**Security module builds upon close to 20 years of heritage in designing and building rugged crypto modules for space and airborne applications**



# EIDEL 3U-ADHA PAYLOAD ICU

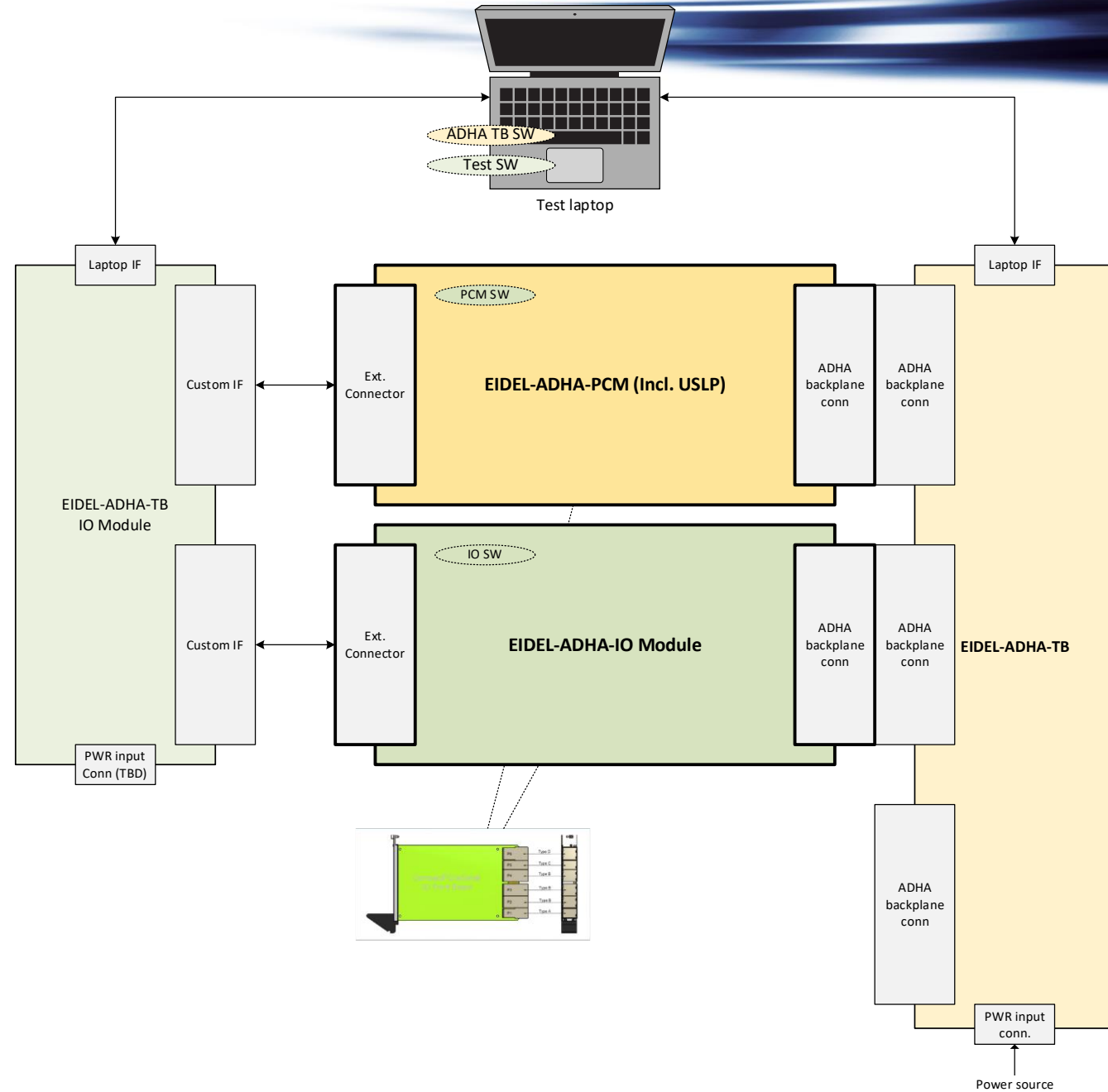
## EIDEL ADHA PICU (Payload Interface Control Unit)

EM version of the ADHA PICU Interface Module will be developed, and full requirement set (to SRR) for all envisaged ADHA PICU modules

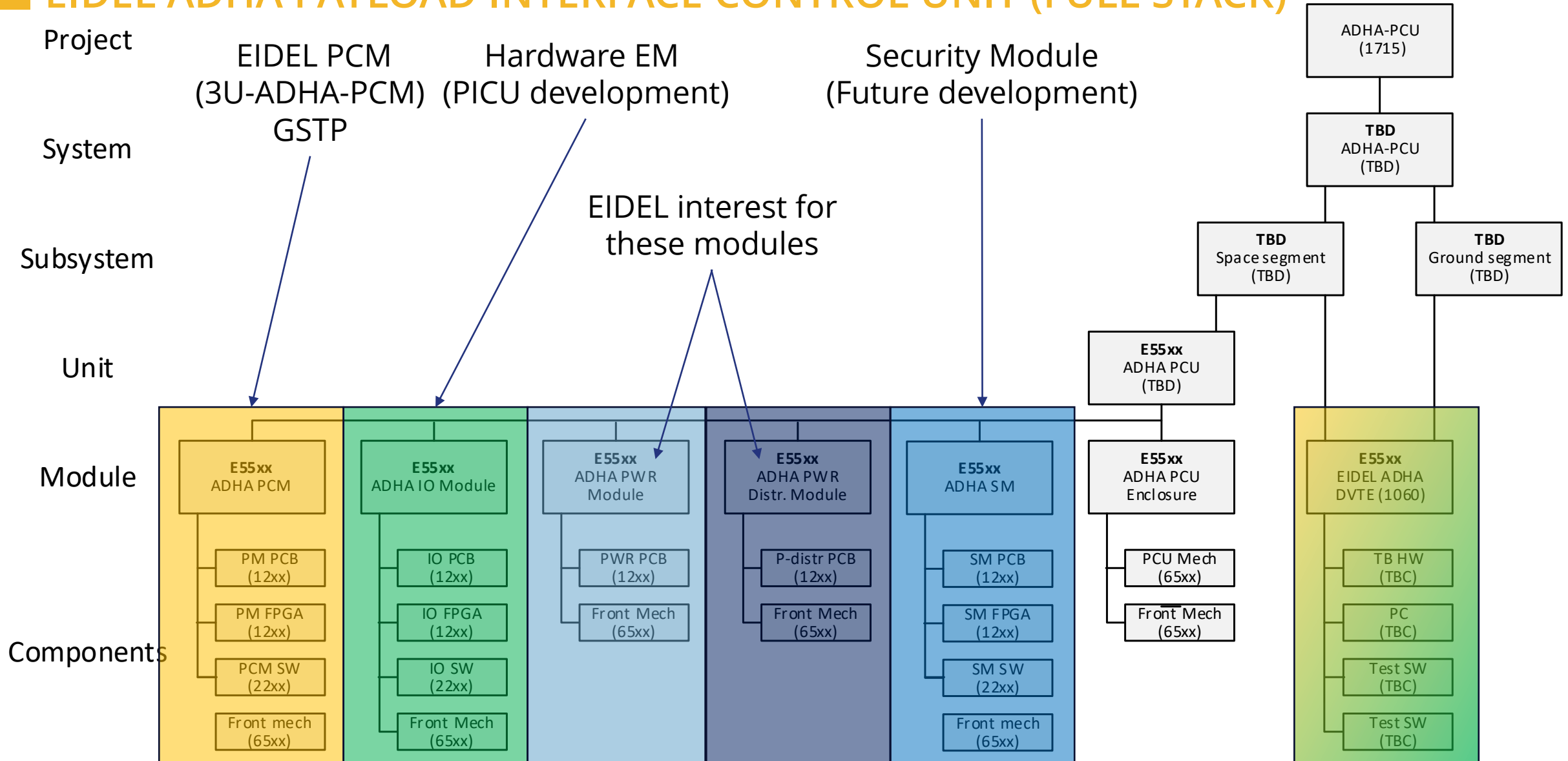
EIDEL-ADHA-PCM Module will be used in conjunction with the EIDEL-ADHA-IO Module.

ADHA Testbench software will be developed further from the CCSDS USLP encoder/decoder project (ESA Contract No.: 4000128421/19/NL/GLC)

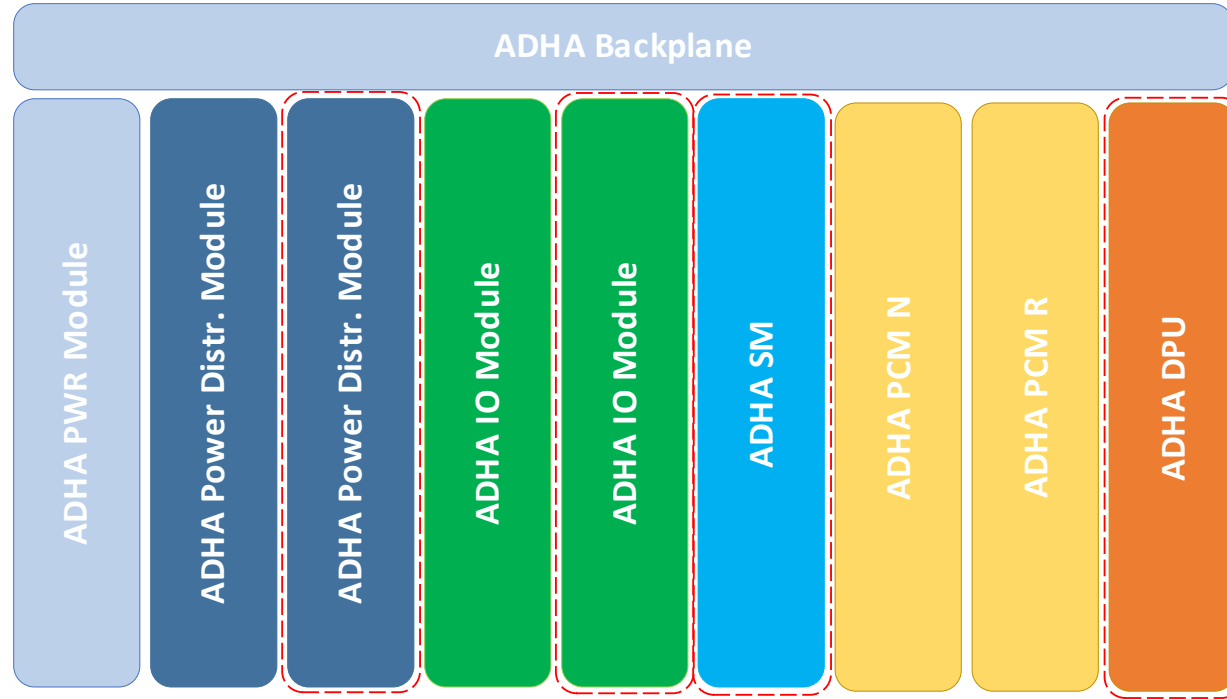
Note: Specification will be addressed as part of ADHA-3 study during 2025, and will be taken into account when it becomes available



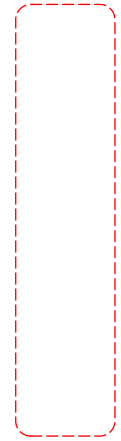
# EIDEL ADHA PAYLOAD INTERFACE CONTROL UNIT (FULL STACK)



# ADHA PAYLOAD INTERFACE CONTROL UNIT - ADHA-PICU - EXAMPLE



Full EIDEL ADHA-PICU stack



Optional module