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# Latest Developments in the Frontgrade Space Computing Ecosystem

24 October 2024, 18th ADCSS

Presenter: Annalena Johansson

# Agenda

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2 GR716B additional features

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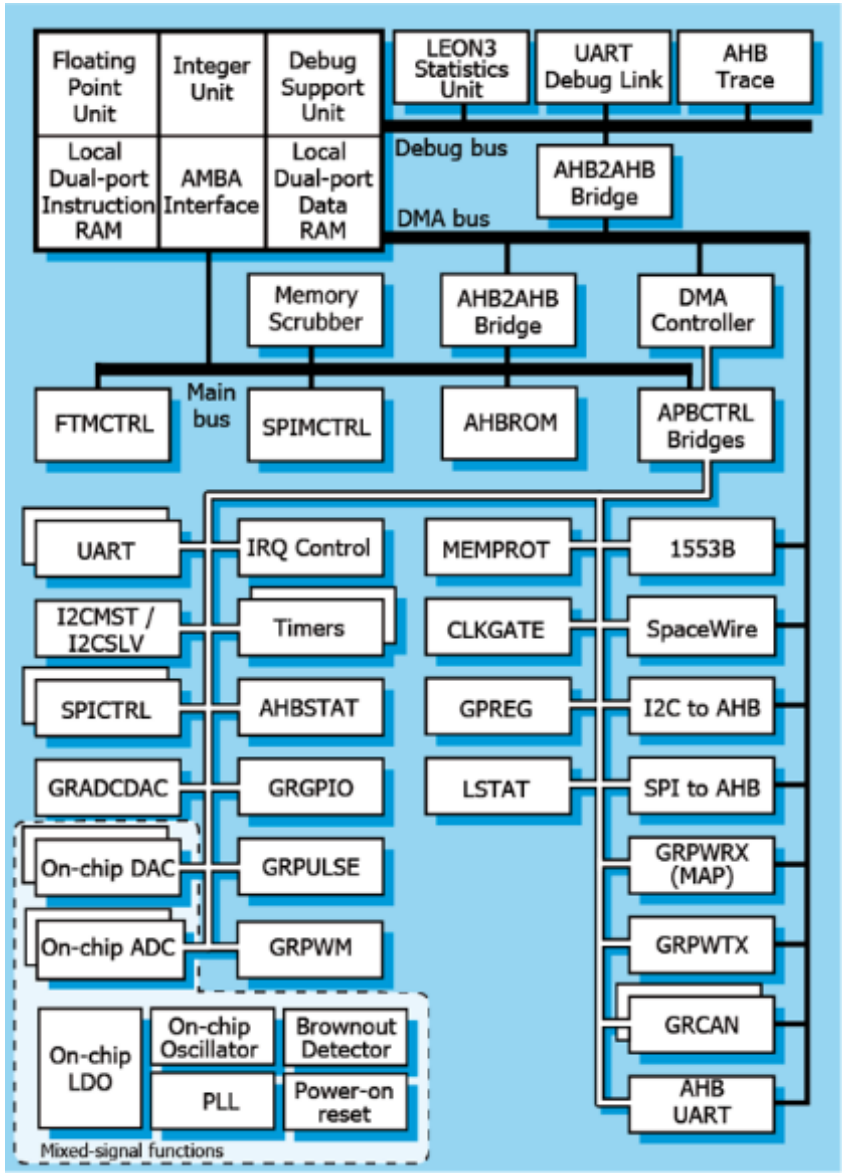
# GR716 microcontrollers: Common Features & Specification

# GR716 - LEON3FT Microcontrollers

- Single-core, Rad-hard and Fault-tolerant LEON3 SPARC V8 processor
  - Floating Point Unit
  - Memory protection units
  - 192 KiB tightly-coupled RAM memory with EDAC
- External EDAC protected memory: 8-bit PROM/SRAM, SPI, I2C
- Many digital I/O interfaces
- On-chip Analog functions like Power-on Reset, ADC, DAC, LDO. Brownout detection etc.
- Pin compatible



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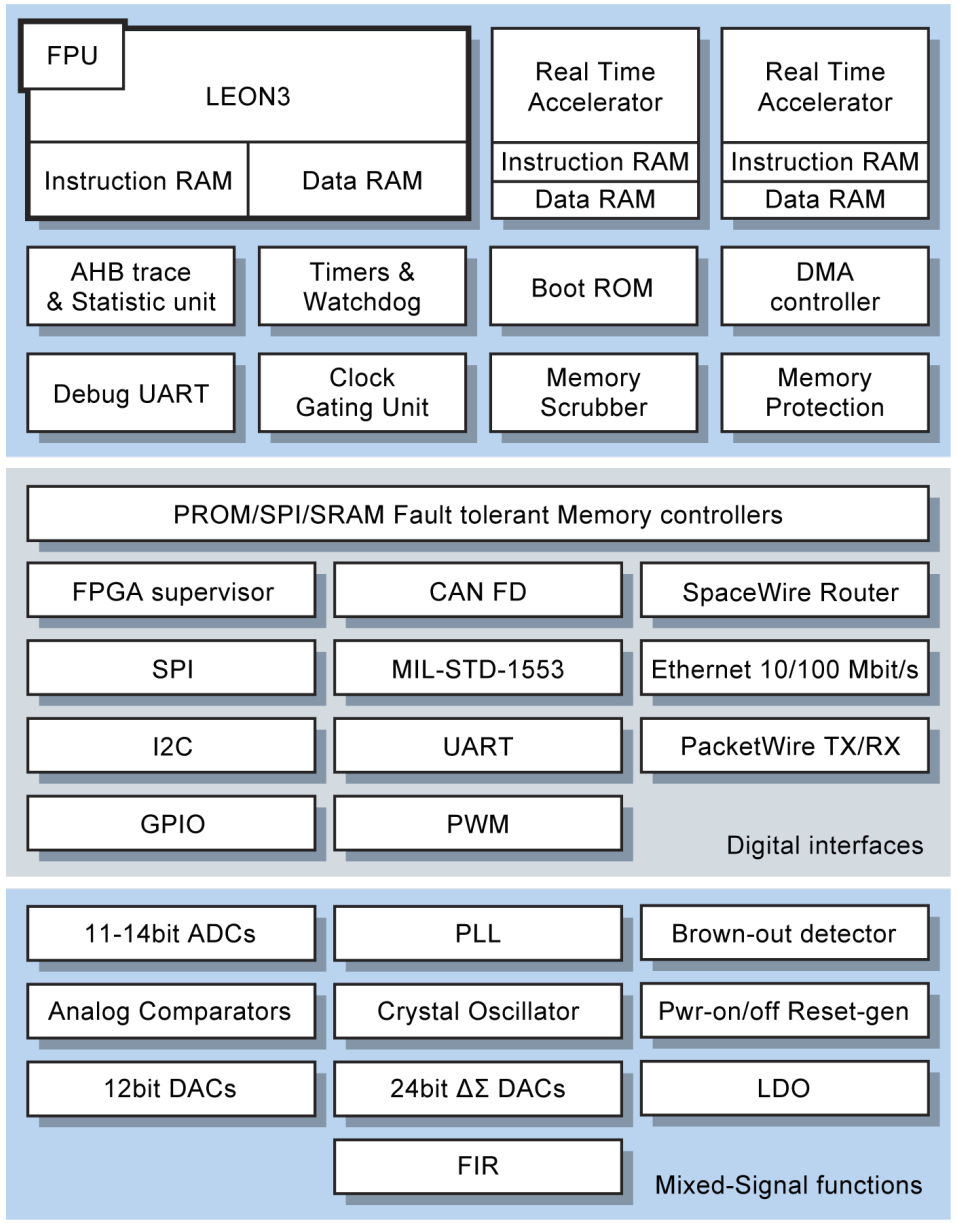
# GR716B – additional features

# GR716B – additional Features

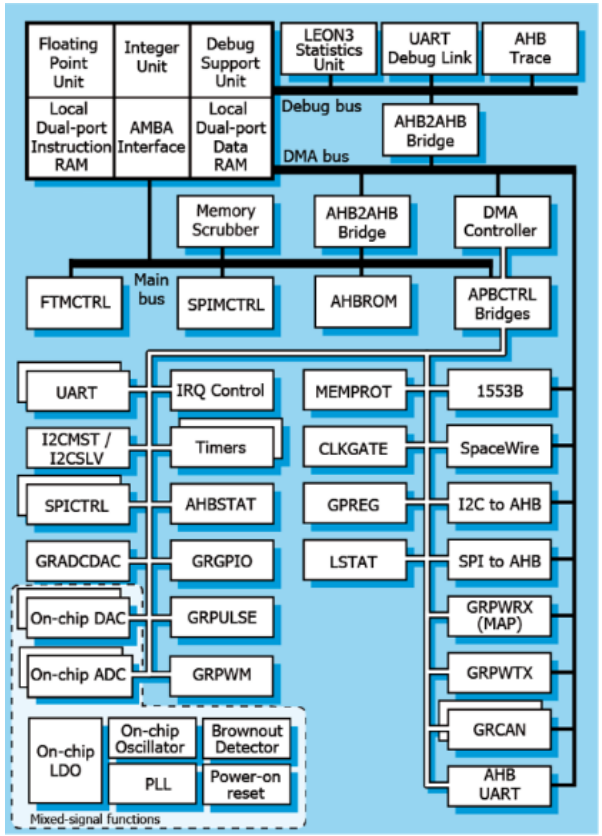
- LEON3FT - Fault-tolerant SPARC V8 32-bit processor, 100 MHz
  - High-Performance Floating Point Unit
- 2x RTA (Real Time Accelerators)
  - Allow complex real-time functions to be implemented independlty from the main LEON3FT
- FPGA supervisor for programming and scrubbing Virtex5 and Kintex UltraScale FPGAs
- DMA controller with support for ‘if-else’ statements
- Enhanced analog cores
- Ethernet 10/100 Mbit/s
- SpaceWire Router with 2 external ports
- CAN FD (Flexible Data Rate)



# GR716 – Digital I/O Interfaces

- SpaceWire Controller
  - Support for RMAP and Time Distribution Protocol.
  - On-chip LVDS or CMOS interface
- Redundant MIL-STD-1553B (BC/RT/BM)
- 2x CAN 2.0B bus controllers (each with nominal and redundant interface)
- 6x UART
- 2x SPI master/slave serial ports.
- 2x I2C master/slave serial ports.
- SPI for Space hardware support for SPI Slave protocol 0,1 and 2
- PacketWire interface with CRC support.
- Programmable PWM interface
- Up to 64 general purpose input and outputs (GPIO) with external interrupt capability, pulse generation and sampling.

Configurable I/O selection matrix with support for mixed signals, internal pull-up/pull-down resistors



# GR716B – Enhanced Analog Cores

**Low Dropout Regulator (LDO)**
- Enables Single 3.3V supply

**Power-on-Reset**

**Brownout Detection**
- 1.8V and 3.3V voltage monitors

**Temperature Sensor**

**PLL**
- System and SpW clock generation

**Precision Reference 1.9 V Output**

**Crystal Oscillator, with external XTAL**

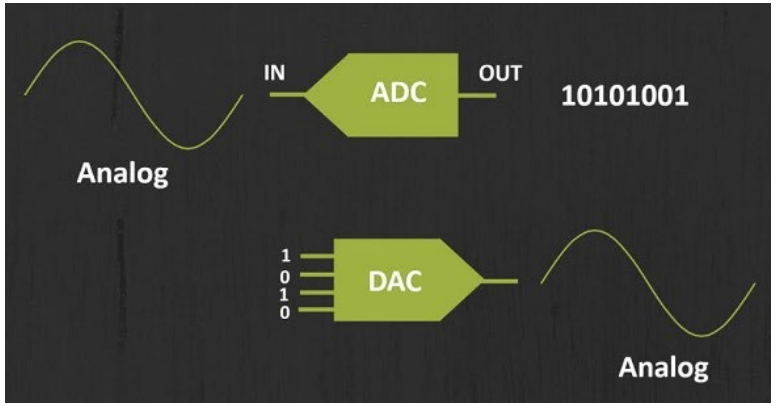
**LVDS transceivers**
- extended common-mode, cold-spare and fail-safe support

**ADC**
- 4x ADC 11bits/14bits @ 500/80 kS/s
- Total channels: 8 differential or 16 single-ended

**DAC**
- 4x 12bit, 3 Msps, digital ramp generation up to 25 MS/s

**Fast Analog Comparators**
- 20 channels
- 7 programmable internal comparison levels or external connection

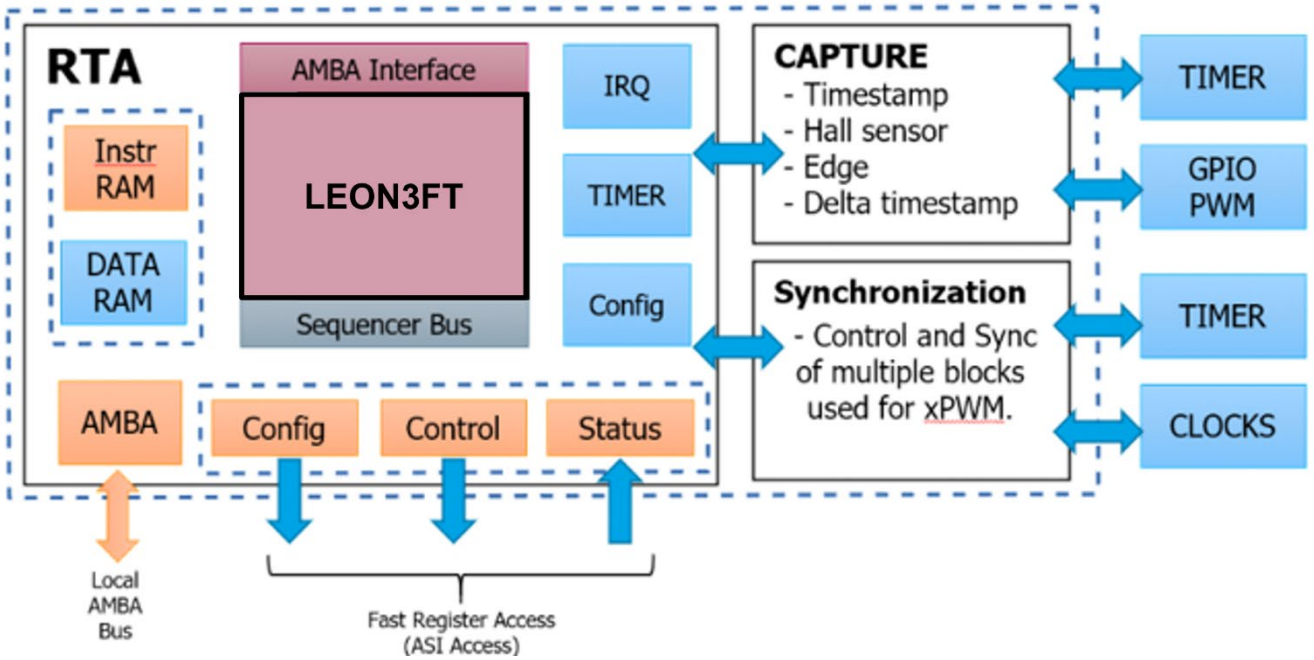
**FIR filter**
- 8 channels, 25Msps, 27 binary programmable taps
- Noise filtering for latch-up detection and other precise applications



# GR716B - Real Time Accelerator (RTA)

**Key takeaways:**

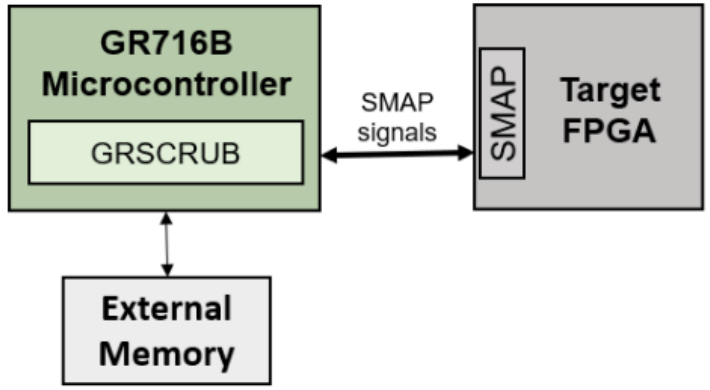
- An RTA can execute software in parallel with the main LEON3FT
- The RTA Task Manager (RTM) can initiate an RTA task routine following real-time events when the sequencer is idle.
- An RTA can execute time-critical real-time functions, such as controlling ADCs & DACs, control-law calculations and performing PWM duty-cycle regulations




Each RTA is isolated from the main GR716B processor ensuring timing independence.

# GR716B - FPGA Supervisor

The FPGA supervisor (GRSCRUB) is responsible for programming and scrubbing FPGA's configuration memory in order to prevent the accumulation of radiation-induced errors.

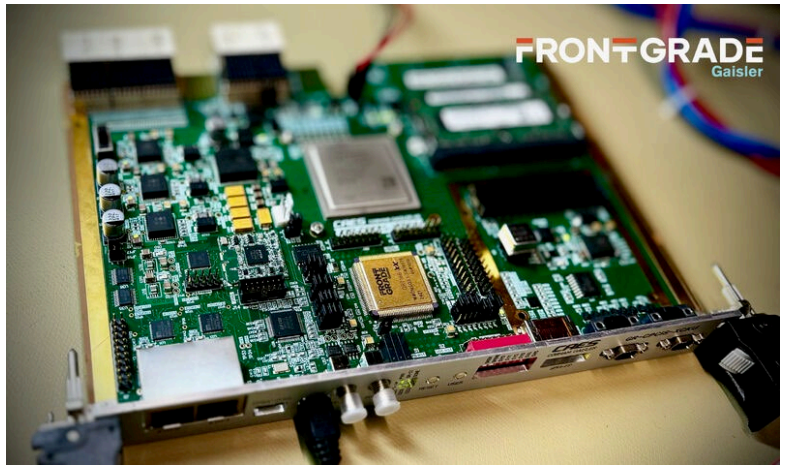



**Baseline features**

- Access target FPGA through the SelectMap (SMAP) interface
- FPGA programming
- Mapping of FPGA frame addresses
- Blind and readback scrubbing allows trade between speed and detection capability
- SEFI detection of the SelectMap interface of the target FPGA
  - allows restoring SMAP functionality after a SEFI
- Targets: Xilinx Kintex UltraScale and Virtex-5 FPGAs
- Periodic scrubbing with configurable delay between runs

**SEE testing**

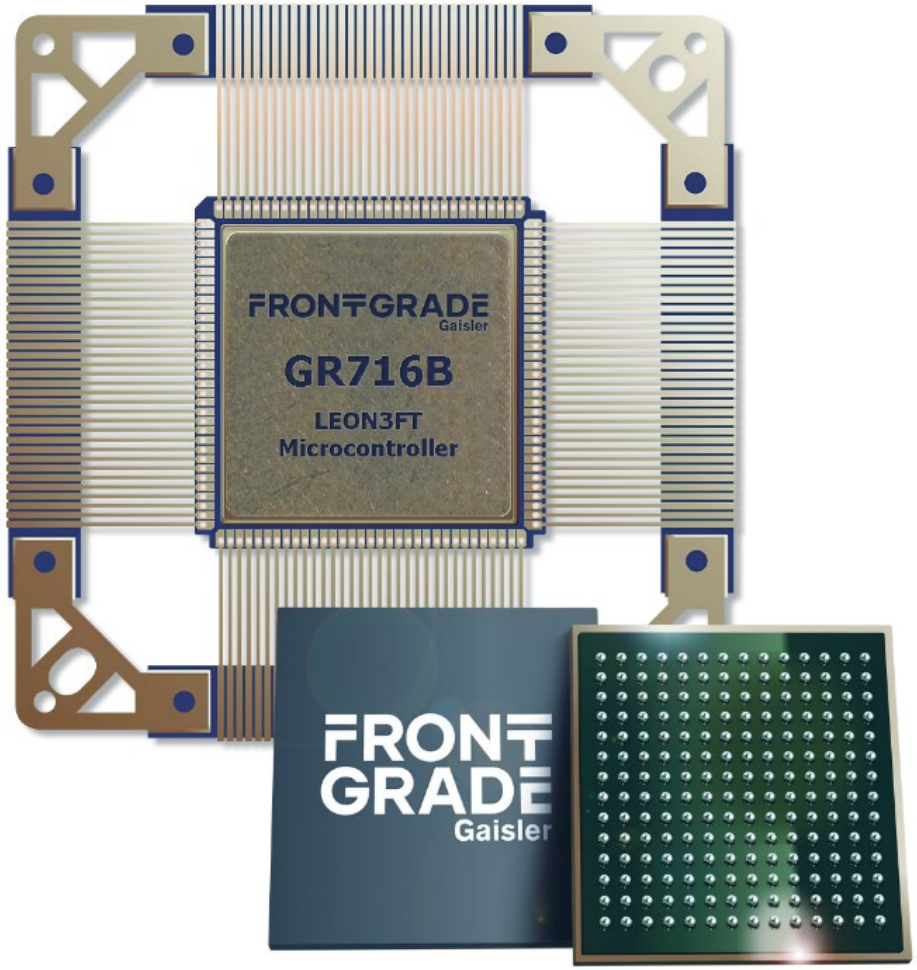
Validated by two proton test campaigns demonstrating that GRSCRUB considerably increases the radiation resilience of the Xilinx Kintex Ultrascale XCKU060



# GR716B LEON Mixed-signal Microcontroller

The GR716B microcontroller is ideal for supervision, monitoring and control in a satellite, such as:

- DC/DC conversion
- Motor control
- Program and scrubber support of FPGA
- Switching power converters
- Power system monitoring and latch-up detection
- Magnetorquer control
- Remote terminal control unit
- Propulsion system control
- Sensor bus control
- Robotics applications control
- Instrument control unit
- Antenna pointing control
- Nanosatellite controller



# GR716A and GR716B – Specification

| Part no. | Processor core | Clock freq. (MHz) | DMIPS/ core | TID krad (Si) | SEL LET (MeV-cm^2/mg) | Power cons. (typical) | Package | Temp. range | Qualification | Availability |
|---|---|---|---|---|---|---|---|---|---|---|
| **GR716A CQFP** | Single-core LEON3FT | 50 | >70 | 100 | > 118 | 320mW | 132-Pin Ceramic Quad Flat Pack | -55°C / +110°C (case) | • Qualification tests as per PCA defined by ESCC Basic Specification No. 2567000<br>• Screening tests as per ESCC 9000 | Flight parts available |
| **GR716B CQFP** | Single-core LEON3FT + 2x RTA | 100 | >140 | 100 (TBC) | > 118 (TBC) | (TBC) | 132-Pin Ceramic Quad Flat Pack | -55°C / +125°C (case) | • ESCC9000 lot qualification (planned) | Prototypes in December 2024* |
| **GR716B PBGA** | Single-core LEON3FT + 2x RTA | 100 | > 140 | 100 (TBC) | > 118 (TBC) | (TBC) | 400 – Pin Ball Grid Array | TBD | • TBD | Prototypes in February 2025* |

**Software toolchains and debugger are available**

GR716A vs GR716B application note available @ Gaisler.com/GR716B

GR716A and GR716B are pin compatible when the same on-chip resources are used. Software needs to be recompiled.

*Subject to change without notice

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# GR716: Software Ecosystem

# GR716 - Software Ecosystem

## GRMON 3.3 C/C++ Debugger

- C/C++ language source level debug capability
- GUI integration
- RTA support
- See dedicated webpage

## GR716B TSIM Simulation

- Cycle-accurate simulator
- Software development can start using simulator before hardware is available
- See dedicated webpage

## Zephyr RTOS

- GR716A/B BSPs and drivers
- See dedicated webpage

## BCC2 – Bare Metal Cross Compiler

- GR716A/B BSPs and drivers
- See User's Manual

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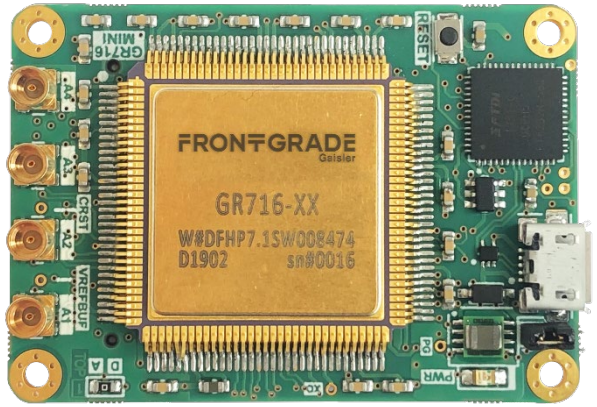
# GR716: Evaluation Boards

# Evaluation Boards for both GR716

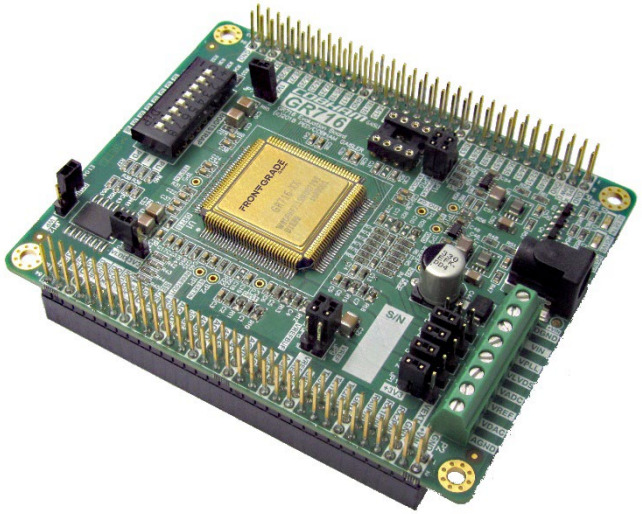
## GR716-MINI




- Size: 37.5% of a credit card
- SPI Flash & SRAM memories
- Available for free-of-charge, time-limited loans

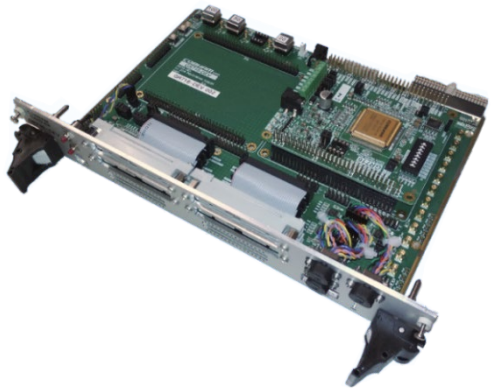
## GR716-BOARD-Daughter

Webpage



- 8 cm x 10 cm format
- Stackable pin headers for I/O interfaces (64)

## GR-CPCI-GR716-DEV Interface Board

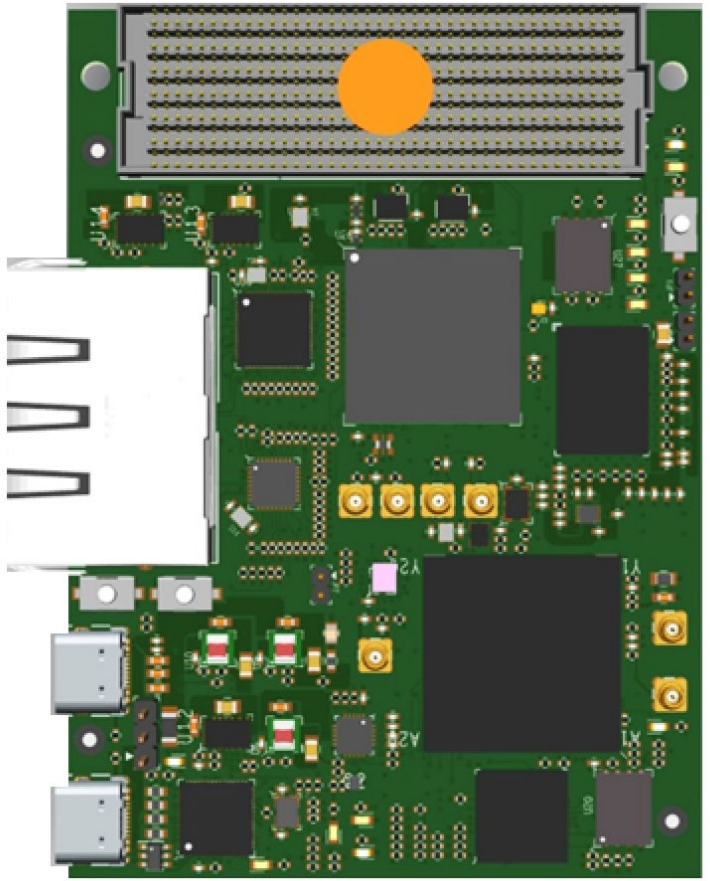


- CPCI 6U format
- Facilitates access to all the I/O and memory interfaces

# GR716B-MIDI-BOARD

- Small form factor
- USB-C connector for debug and power
- GR716B Processor
  - 1 x Ethernet for communication
  - 1 x SpaceWire to FMC+ connector
  - 1 x SpaceWire to FPGA
  - 64Mb x 16 MRAM
  - 512Mb SPI FLASH
  - 2 x High performance ADC to on-board MMCX connector
  - 1 x DAC channel to on-board MMCX connector
  - 1 x on board thermistor
  - 41 x GPIO connected to FMC+ connector
- CertusPro FPGA
  - 1 x Ethernet for communication and debug
  - 4 x SerDes to FMC+ connector
  - LVDS to FMC+ connector
  - 3V3 I/O to FMC+ connector
  - 1GB DDR3
  - 512Mb SPI FLASH
  - 4 x Analog channels to on-board MMCX connector

Available for free of charge, time-limited loans



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# GR765 Multi-Processor System-on-Chip

# Instruction Set Architectures

### Why RISC-V?

- Hardware and software potential for future space applications: A new class of processors requires a modern architecture
- Enabling new technologies by standardization
  - Hypervisor support
  - Vector extension, …
- Growing base of 3rd party ecosystem:
  - Toolsets
  - Libraries, engines etc.
- Attractive to talent entering the space domain
- Influx of know-how by talent entering the space domain

RISC-V®

### Why SPARC?

- Existing base of space proven HW and SW designs
- Mature ecosystem for today's space applications, e.g. qualified OS
- Accumulated development know-how in the industry
- Software backward compatible with existing LEON devices

SPARC

### GR765 provides RISC-V and SPARC

- Both architectures are needed by the industry
- Faster time-to-market for RISC-V while continuing SPARC – ease transition between the two architectures
- Minimal silicon overhead - sharing of resources on chip. User selects CPU (LEON5FT or NOEL-VFT), device cannot operate with both at the same time.

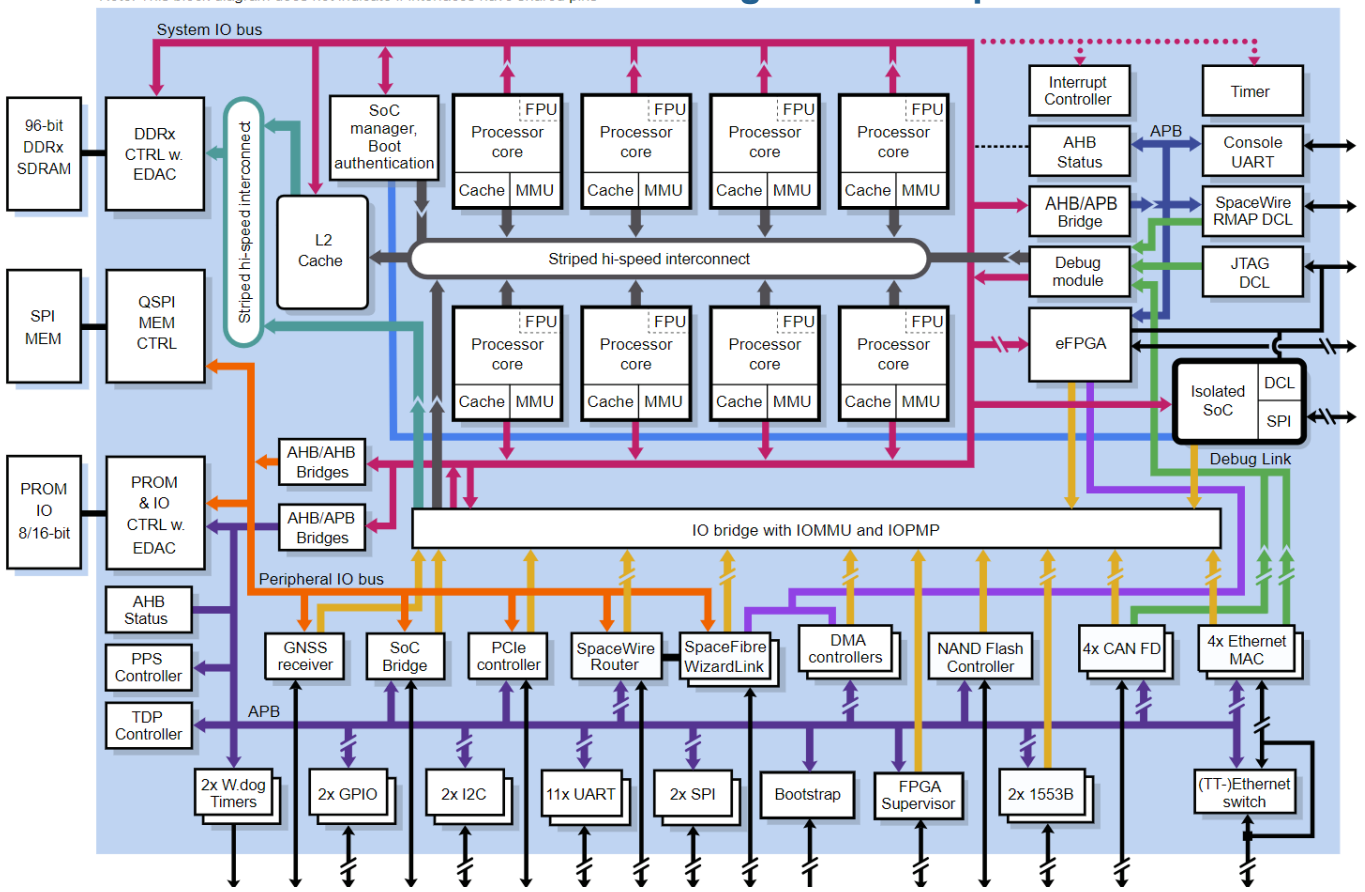
# GR765 – Octa-Core Processor

- Fault-tolerant **octa-core** architecture
  - **LEON5FT SPARC V8 or NOEL-V RV64GCH**
  - Dedicated FPU and MMU, 64 KiB per core L1 cache, connected via multi-port interconnect
- **1 GHz processor frequency - 26k DMIPS**
- 4+ MiB L2 cache, **512-bit** cache line, 4-ways
- **DDR2/3/4** - TBC
  - 96-bit interface with dual x8 device correction capability
  - 80-bit interface with x8 device correction capability
  - 72-bit interface with error detection capability (parity)
- 8/16-bit PROM/IO interface
- **(Q)SPI and NAND memory controller interfaces**
- **eFPGA 30k LUT**
- **Built-in GNSS receiver for (GPS and Galileo) – NavRix IP from Beyond Gravity**
- **Hardware authenticated boot (hybrid scheme with ECDSA, ML-DSA)**
- **Isolated SoC offering authentication / crypto / RoT functionality**
- **LGA1752/FF1752 package**
- **Target technology: STM 28nm FDSOI. ESCC9030 qualification**

**In development**
**No guarantee of product launch**

LEON5 NOEL-V

Note: This block diagram does not indicate if interfaces have shared pins




SPARC RISC-V®

# GR765 – Interfaces

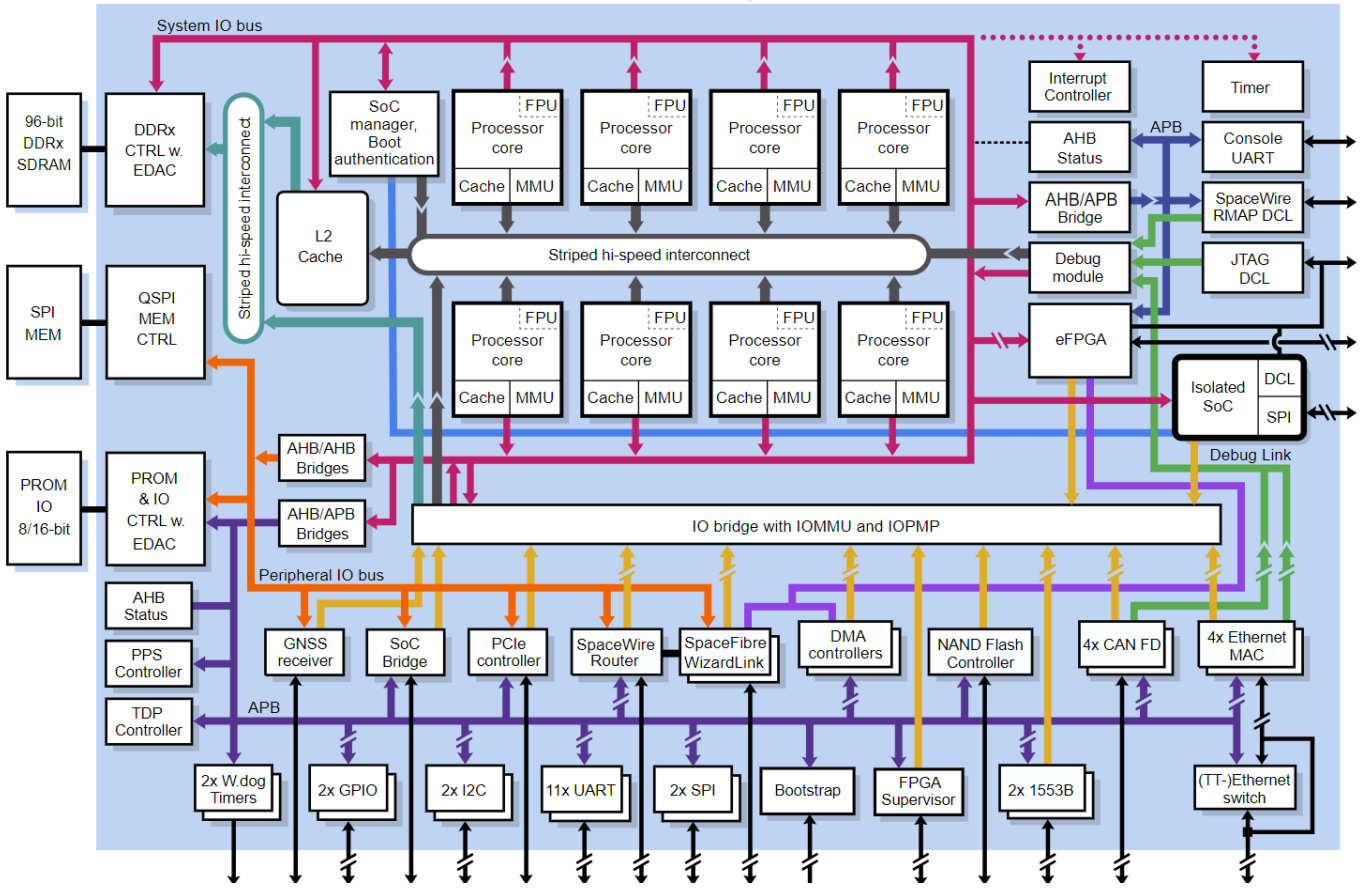
**Interfaces – SPARC and RISC-V mode**

- **PCIe Gen 3 2 port x4, or 1 port x8 with Root Complex**
- **SpaceFibre 4 ports x1 6.25 Gbit/s + WizardLink support (TBC)**
- **12-port** SpaceWire router with +4 internal ports
- **4x** 10/100/1000 Mbit Ethernet **w. TTEthernet capable switch**
- **2x** MIL-STD-1553B
- **4x CAN FD**
- **2x I2C interface, 12** x UART, **2x** SPI controller
- **SoC Bridge interface**
- **FPGA Supervisor interface**
- **Timers & Watchdog, GPIO ports**
- **Debug links:**
  - Dedicated: JTAG and SpaceWire
  - CAN, Ethernet

**In development**
**No guarantee of product launch**

LEON5 NOEL-V

Note: This block diagram does not indicate if interfaces have shared pins

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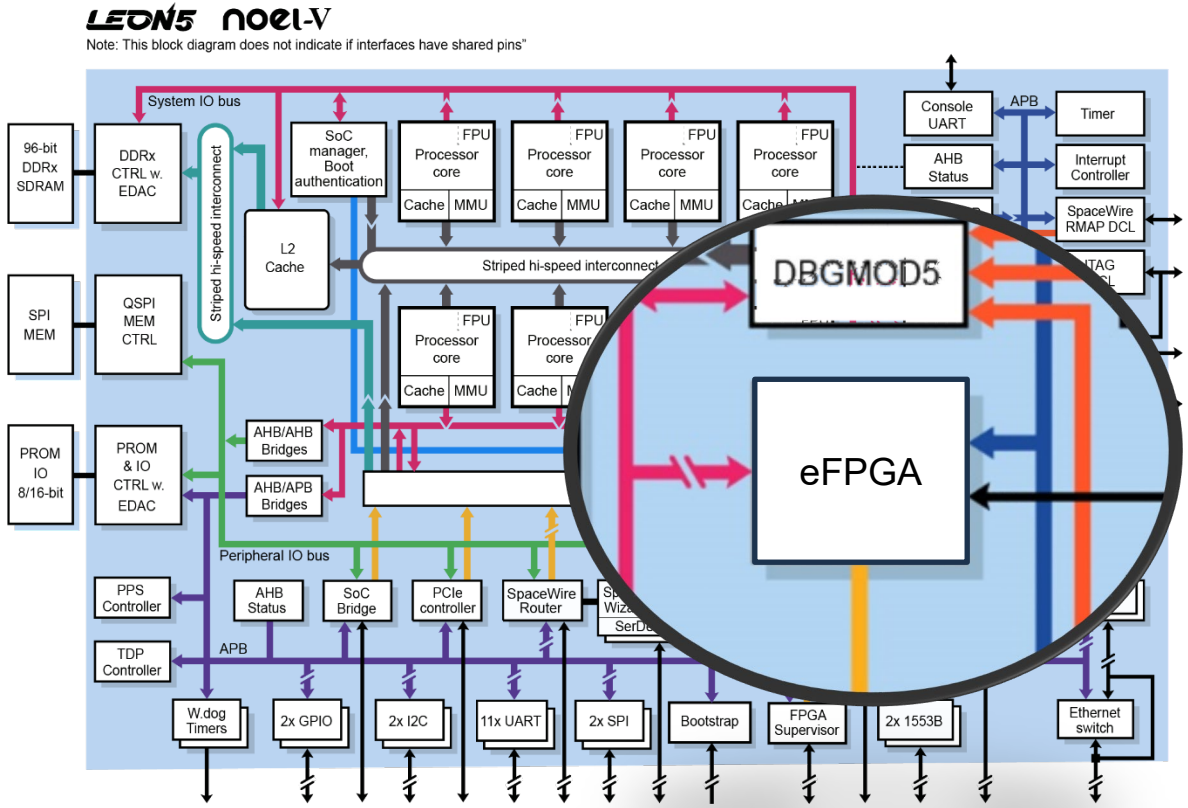
# GR765 – eFPGA

- **GR765** will incorporate a **NanoXplore eFPGA**
- **30’000 LUT** logic resources
- The eFPGA subsystem will be possible to operate **without processor** intervention.
- **Reprogramming** of the eFPGA will **not affect processor execution**.
- The eFPGA subsystem will be **programmable** from **processors**.
- **Bitstream authentication** will be available.
- Supported by **standard NanoXplore tool set.**
- Supported by **GRLIB IP** cores.




SPARC RISC-V®

NanoXplore

# GR765 – Security Feature Overview

**Functional separation (Time and Space Partitioning)**

- NOEL-V H extension + Advanced Interrupt Architecture + IOPMP/MMU
  - Allows to group IO units together with guest VMs and to separate VMs+IO from each other.
  - Same IOMMU implementation for both SPARC and RISC-V modes

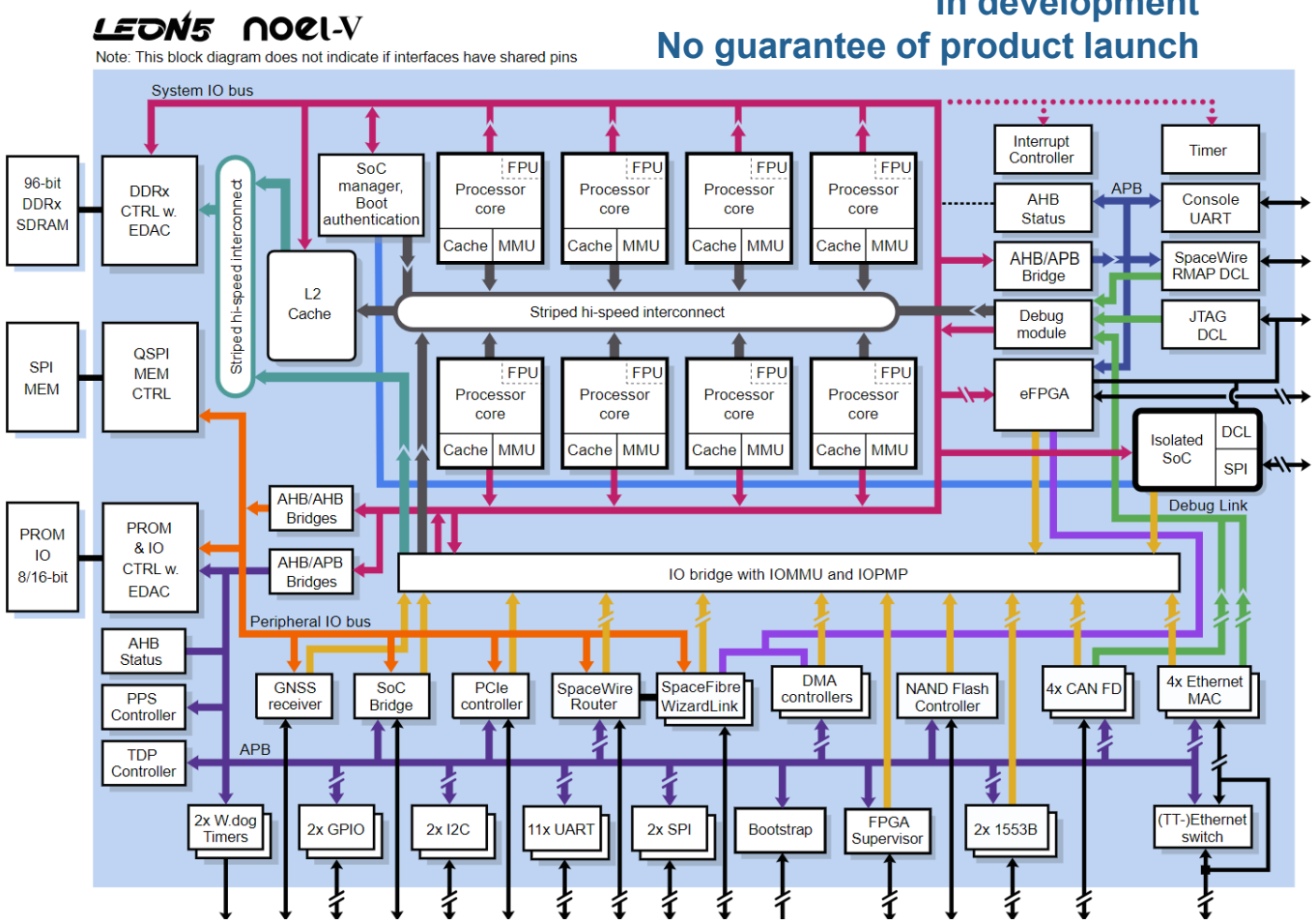
**Timing isolation (safety and security)**

- Striped interconnect can be configured to group processors and IO peripherals into groups without timing interference between them.

**Cybersecurity features**

- NOEL-V Control flow integrity (RISC-V standardization ongoing) – no jumps or return to wrong place
- Authenticated boot HW and Isolated SoC
  - Provide authentication of boot software and FPGA images before they are used in the system
  - Provide crypto key storage

**In development**
**No guarantee of product launch**

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# GR765 - Software and Development support

## Next-Generation SoC

# Software

- Complete ecosystem
- A combination of Gaisler and 3rd party software

**Tool chains, Operating systems and compilers**

- Bare-C
- Linux
- RTEMS
- VxWorks
- Zephyr

**Hypervisors**

- XtratuM/XNG (FentISS)
- PikeOS (SYSGO)
- Xvisor

**Boot loaders**

- MKPROM2
- GRBOOT Flight bootloader

**Tools**

- GRMON3
- TSIM3

# GR765 Development Support

- The following development support is planned as part of the GR765 product development

  - GR765 evaluation board – Low complexity board (-MINI concept): DDR3 SDRAM, SPI Flash for boot memory, 2x, SpFi, 4x SpW, 1x JTAG, 1x Eth, 1x UART, 2x CAN FD – Performed as part of GR765 phase 2 RISC-V add-on. Planned to be available at the same time as first prototype devices.
    (Developed within GR765 PH2 RISC-V activity)

  - GR765 development kit – Fully fledged board, all interfaces available, targeting ADHA compliance.
    (Developed within GR765 PH3)

  - GR765 SBC reference design – Reference design development, develop flight SBC concept. Timing analysis to be performed for critical interfaces.
    (Developed within RISC-V TDE)

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# Status and Schedule

Next-Generation SoC

# Status and Schedule