EEE Space Component Sovereignty for Europe
Ultra Deep Submicron Microelectronic Technologies

ADCSS 2024
October 22 – 24

Boris Glass
TEC-EDM

Outline

- European Sovereignty and Supply Chain
- Activities' Status 2024
- UDSM Activities
- IP Building Blocks
- Development Plan

1: Vision – European Sovereignty

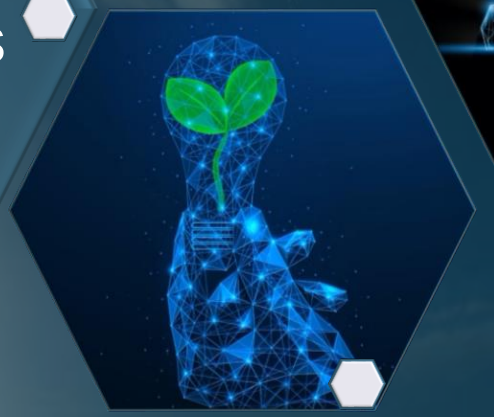
Sustainable products, no access restrictions

Increase European competitive-ness

Strong European Supply Chain

Strategic partnerships

Time-to-market of qualified products



EEE Space Component Sovereignty for Europe

- To establish/reinforce a sustainable European supply-chain for state-of-the-art, high-value European EEE Components in a timely manner
- Creation of the GSTP Component "**EEE SPACE COMPONENT SOVEREIGNTY FOR EUROPE**" (GSTP EEE Sovereignty Component)
- Implementation principles are based on approach used for GSTP Element 1 "Develop" (compendium, WorkPlan/Procurement Plan, Letter of Support, ITT, Contract)
- Work plans will be structured along **6 technology lines**
- A key objective is to implement an end-to-end fully coordinated plan for each Technology Line.

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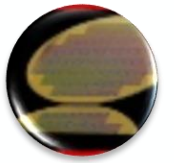
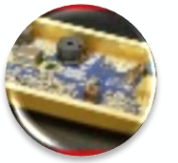
WBG Power and RF



Photonics

Solar Cells

Packaging, PCB and EA



Test Facilities

EEE Sovereignty initiative – Status - 2024

Test Facilities

GTE3-601QE - Development of a High Energy Ions Beam Testing Capability (>22MeV/n)

Wide Band-Gap Power and RF

GTE3-201ED - Super Scaled Nitride Technology (S2CANT)

GTE3-202ED - European Power GaN supply chain (EPOGAN)

GTE3-203ED - European Power SiC supply chain (EPOSIC)

GTE3-204ED - Thermal Heat Reduction techniques for Semiconductor Technology (THRUST)

GTE3-205ED - GaN monolithic IC Pre-Industrialisation development (GaNICp)

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GPP

FPGA

GTE3-101ED - Ultra Deep Sub-Micron Foundation and Platform Technology

GTE3-102ED - Ultra Deep Sub-Micron Interface and System-in-Package Technology

EEE Sovereignty initiative – Status - 2024

Overview

- ITT => contract for approved activity
- Workshop / OSIP campaign for UDSM, Photonics, Packaging and PCB
- WP update
- CM25 preparation

11 Participating States
90 M€

ITT/RFQ
GTE3-203ED
GTE3-601QE

ITTs
GTE3-101ED
GTE3-201ED
GTE3-204ED

RFQ
GTE3-205ED

Contracts
GTE3-203ED
GTE3-601QE

Contracts
GTE3-101ED
GTE3-201ED
GTE3-204ED

WP/PP Update

Workshops/OSIP Campaign

WP/PP Update

ITT
GTE3-102ED

Contracts
GTE3-102ED

Q1 2024	Q2 2024	Q3 2024	Q4 2024

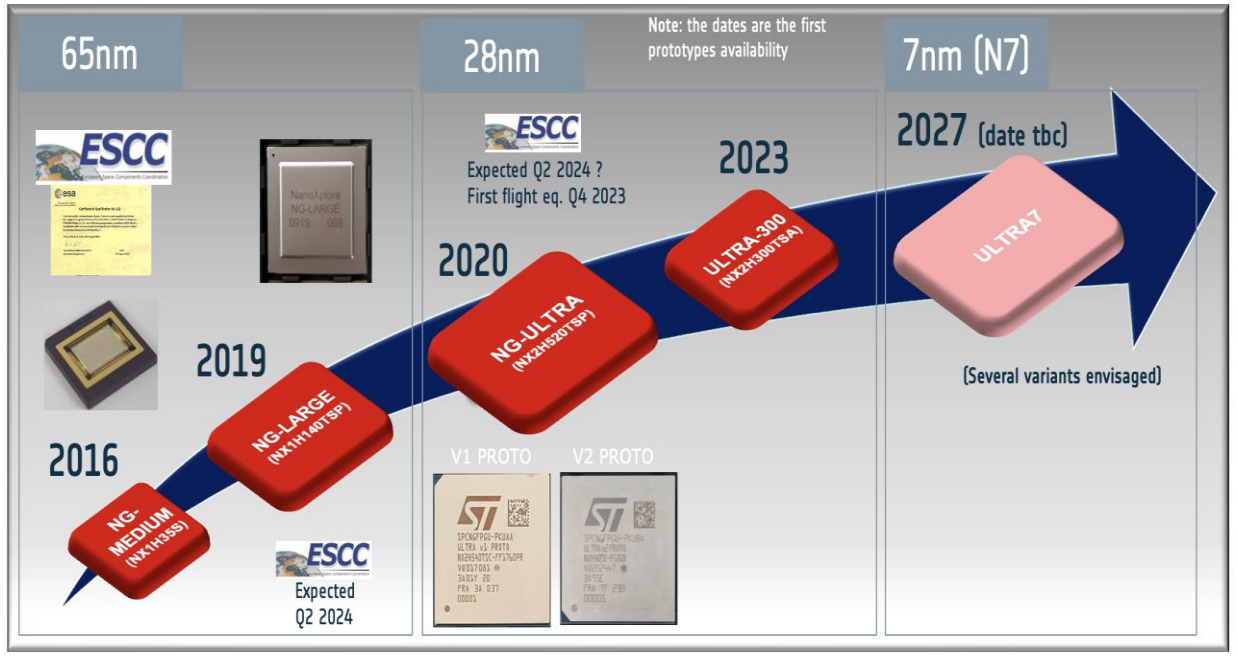
2: ESA - EC Collaboration and development plan

Collaborative approach

- Strong synergy with European Space Component Coordination (**ESCC**) /Component Technology Board (**CTB**)
- ESCC CTB roadmaps and Harmonisation roadmaps fully considered as a basis, but with additional supporting information (business case, quantified space system performance benefits, etc.)
- Coordination with National Agencies, **EC**, **EDA** using existing channels (e.g. **JTF**)
- No direct link to European Chips Act however with expectations that there will be synergies
- Working Arrangement between ESA and EC on the Coordination of Security Critical Electrical, Electronic and Electro-mechanical Components (**SecEEE**)

Demonstrated Track Record

- 4 products in less than 10 years

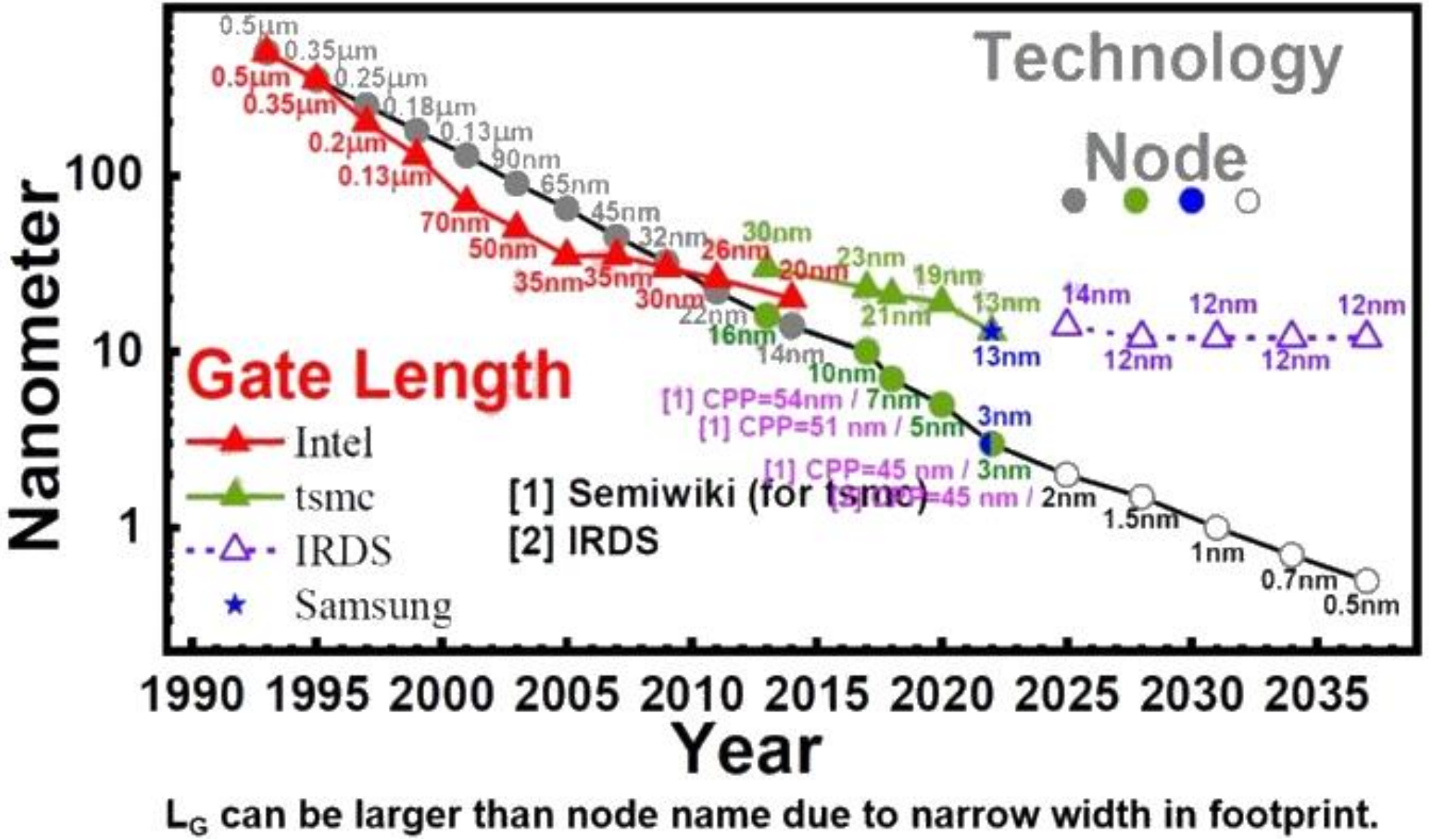


In this context, there is a need to accelerate the development of European space FPGA based on 7nm (N7). The Commission and the European Space Agency should join forces and ensure complementarity and consistency between their respective activities. We should build upon the very good example of cooperation we put in place to support the development of FPGA based on 28nm, a few years ago.

European Commission

EUROPEAN DEFENCE AGENCY

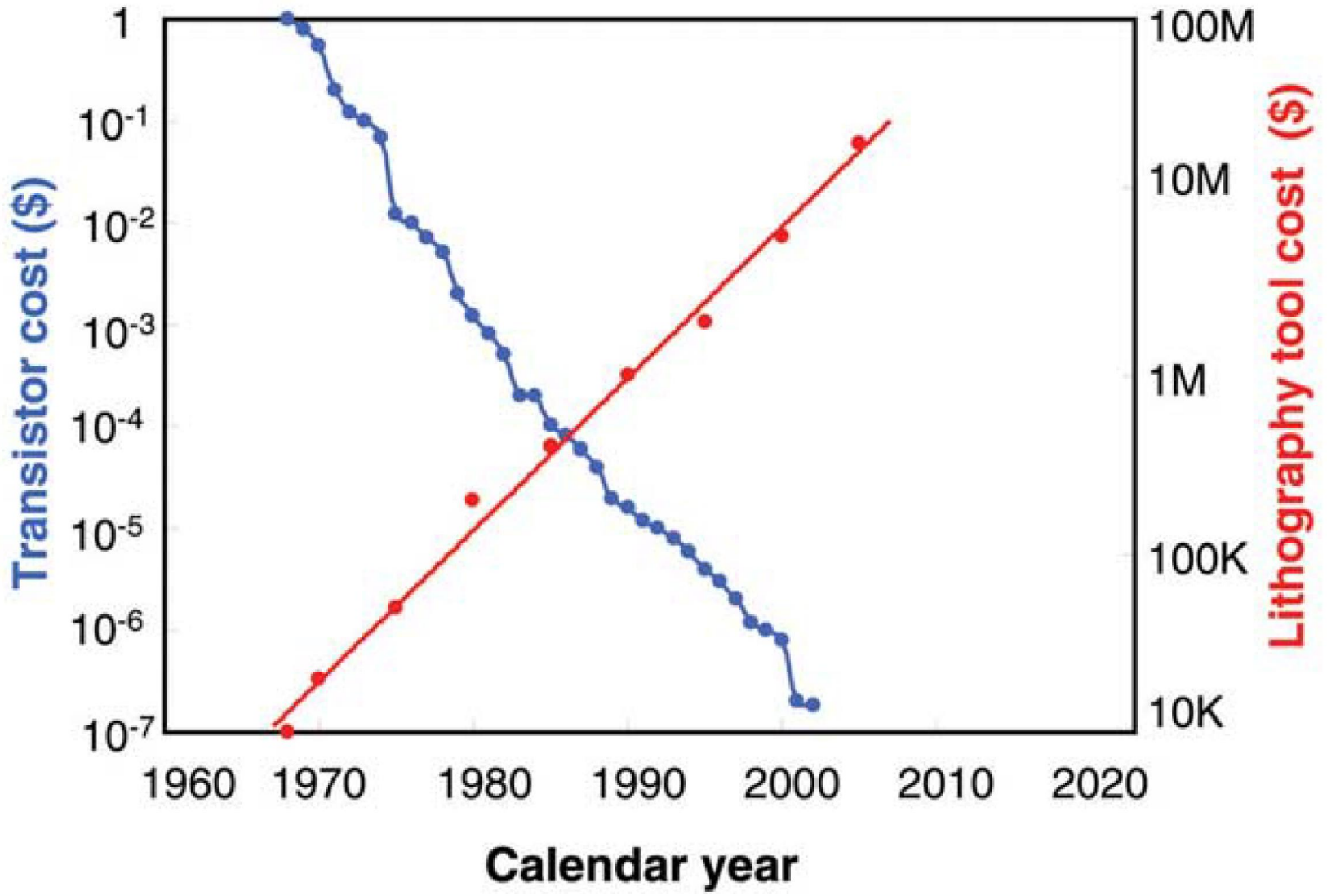
Technology Scaling – Gate Length Evolution



L_G can be larger than node name due to narrow width in footprint.

Sachidananda Dash
DRAM Product Engineer at Micron Technology
Taichung City, Taichung City, Taiwan

Technology Scaling – Lithography Cost



Moore's law: the future of Si microelectronics

Scott E. Thompson ✉, Srivatsan Parthasarathy ✉

Ultra Deep Sub Micron (UDSM) Activities – Status

- UDSM 0 - ARTES AT 5C.443 (2 M€) - ***INFINIT***
  UDSM Assessment for On-Board Digital Processors
  Assessment of 7nm technology and libraries
  Kick-Off January 2024, 1st test vehicle tape-out on October 15th.

- UDSM 1 – GTE3-101ED (9 + 10 M€)
  Foundation Library and Platform Technology
  Kick-Off November 2024

- UDSM 2 – GTE3-102ED (10 + 10 M€)
  UDSM Interface and SiP Technology
  Workshop held on May 23-24 at ESTEC
  ITT in Preparation

Objectives

Ultra Deep Sub-Micron

GPP

GTE3-101ED - Foundation and Platform Technology

19ME – Kick Off: 15 Nov 2024

Description :

FDSOI STM 28nm

- Die to die interface in 28nm – (CNRZ and/or UCIe)

FDSOI GF 22nm

- Foundation library
- Die to die interface in 22nm – (CNRZ and/or UCIe)
- HSSL SR and LR 28G
- DDR4
- PCIe, Ethernet, SpF controller
- **Router 28G**

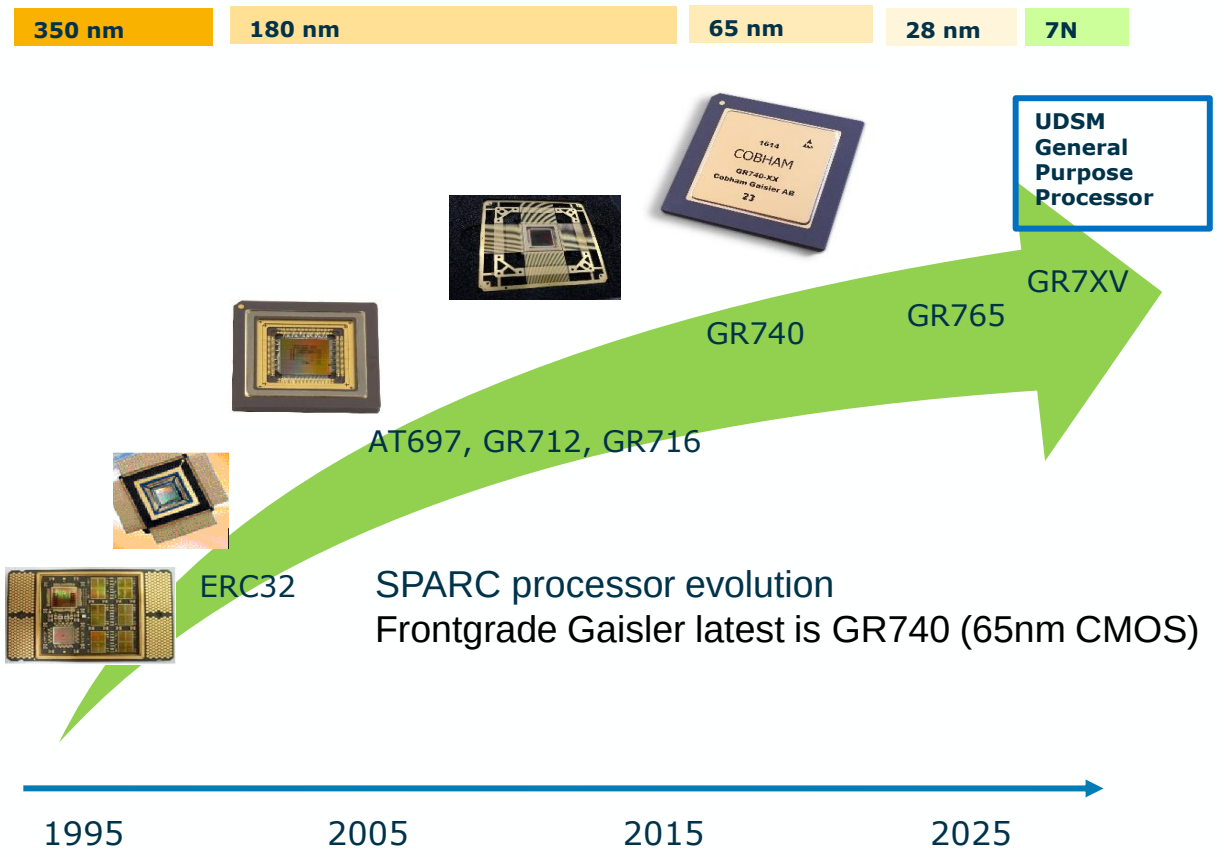
FinFET TSMC N7

- Foundation library
- **RISC-V Chiplet**

TO: B. Glass

Objectives: General Purpose Processor:

- Develop next generation European space general purpose processor, based on open-source RISC-V and exploiting N7 FinFET technology
- Develop a mature SW tool ecosystem to exploit multi-core parallel processing



Status

Ultra Deep Sub-Micron

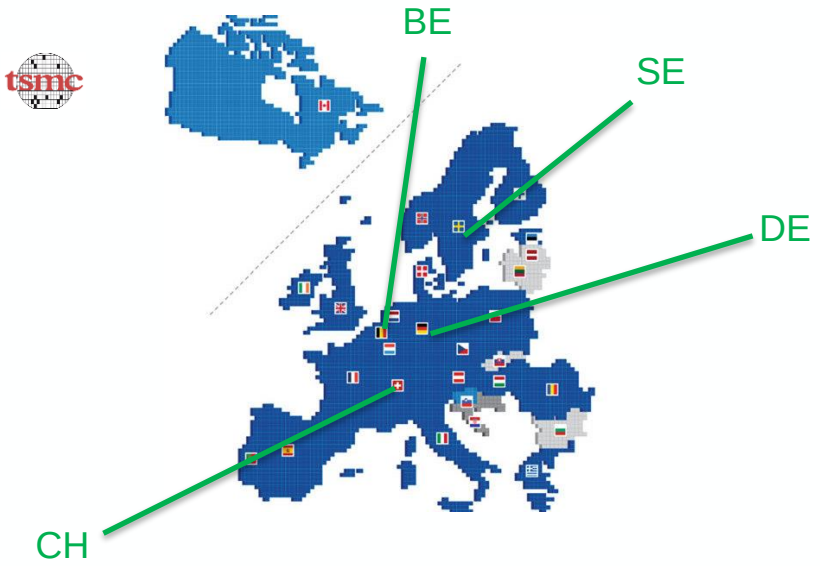
GTE3-101ED - Foundation and Platform Technology

19ME – Under evaluation

Status: Negotiation finished, Kick off on November 15, 2024

Challenges:

- ❑ Alignment with GTE-102ED



TO: B. Glass

Objectives

Ultra Deep Sub-Micron

FPGA

GTE3-102ED - Interface and System-in-Package Technology

20ME – Under preparation

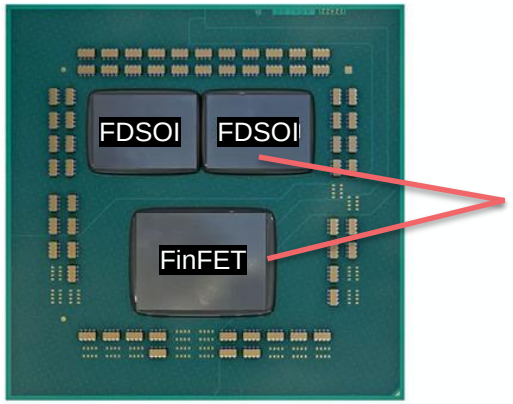
Description :

Contribute to the FPGA Development Roadmap

FinFET TSMC N7

- Foundation library
- Die to die interface in 7nm
- HSSL LR 112G
- PCIe, Ethernet and SpF controller
- DDR4
- **FPGA/DSA chiplet**

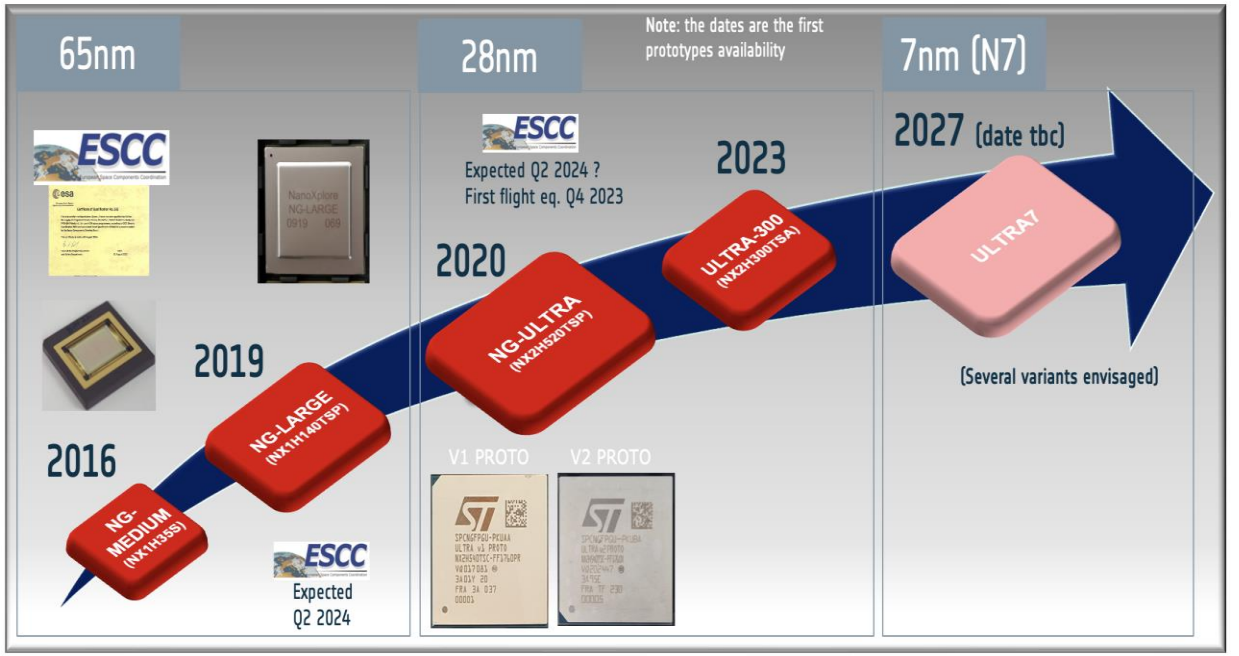
SiP Technology



Chiplets

Roadmap: Field Programmable Gate Array (FPGA):

- Increase portfolio of European FPGAs (RF and security)
- Develop next generation FPGA ULTRA 7
- Mature FPGA development tools



Status

Ultra Deep Sub-Micron

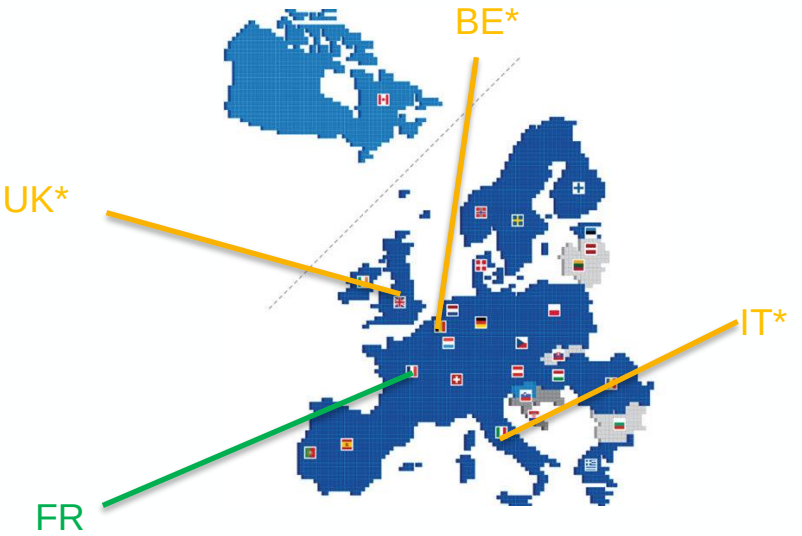
GTE3-102ED - Interface and System-in-Package Technology

20ME – Under preparation

Status: ITT in preparation, seeking for delegate support

Challenges:

- ❑ Aligning IP specification
- ❑ IP cross licensing of building block IP
- ❑ Testchip manufacturing



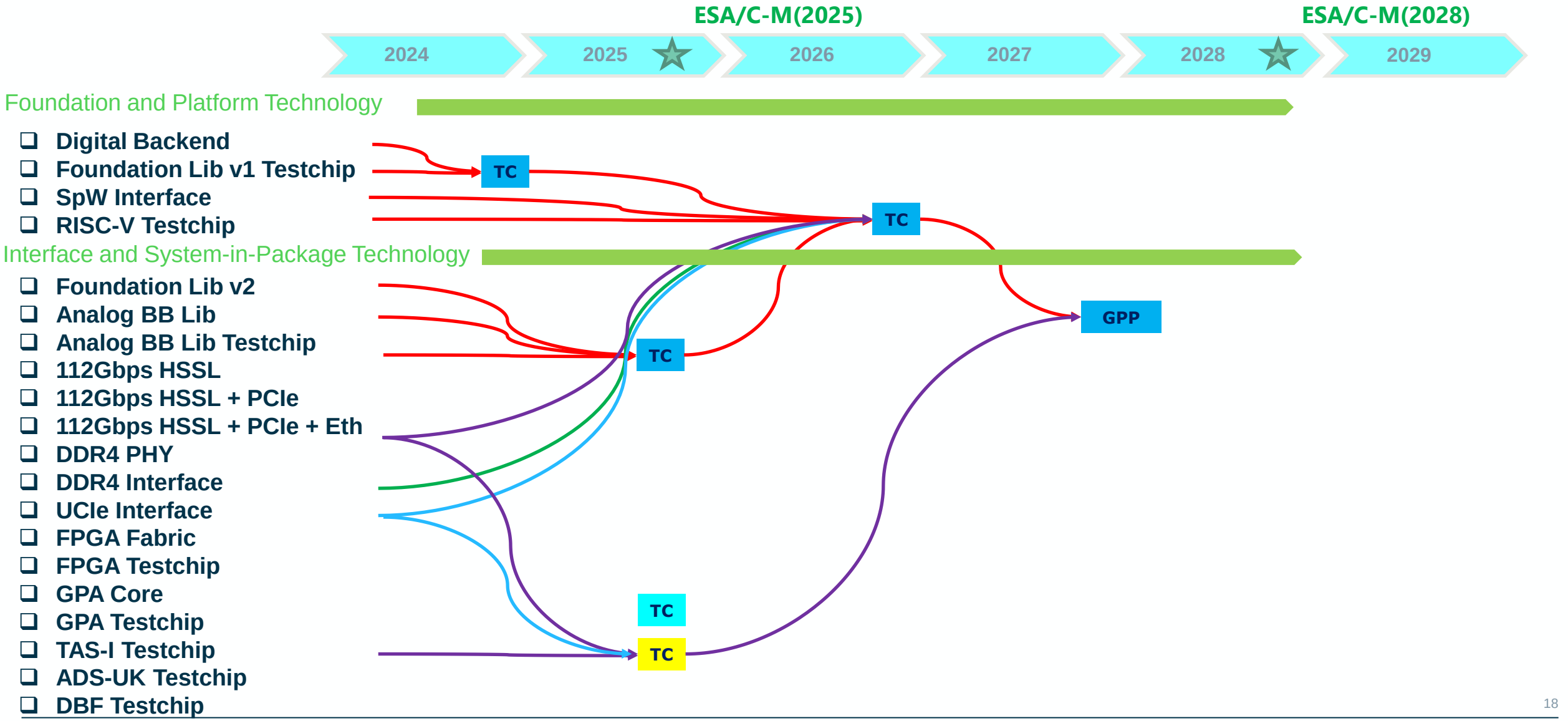
* Interest confirmed, support to be provided

TO: D. Merodio

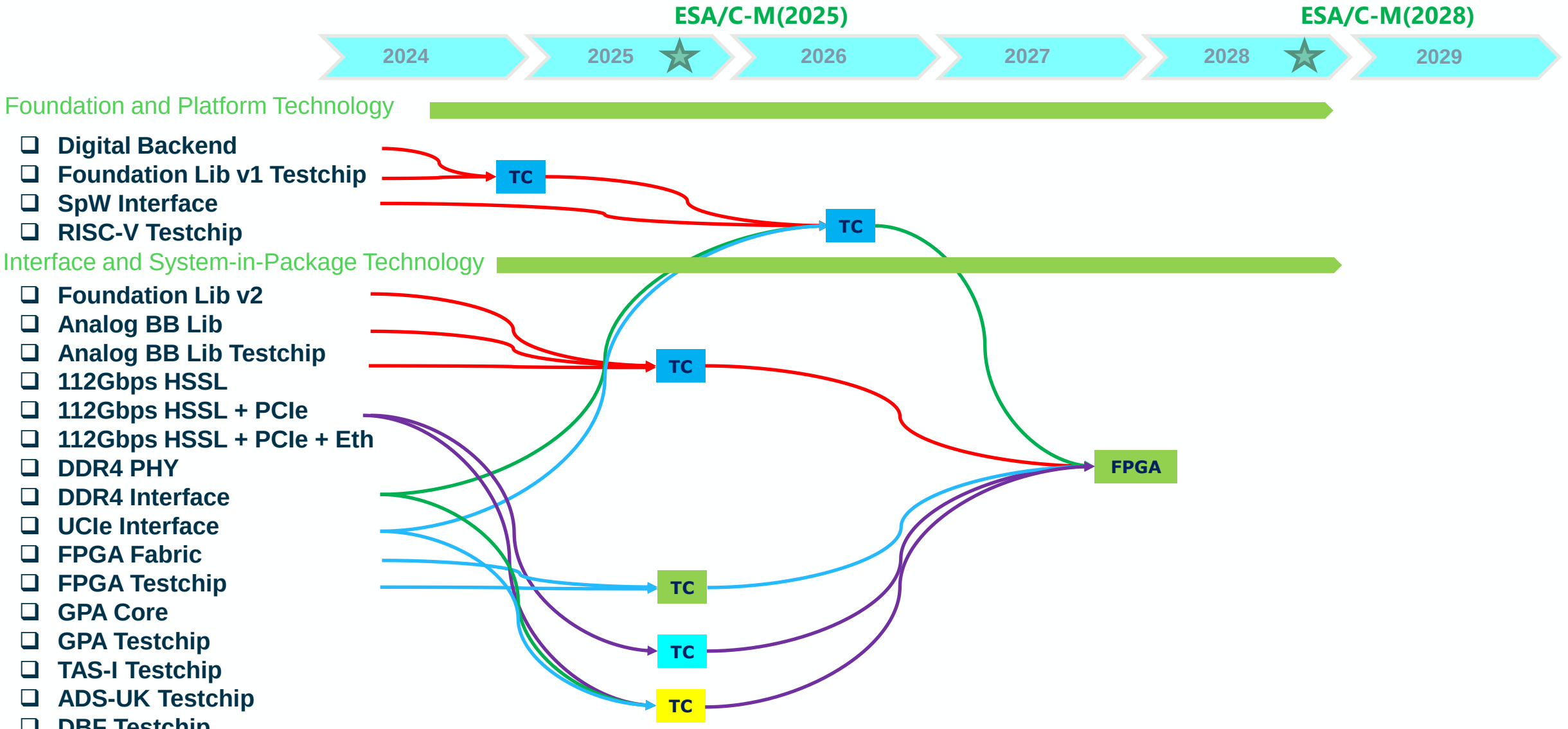
UDSM Technology and IP

- Foundation (digital cells, memory blocks, IOs, ..,) Library
- Analog Building Blocks (T Sensor, P and Aging Monitors, Oscillator, PLL, …)
- Interfaces (LVDS, …)
- High Speed Serial Link (Long Range) PHY
- PCIe controller
- Ethernet controller
- JESD204 and SpF controller
- UCIe die to die Interface
- DDR4 PHY memory interface
- DDR4 controller
- FPGA fabric
- General Purpose Processor (RISC-V based)

UDSM N7 Development Plan - GPP



UDSM N7 Development Plan - FPGA



Extension UDSM Technology and IP

By extending the range of IPs the UDSM technology could also become of interest to specific payload applications.

The proposed IPs are:

- General Purpose Accelerator (RISC-V based)
- High Speed Serial Link (Short Range) PHY
- RF ADC and DAC
- High Speed Digital Down Conversion
- System in Package with optical interconnect

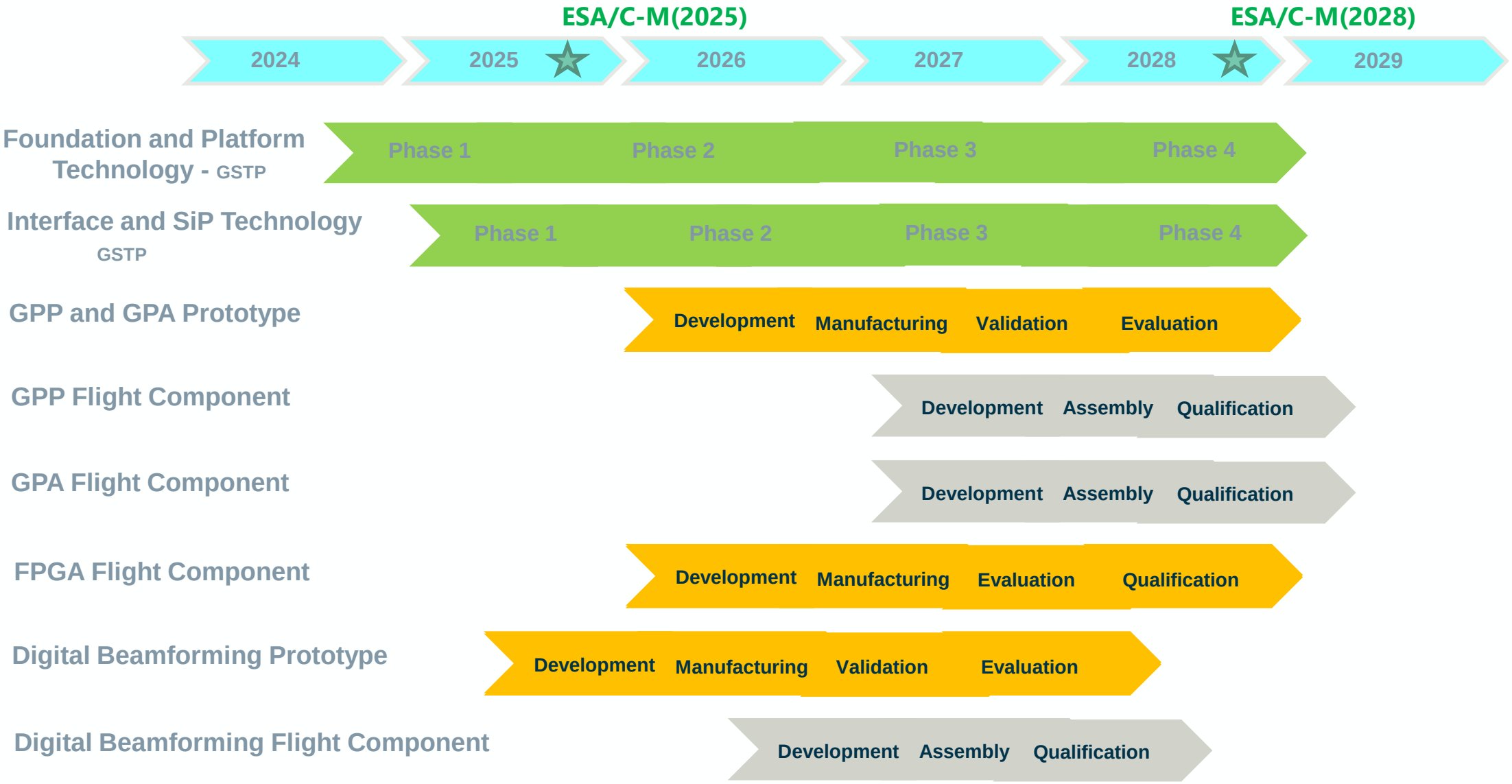
Two WG are working to determine the requirements for these payload applications

- Beamforming WG
- UDSM Processor WG

Specifically for telecommunication processors a 3rd working is proposed to be started

- Tele-communication Processor WG

UDSM Technology and Component Development Plan



UDSM Component Product Portfolio

Field Programmable Gate Array (FPGA):

- Increase portfolio of European FPGAs (RF and security)
- Develop next generation FPGA ULTRA 7
- Mature FPGA development tools

General Purpose Processor (GPP)

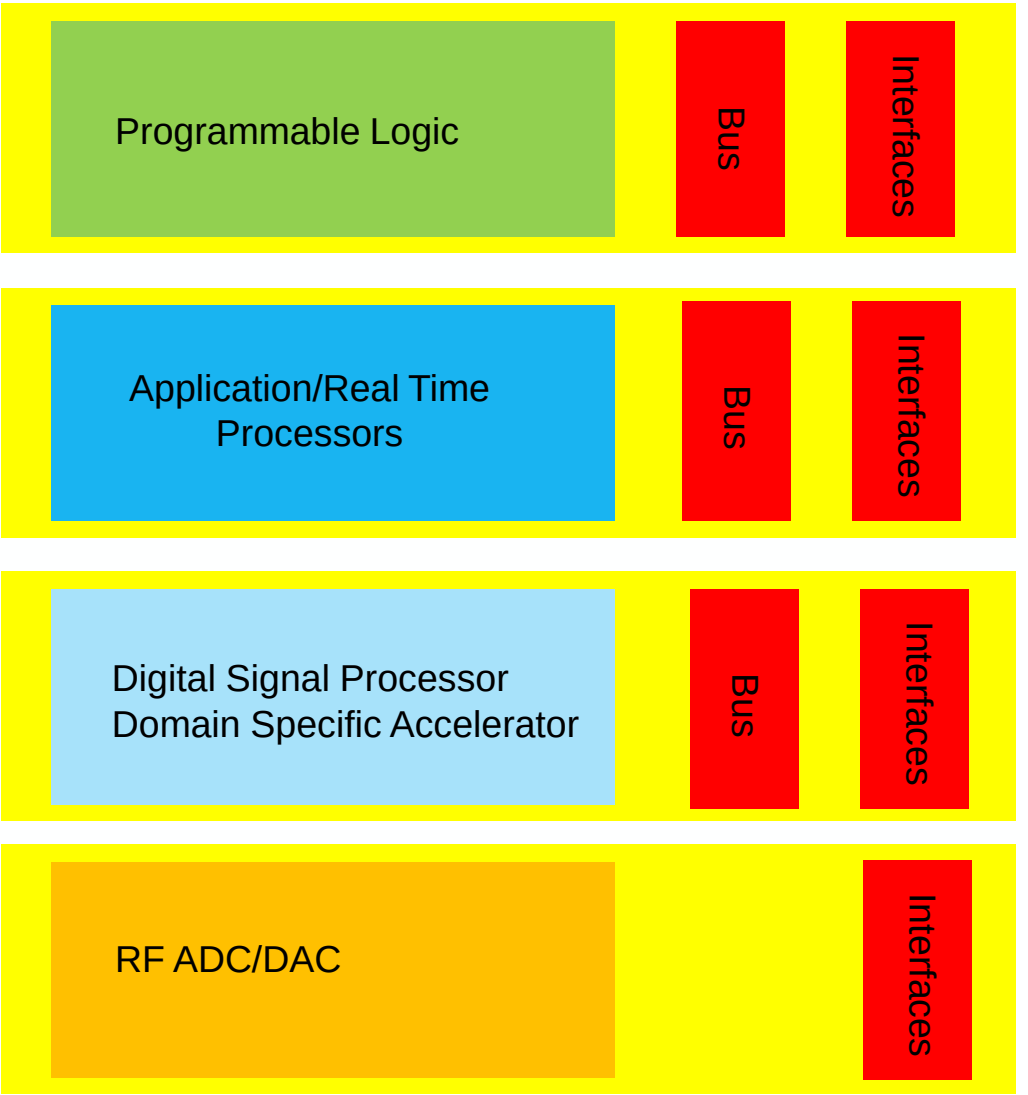
- Develop next generation European space general purpose processor, based on open-source RISC-V and exploiting N7 FinFET technology
- Develop a mature SW tool ecosystem to exploit multi-core parallel processing

General Purpose Accelerator (GPA)

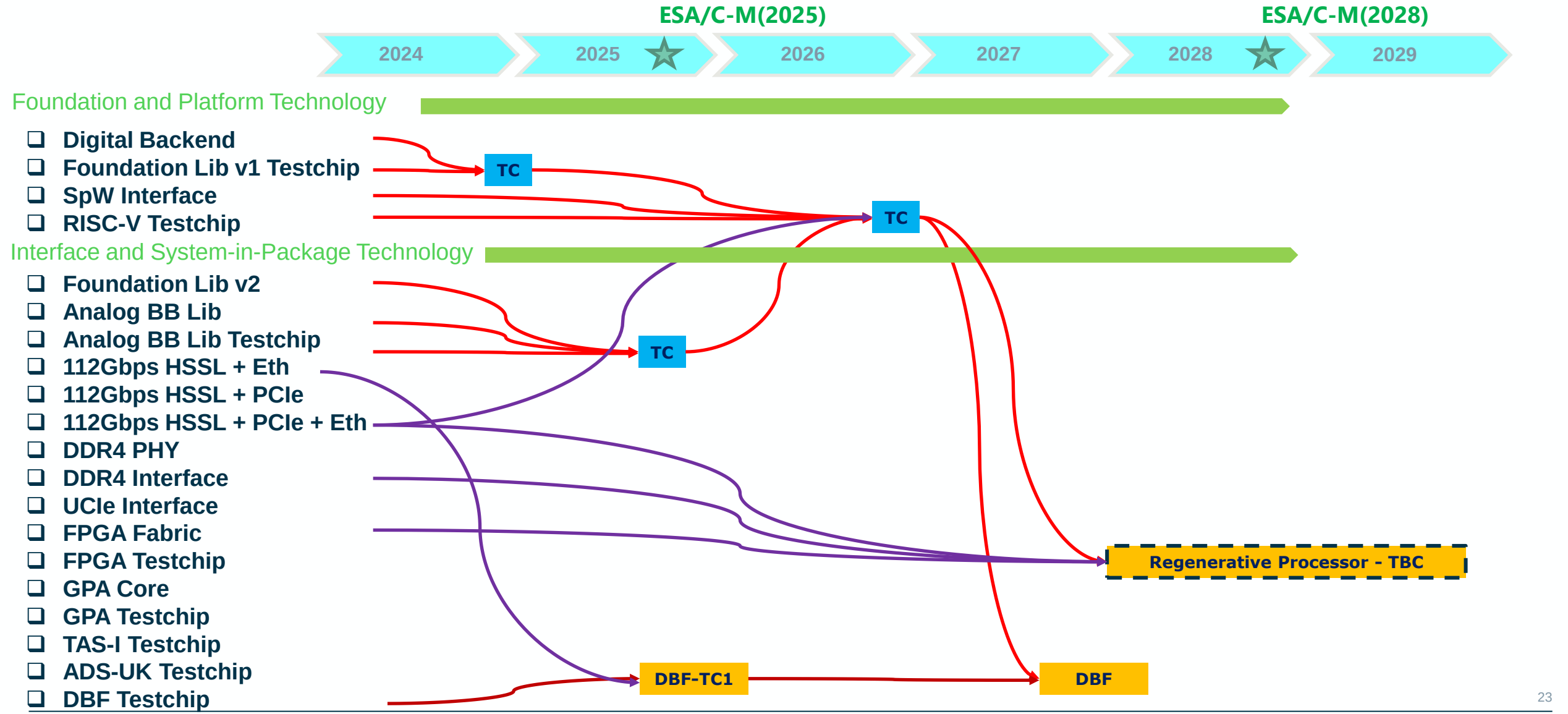
- Develop high performance European space general purpose accelerator, based on open-source RISC-V and exploiting N7 FinFET technology
- Applications: Digital Signal Processing for SAR, Digital Beamforming, AI,
- Develop a mature SW tool ecosystem to exploit multi-core parallel processing

Digital Beamforming (DBF)

- Develop antenna digital beamforming chipset based on N7 FinFET technology
- Develop low-power ADC/DAC on N7 FinFET technology
- Develop a digital beamforming processor



UDSM N7 Proposed Development Plan – DBF



Thank you

Space FPGA Users Workshop
25 – 27 March 2025
ESTEC
Noordwijk, The Netherlands

Analogue and Mixed Signal ASICs for Space
16 – 18 June 2025
Uninova
Lisbon, Portugal