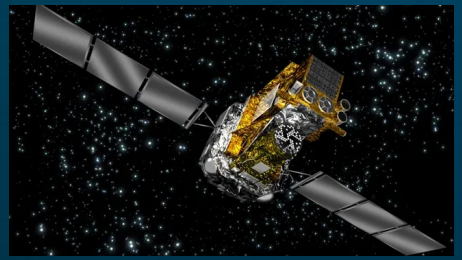
POWERING THE FUTURE OF MISSIONS CRITICAL INFRASTRUCTURE

Date: October 2024

Adoption in Growth Applications

PRECISION INSTRUMENTS



Function
- Science Instruments
- Distributed Sensors

Lattice Value
- Rad Tolerant FPGAs
- Distributed Sensors

COMMUNICATIONS

Function
- Optical Communication
- High Bandwidth

Lattice Value
- Platform Management
- Rad Tolerant

LANDERS

Function
- Supervisor
- Sensor Processing

Lattice Value
- Better SEU Resilience
- Multiple FPGA sizes

SMALL SATELLITES

Function
- Communication
- Autonomy

Lattice Value
- Motion / Motor control
- Vision Processing

Lattice Value in Aerospace & Defense

LATTICE NEXUS™

- Logic density of 17K to 100K LCs
- Max power from 100mW-1W
- 10Gb Serdes, PCIe, USB & DPHY
- SRAM based & Non-volatile options

LATTICE AVANT™

- Logic Density of 260K to 630K SLCs
- Max power from 1W-10W
- 25Gb Serdes, DDR4/5 interfaces
- Hardened Security Engine

LOWER POWER | **HIGH RELIABILITY** | **SMALLER SIZE**

Hardware Security | Enhanced Reliability | Product Longevity | Safety | SWAP-C Optimized | Extended Temperature | Ruggedized Packaging

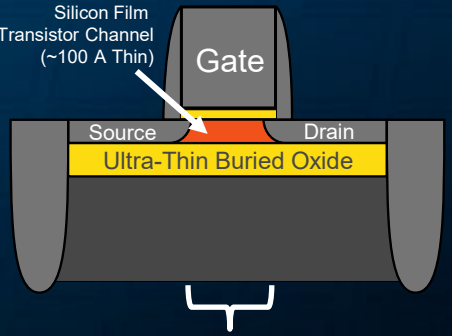
New Features, Supply Chain Resilience and Fast Cadence of Solutions

Nexus Overview

FDSOI Reliability

- Inherent SEU Resilience, no MBU
- SEE latch-up immunity to LET >100 MeV
- High Total Ionizing Dose Threshold
- SEU_{CRAM} 2.5E-8 events/bit/day [1]

Lattice FPGA in 28nm FD-SOI



Critical Area significantly reduced

Nexus Benefits

- 75% lower power than competing FPGAs
- > 3x Small form factor, no pwr sequencing
- FPGA with Instant-on (3-30ms)
- Hardened Scrubber, ECC, CRC

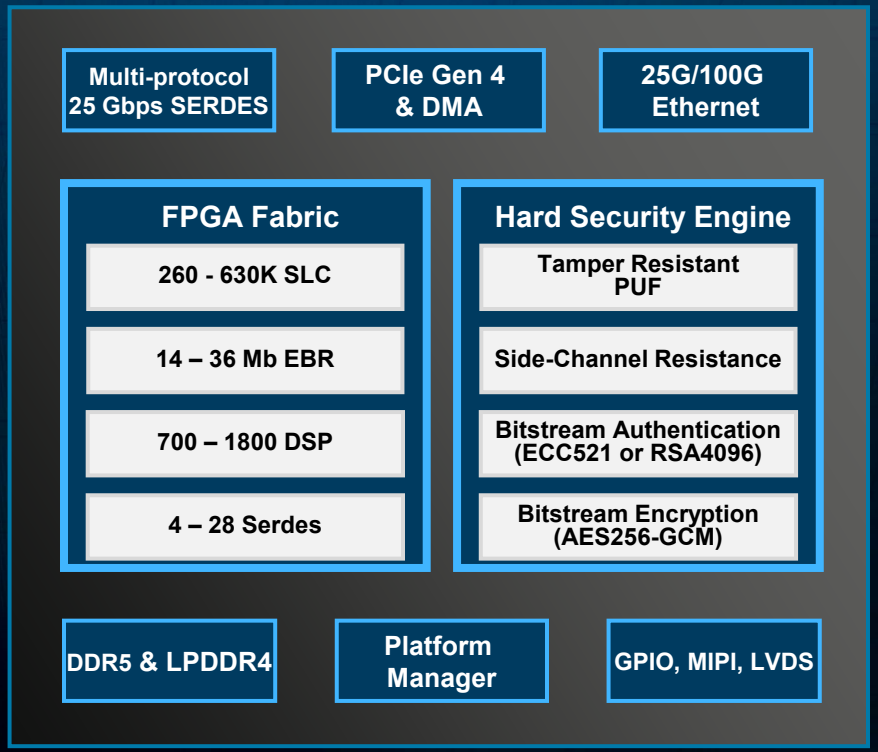
Balancing FPGA Performance for Space Missions Without Compromising Commercial Benefits

1- SEU rate (GEO, GCR, Solar Min, 100 mils Al, WC) calculated without hardened scrubber

Lattice Avant Platform: Low-power, High Reliability Mid-Range FPGA

Innovative FPGA based on 16nm FinFET

- 1st with fast, secure boot in less than 50ms
- 1st with only 3 Power Rails! No up / down Sequencing[1]
- 1st with SEL immunity



Advanced FPGA Architecture

- Timing closure up to 350 MHz
- EBR/DSP/Clocks up to 625 MHz

Innovative Architecture based on 16nm FinFET

- Fast, Secure boot in less than 50ms
- Redundant platform manager

Highest Reliability And Best-in-Class Security

- SEL immunity and hardened Scrubber
- Bitstream & User data encryption

Market Leading Power Efficiency

- Max static power less than 2W
- 3 power rails, no sequencing

1- Only if the external flash is powered with VCC greater than 1.8V, the FPGA supplies great than 1.8V must ramp up at least 300us before VCCIO1

On-Device Edge AI

Over 50M Edge AI FPGA Solutions Shipped

LATTICE SEMICONDUCTOR™

MIRAMETRIX

CONSUMER

CLIENT

AUTOMOTIVE

AVIONICS

- Human Presence Detection
- Depth Sensing / Multiple persons
- 3D Head Pose and User Position
- Face ID & Landmarks Tracking
- Eye Feature Detection & Tracking
- Gaze
- Gesture Tracking

What's next?

Optimized AI Hardware and Application Layers at low power

Sensor Fusion & Machine Learning
PoC

- Lattice Avant FPGA
  - 93K LUT4, 211 DSP, 731 EBR
  - Vision: 26K LUT, 42 DSP, 399 EBR for ML engine
  - Lidar: 21K LUT, 92 DSP, 12 EBR
  - Radar: 4K LUT, 22 DSP, 154 EBR
  - RISC-V configures processing modules and initiates operations
  - RISC-V performs post processing of ML to build bounding box
  - 50% of FPGA resources utilized, total power less than 1W