Development Status of the 2nd-generation On-board Processing Unit Using COTS GPU

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Mitsubishi Electric Corporation (MELCO)

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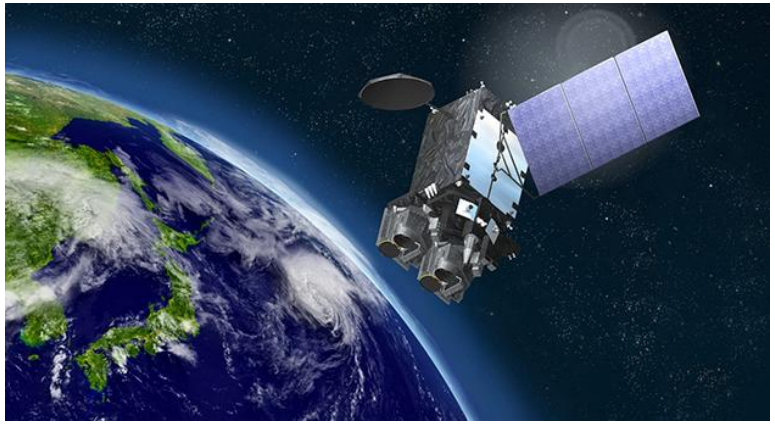
Introduction

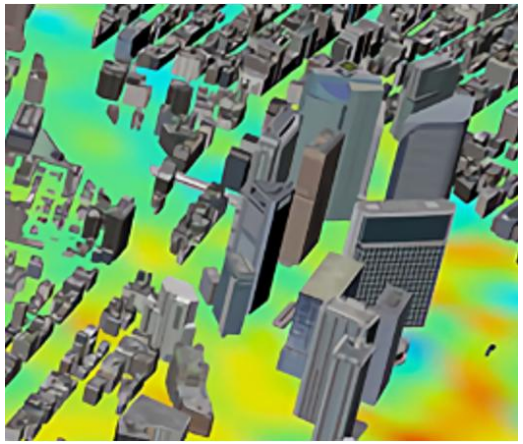
- **Many missions so far:**



GEO Satellite

LEO Satellite

Lander



Ground

Data Handling

- CCSDS TC/AOS
- SpaceWire
- 1553B…

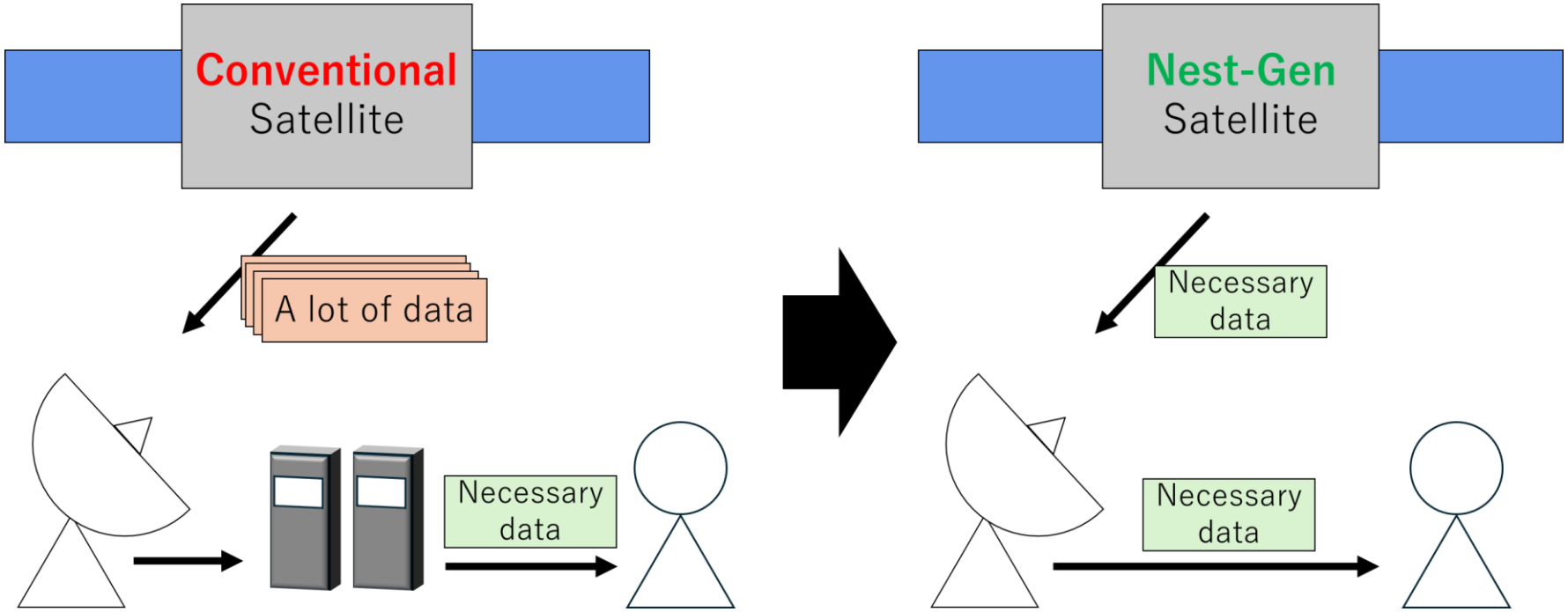
Data Processing

- SAR imaging
- Optical imaging
- Target detecting
- Template matching …

Introduction

- **Background:**
  - —Increasing the amount of payload data from advanced satellite sensors.
  - —Growing user demand for faster data delivery.
  - —Evolution of semiconductor technology.

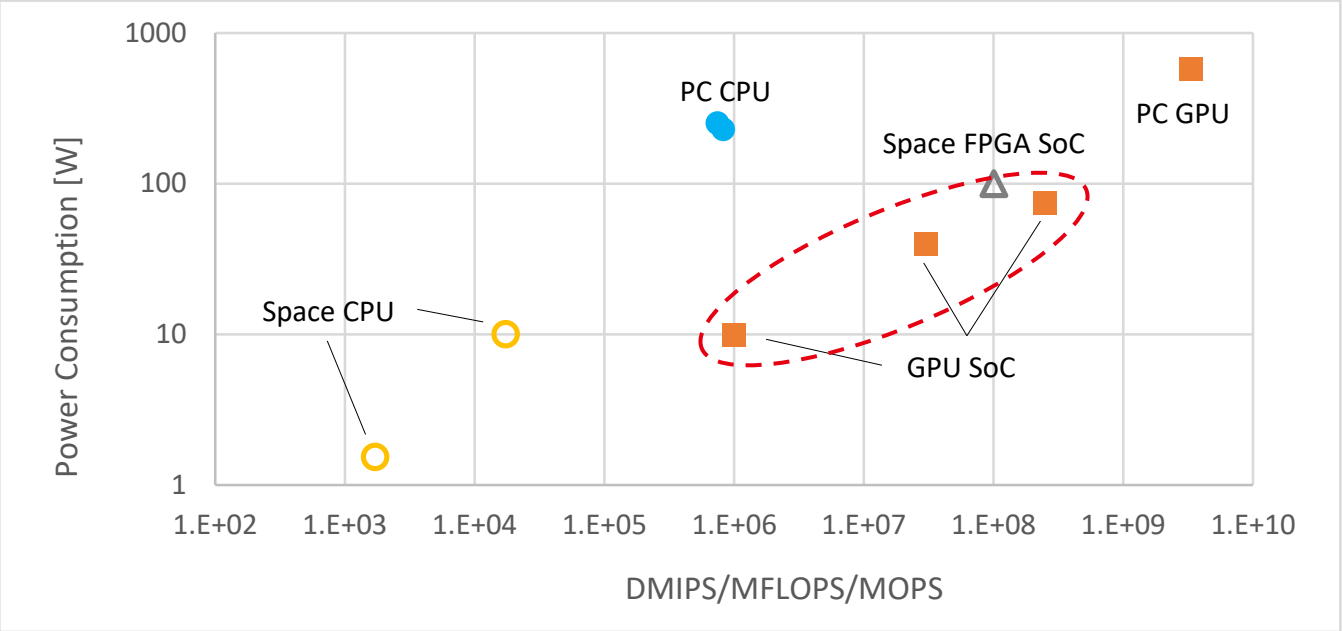
- **Solution:**
  - —Process & Compress raw data in orbit.
  - —Downlink only necessary data.
  - —Overcome limited downlink bandwidth.



Introduction

- **Problem:**
  - Space-grade CPUs lack sufficient performance for these demanding tasks.
  - PC CPUs and PC GPUs have too large power consumption.

- **Our Approach: COTS GPU-SoC**
  - Achieving both high performance and low power consumption.
  - Easy to reconfigure or update in orbit.
  - Low procurement costs.



* The evaluated processors are as follows. Those for space are underlined (shown in white in the diagram).

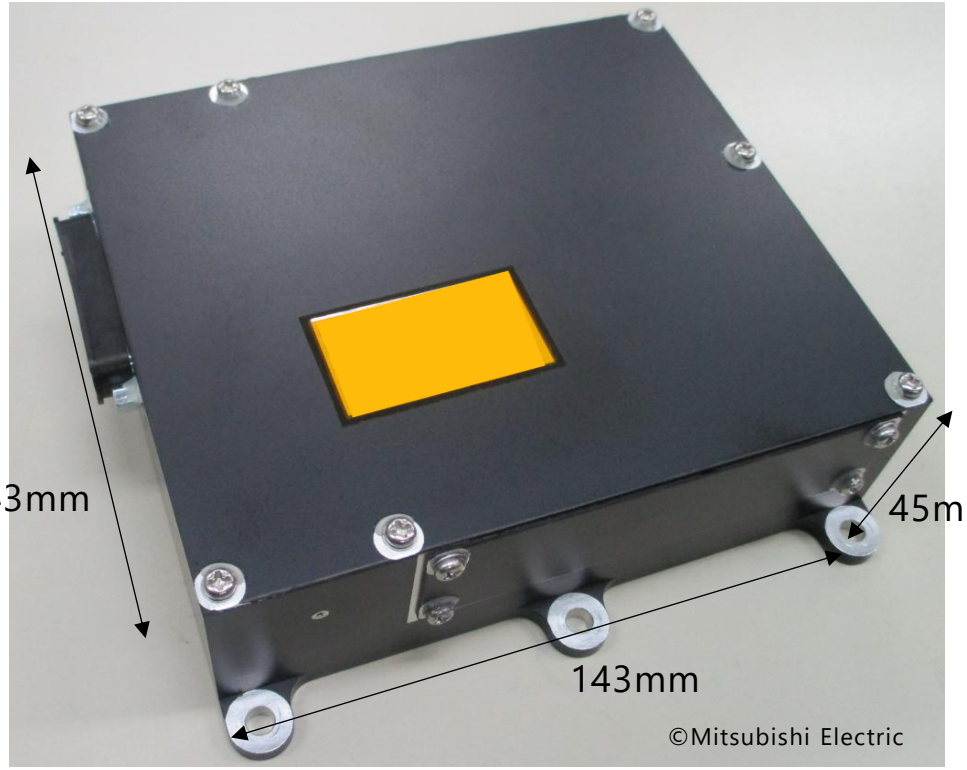
CPU：Ryzen 9 7950X, Intel i9-14900KF, HPSC, GR740

GPU：GeForce RTX 5090, Jetson AGXi Orin, Jetson AGX Xavier, Jetson TX2i

FPGA：Versal VC1902

Our History: 1st to 2nd Generation

- **Since 2020:**
  - —Developing COTS GPU for On-board Processing.
- **1st-Gen Achievement: GEMINI**
  - —Will be launched and demonstrated in JFY2025.
- **Mission Objectives:**
  - —SAR processing on GEMINI simulated data.
  - —Target detection with AI.
  - —On-orbit software updates.
  - —Investigation SEEs during the one-year mission period.
  - —Measuring MTBF in space environment.



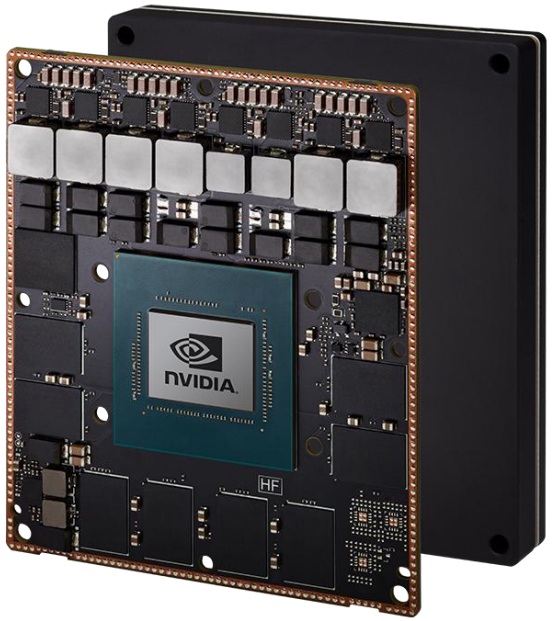
RAISE-* (**RA**pid **I**nnovative payload demonstration **S**atellit**E**-*):
a satellite for on-orbit demonstration themes selected in the "Innovative Satellite Technology Demonstration Program".

GEMINI: cots **G**PU based **E**dge computing for **MI**ssion systems utilizing model based systems engi**N**eer**I**ng)

Our History: 1st to 2nd Generation

Developing the 2nd-Generation since 2022.

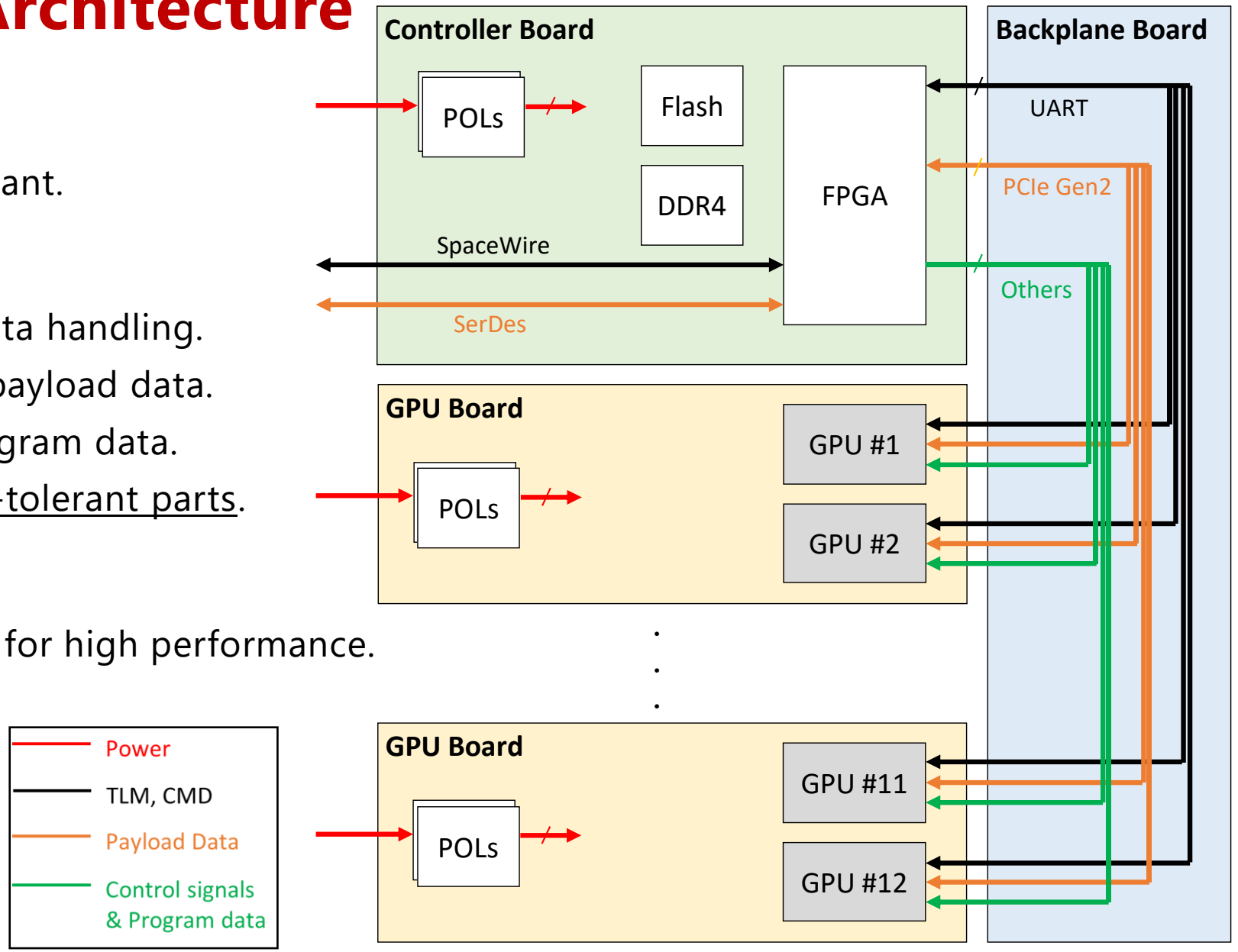
- **2nd-Gen Adopted Device:**
  - —NVIDIA Jetson AGX Xavier Industrial (JAXi)
- **Key Features:**
  - —Highly integrated module (SoC, DRAM, flash, power, clock, etc.).
  - —High-speed interfaces (e.g., PCIe for > several Gbps).
  - —Enables high performance with low design cost.



https://www.nvidia.com/ja-jp/autonomous-machines/embedded-systems/jetson-agx-xavier/#

2nd-Gen System Architecture

- **Standard:**
  - 6U SpaceVPX (VITA78) compliant.
- **Controller Board:**
  - FPGA for system control & data handling.
  - DDR4 memory for buffering payload data.
  - Flash memory for storing program data.
  - Implemented using radiation-tolerant parts.
- **GPU Boards:**
  - Utilize COTS/low-grade parts for high performance.
  - 2 JAXi modules per board.
  - Total of 6 boards (12 JAXis).



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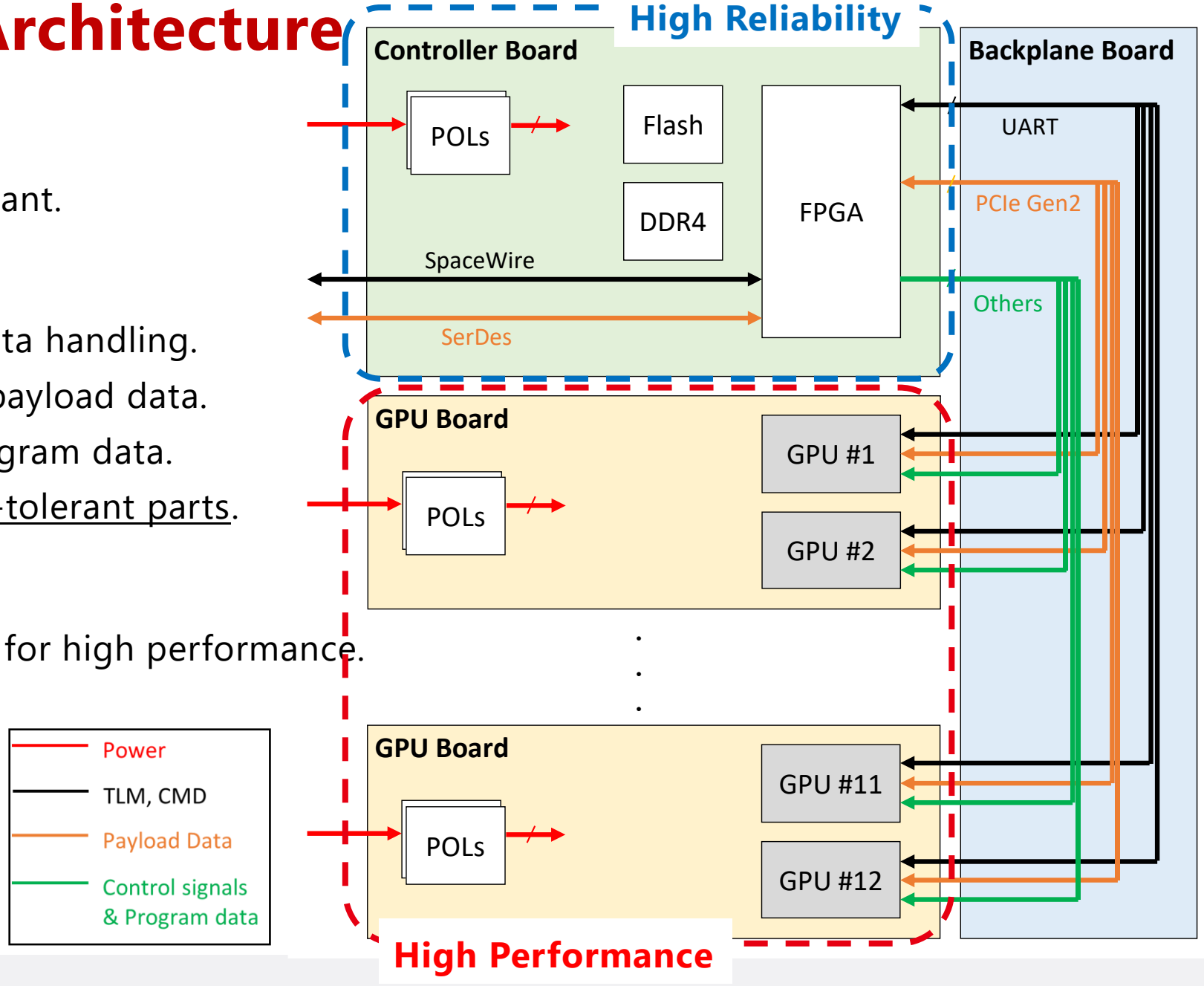
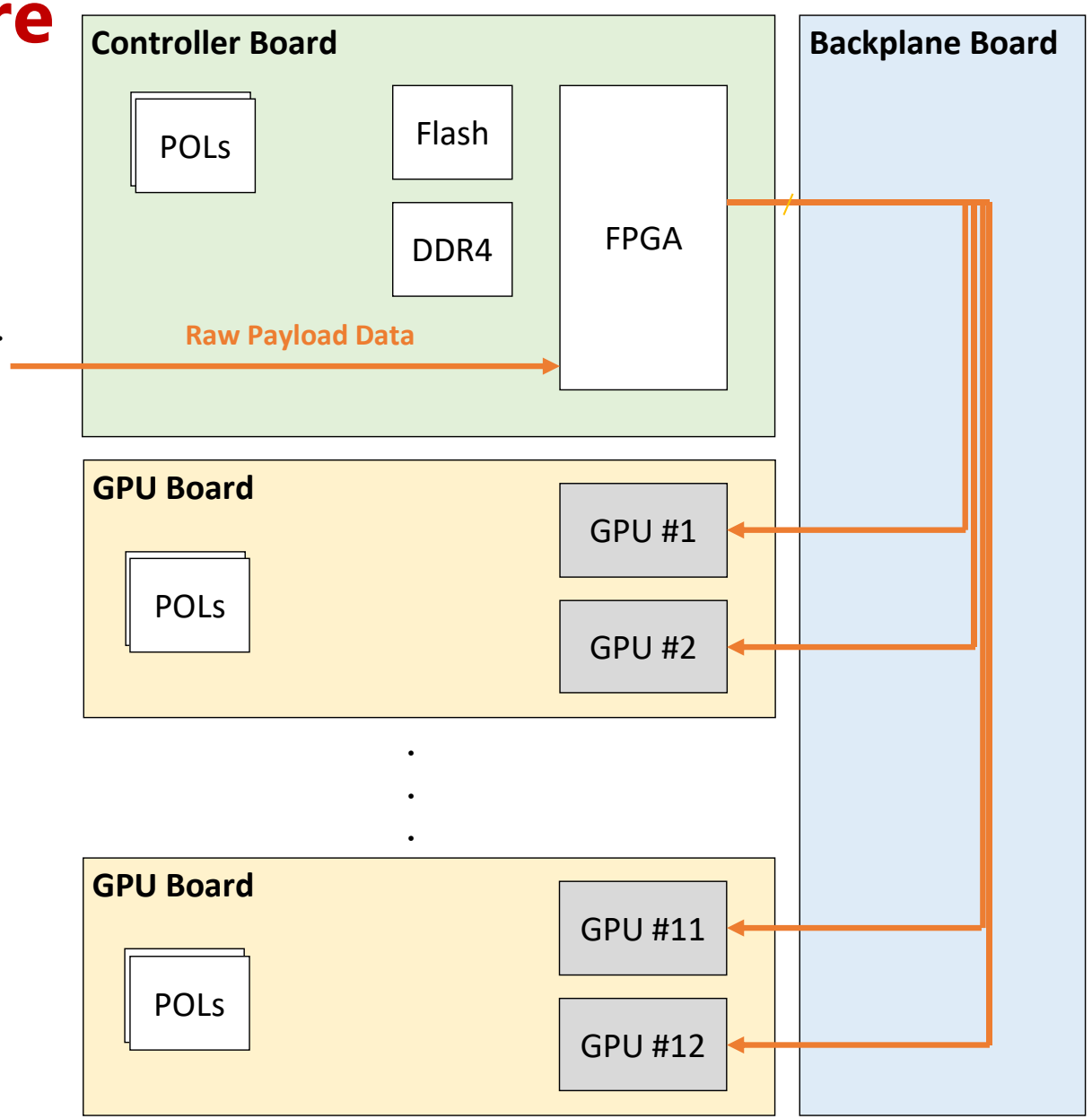


2nd-Gen System Architecture

<Data Processing Flow>

1. **Distribute:**
   FPGA distributes raw data to each GPU via PCIe.
2. **Process & notify:**
   GPUs process data in parallel,
   and GPUs notify FPGA of completion via UART.
3. **Request:**
   FPGA requests the processed data from GPUs.
4. **Send:**
   FPGA sends the processed data
   to external recorder.



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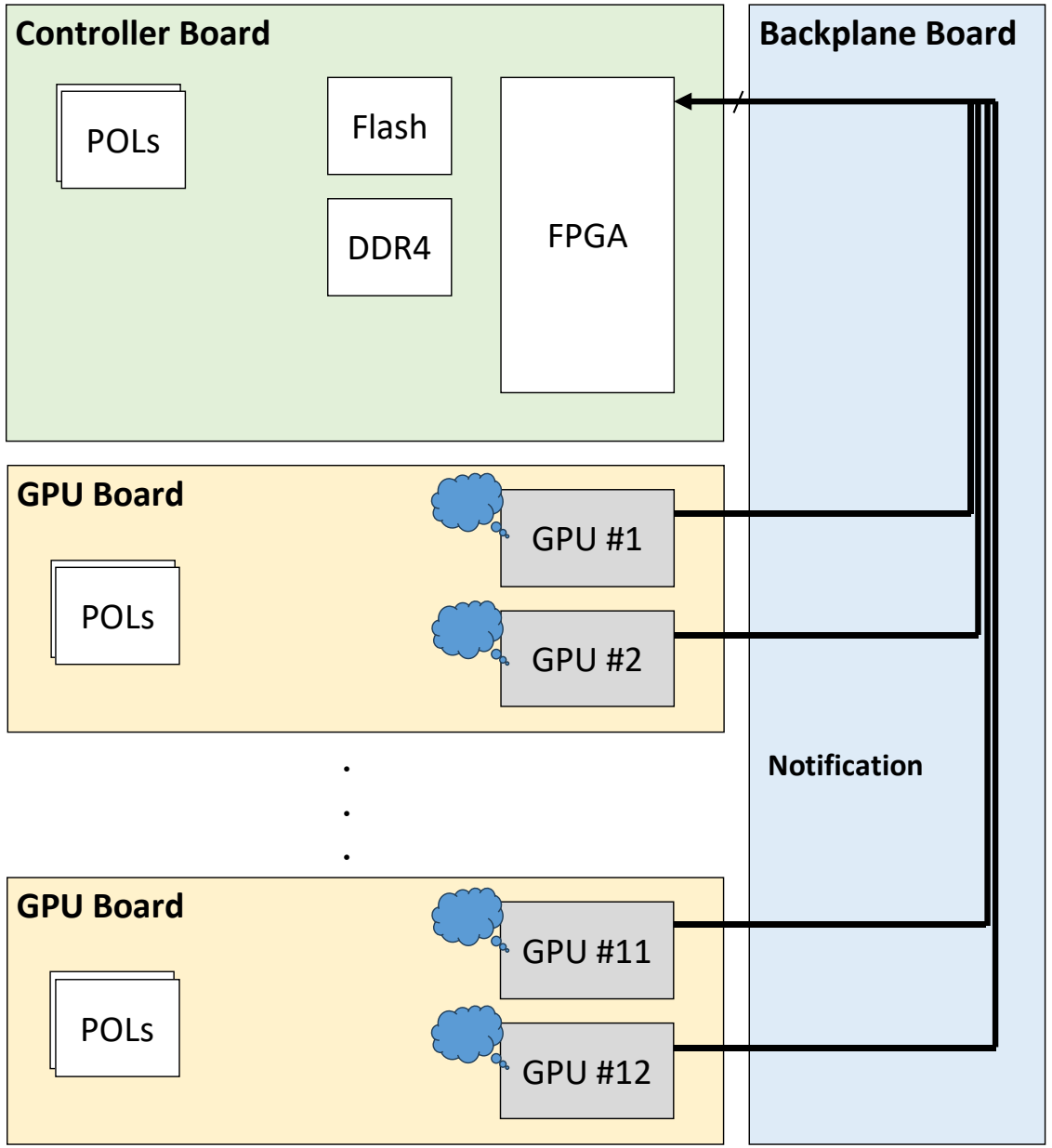

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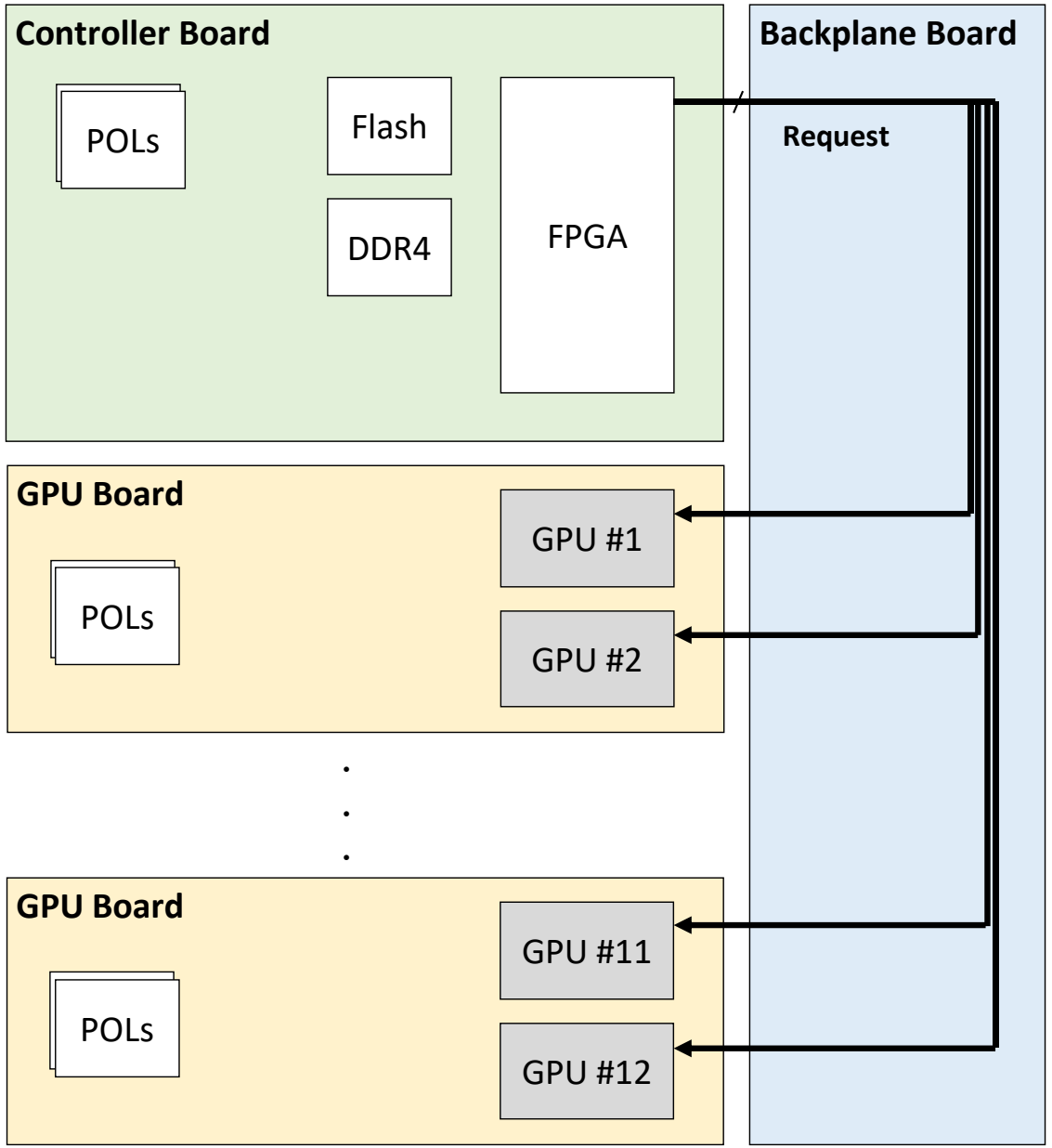

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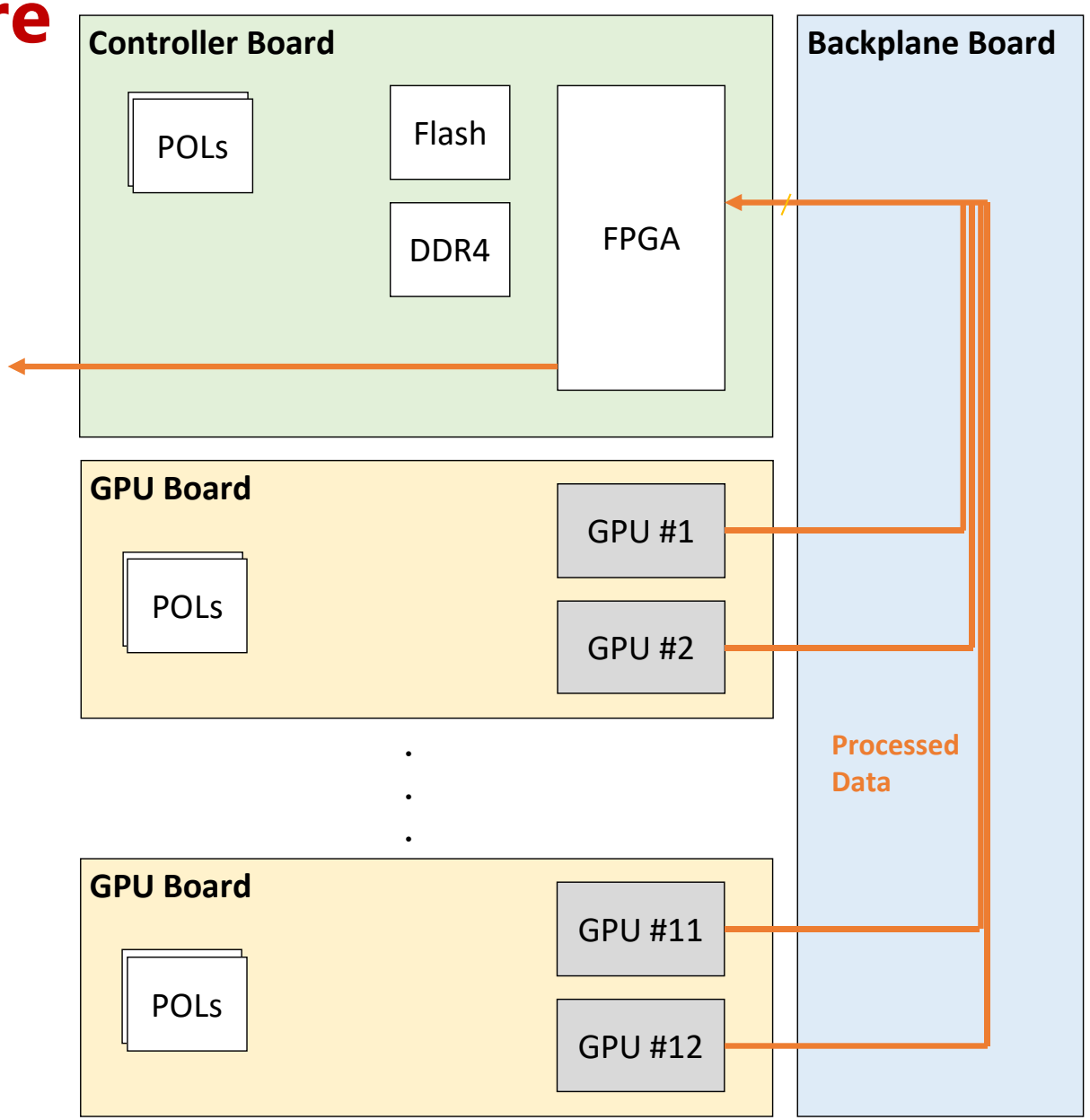
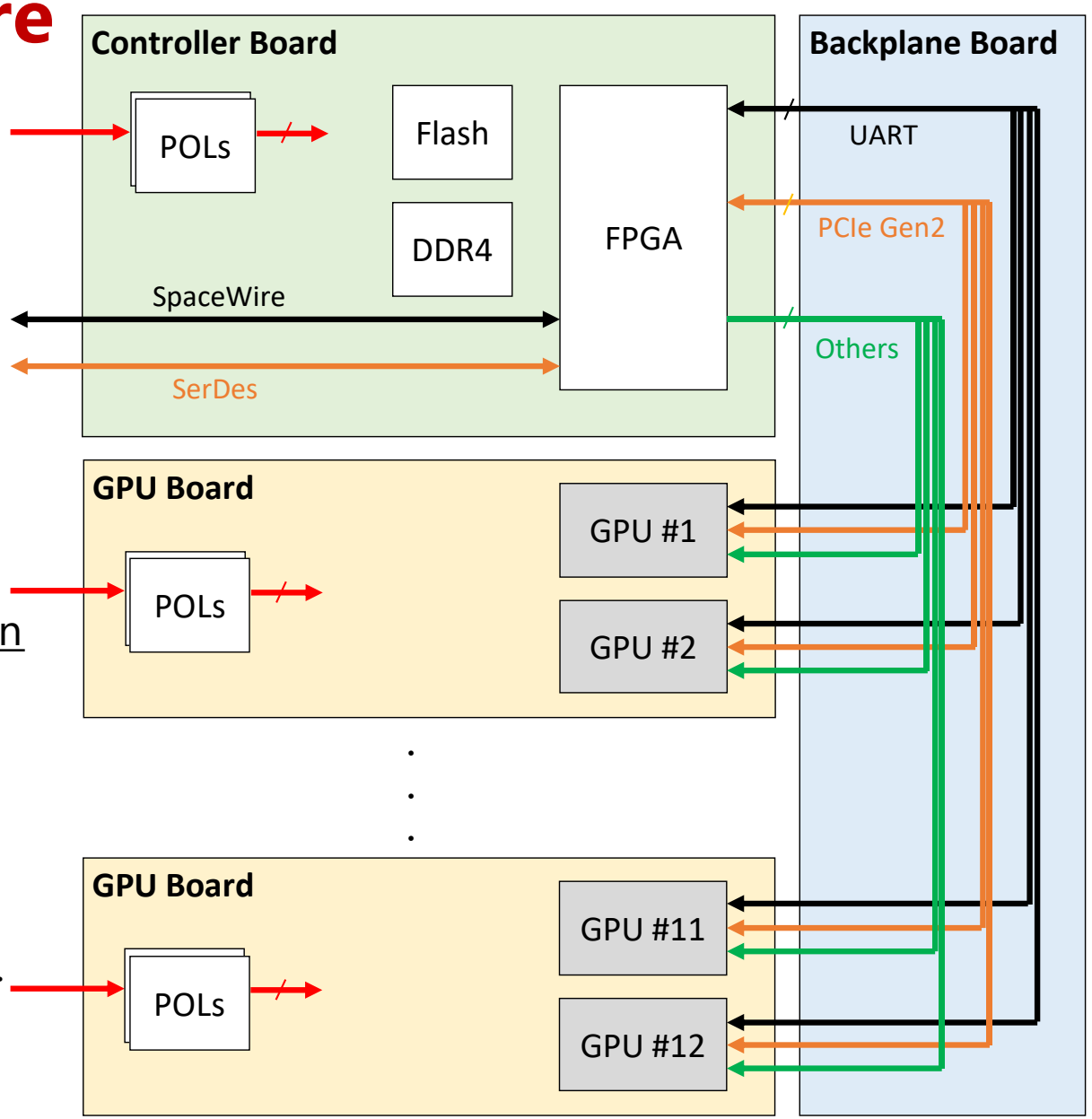


2nd-Gen System Architecture

<Radiation Hardening (1): SEL>

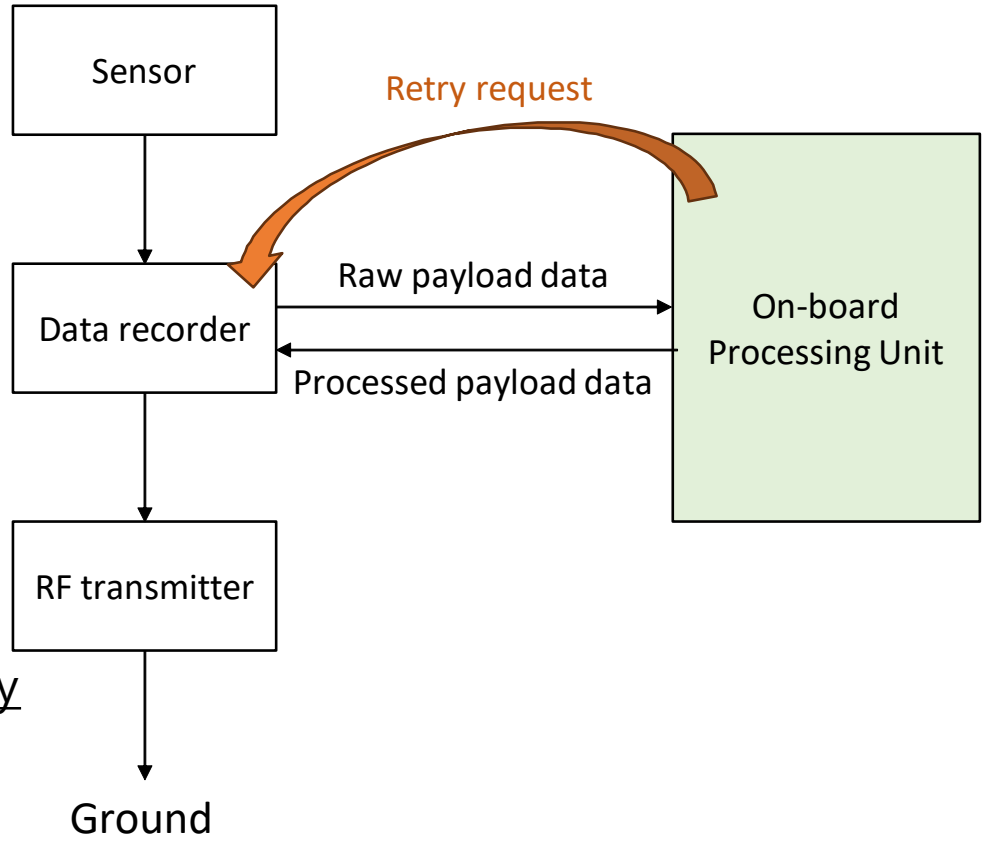
- **Challenge:**
  - —Single Event Lath-up (SEL):
    A destructive overcurrent failure.
- **Our Solution:**
  - —**Isolation:**
    POL converter's overcurrent detection/shutdown function isolates the faulty module and prevents failure propagation.
  - —**Redundancy:**
    Up to 10 GPUs can be operated in parallel and 1 spare GPU board (2 modules) on standby.



2nd-Gen System Architecture

<Radiation Hardening (2): SEU/SEFI>

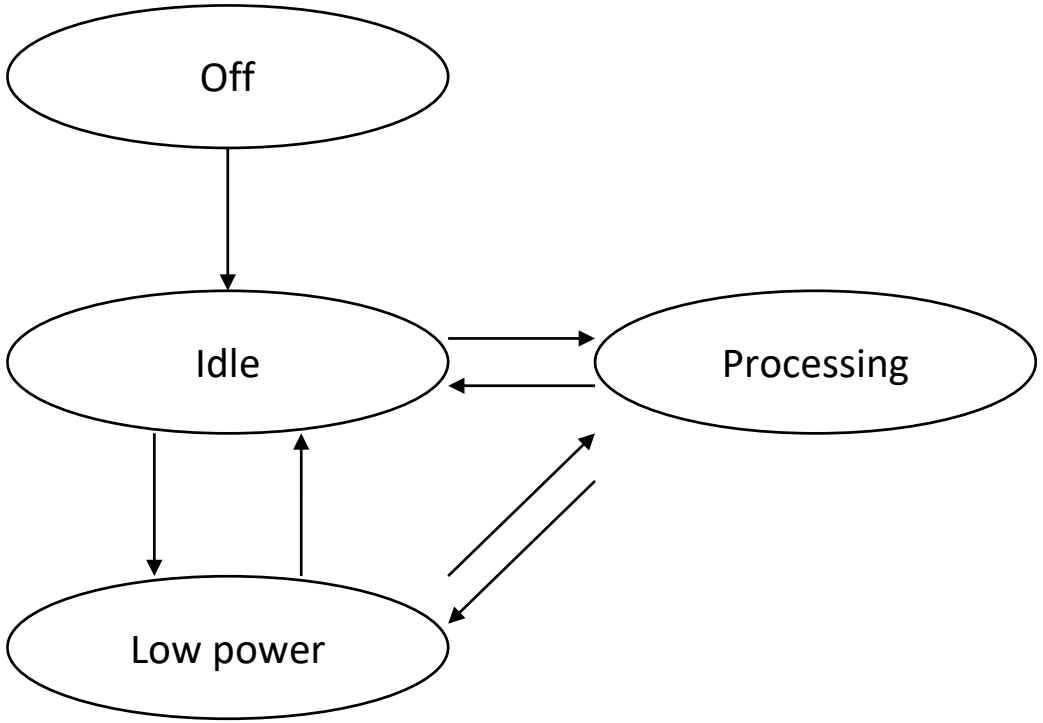
- **Challenge:**
  - Single Event Upset (SEU) & Functional Interrupt (SEFI): Transient errors during processing.
- **Our Solution:**
  - **Retry Mechanism:**
    - Retry request is sent to an external data recorder.
    - Power cycling (if necessary).
  - **Program Data Integrity:**
    Program data is stored in radiation-tolerant flash memory on the controller board, and deployed from FPGA to GPUs.



2nd-Gen System Architecture

<Running modes>

This system has four running modes.

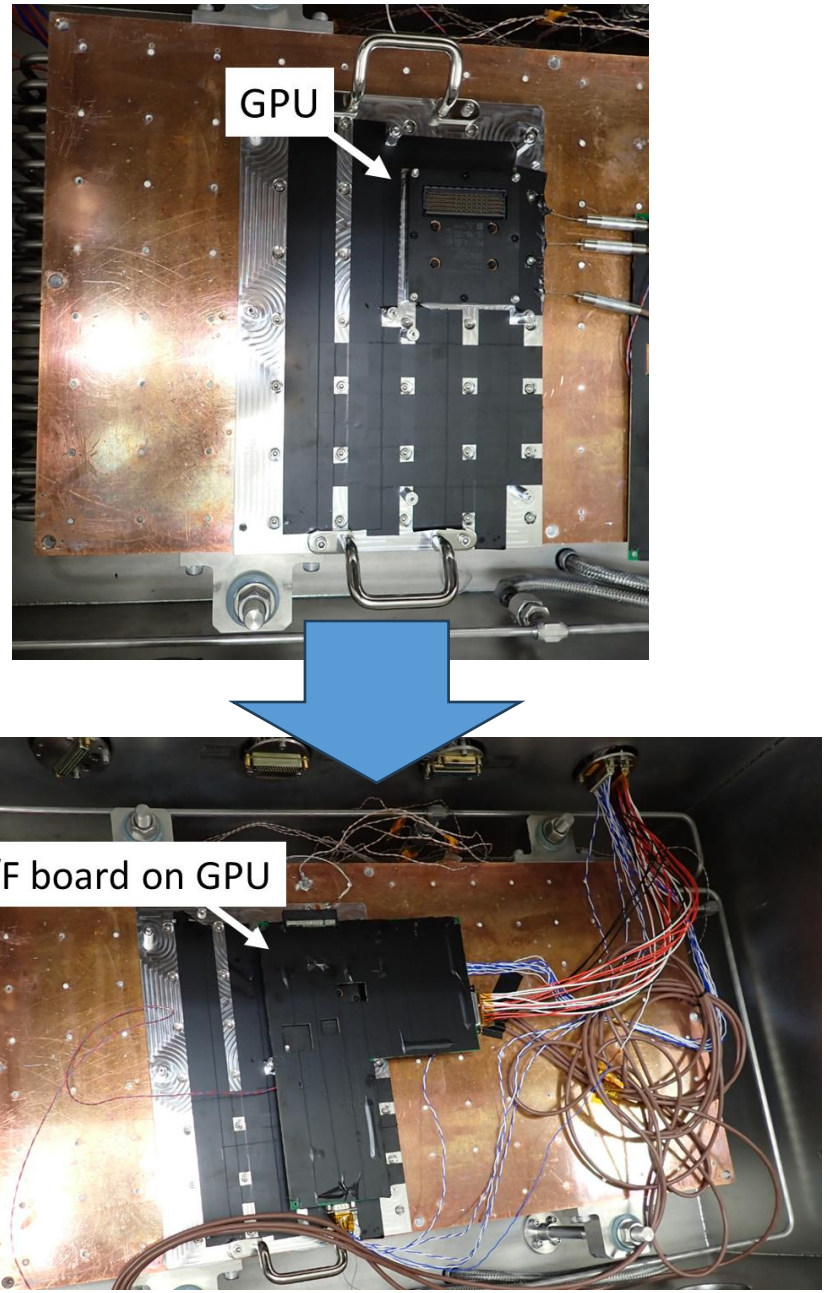


Mode	Power consumption
Off	< 0.1 W
Idle	< 80 W
Processing	< 500 W
Low power	< 10 W

※Off mode is reachable from any mode.

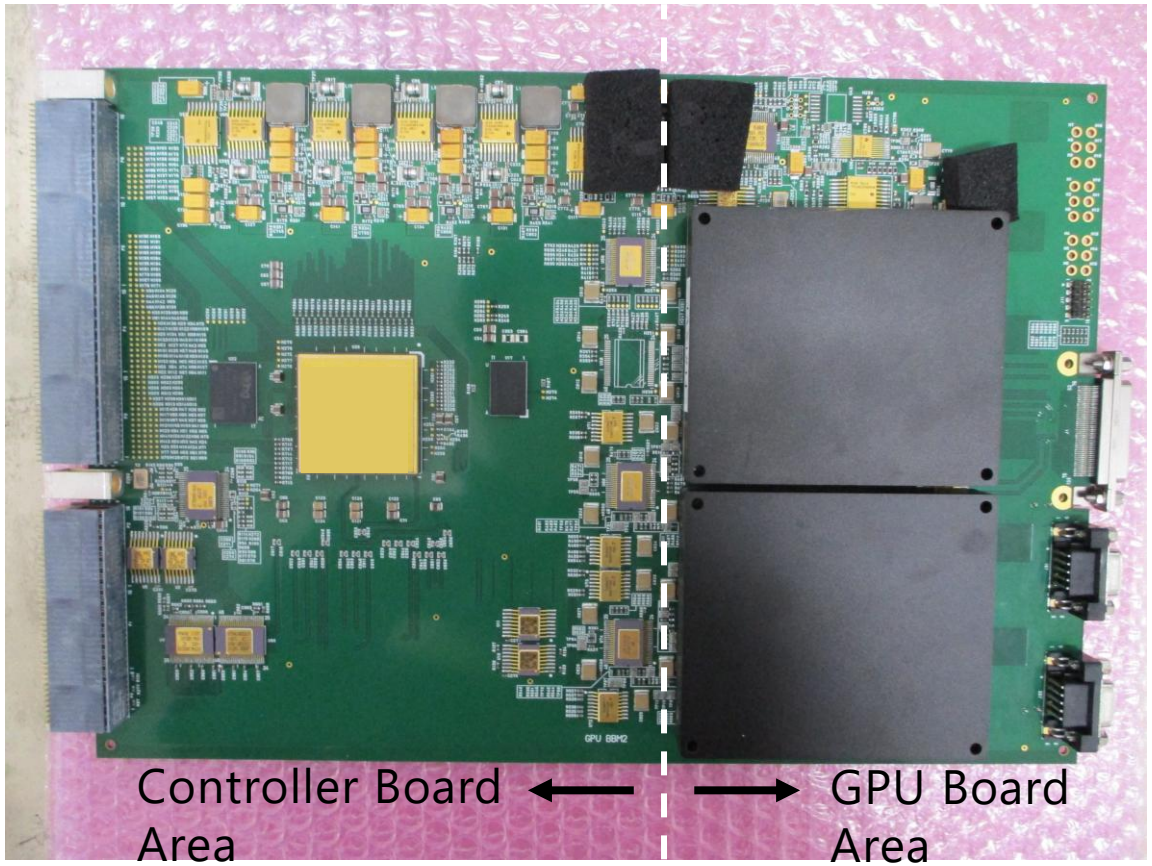
Environmental Tests for GPU

- **Tests Performed:**
  - —Vibration Test.
  - —Shock Test.
  - —Thermal Vacuum Test.
- **Test Program (operated periodically):**
  - —AI inference.
  - —Health checks of memory and UART/PCIe interfaces.
  - —Logging temperature and CPU/GPU usages.
- **Results:**
  - ✓ No damage and failures in all tests.
  - ✓ Stable operation during thermal vacuum tests.
  - ✓ Internal temperatures remained within specified limits.



Bread Board Model (BBM)

Completely developed BBM and conducting the functional performance tests.



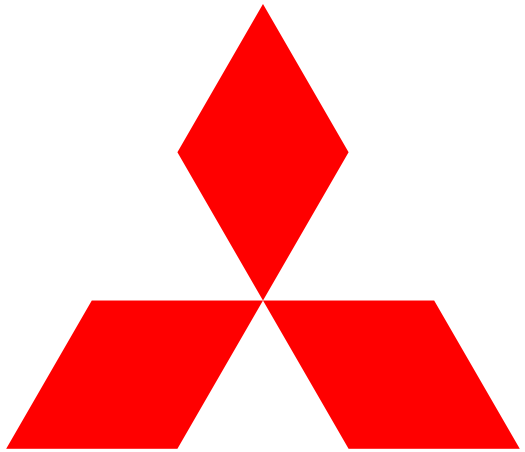
Main Functions	Verification Results
GPU Power Control	✓ Worked normally during both power-on/off sequences.
Telemetry/Command Control	✓ Processed normally.
Payload Data Handling	✓ Proper data handling and PCIe DMA with two GPUs.
Program Data Deployment	➢ Ongoing.

Summary

- **Developing a 2nd-Gen On-board Processing Unit using NVIDIA JAXi COTS GPU.**
- **Environmental tolerance confirmed:**
  GPU module passed vibration, shock, and thermal vacuum tests.
- **Main Functions Verified:**
  BBM tests showed satisfactory results for power control, T&C, and data handling.
  Verification of program data deployment function is ongoing.

Future Works

- **Execute computationally intensive tasks and evaluate processing time/latency.**
- **Conduct thermal cycle test to assess system lifetime.** **←Ongoing.**
- **Investigate strategies for managing multiple GPU's heat.**



MITSUBISHI ELECTRIC

Changes for the Better

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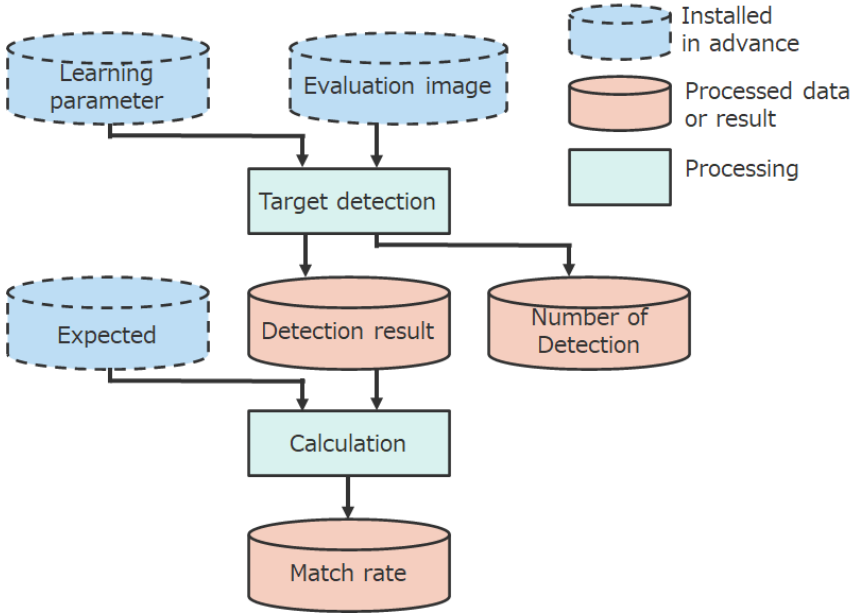
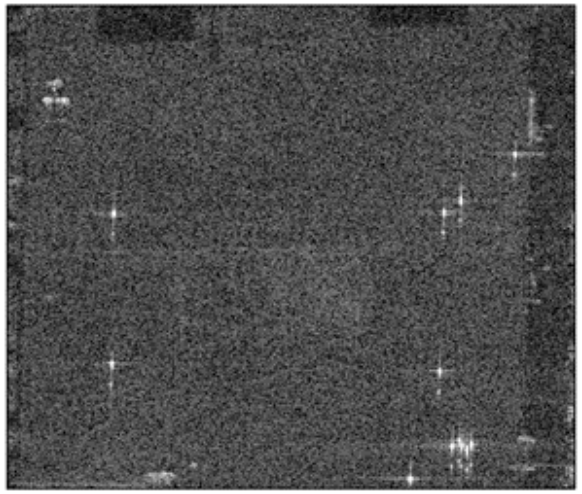
Appendix

GEMINI S/W

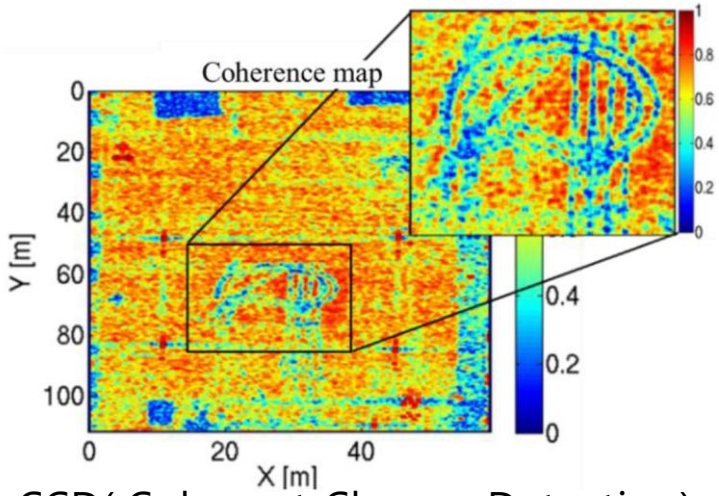
- **SAR Processing**
- **Target Detection**
- **Update Learning Parameter**



Target detection flow



SAR Image



CCD(:Coherent Change Detection) Image

Expected detection result