MEMORY SYNCHRONIZATION IN MULTI-PROCESSING SYSTEMS FOR THERMAL OPTIMIZATION IN SATELLITE PAYLOADS

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AGENDA

MOTIVATION: THERMAL CHALLENGES IN SMALL SATELLITES

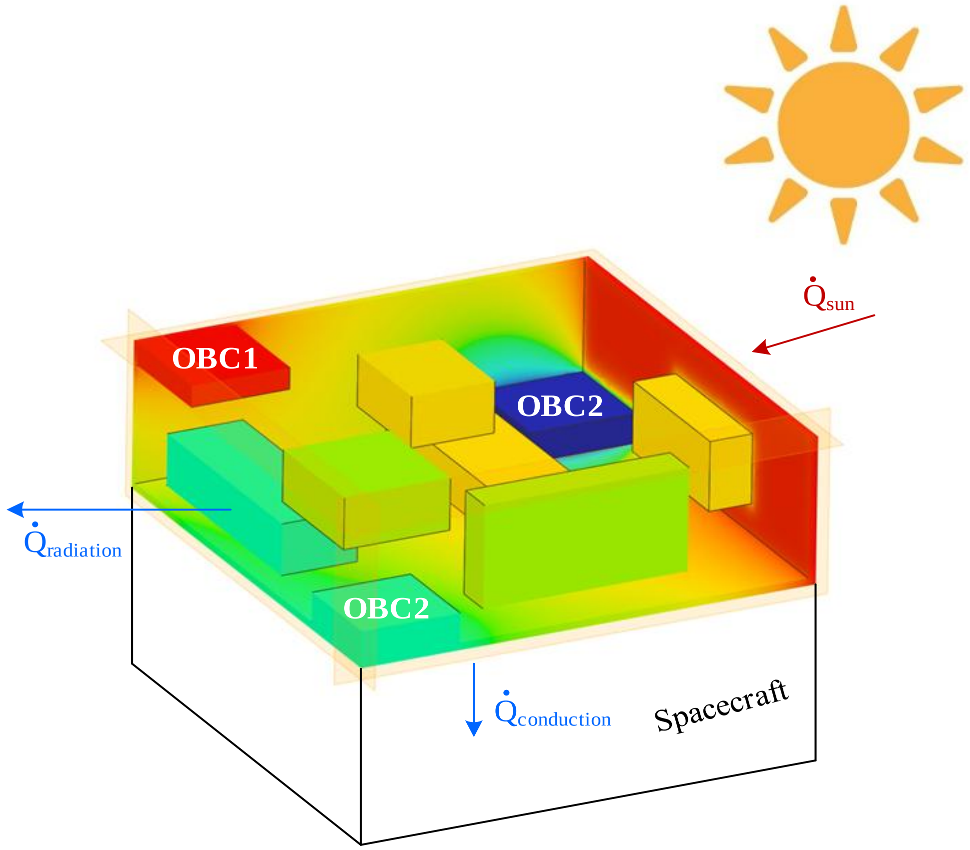
Thermal Control under Tight Power Constraints

- Dense electronics ⟹ significant heat, limited dissipation
- Heaters inefficient under small-sat power budgets
- Tiny temperature shifts ⟹ drift & image degradation
- Recent solutions: TECs, hybrid, cryocoolers (Bennett 2023, Ortiz 2024)
- Demand: low-power, high-precision thermal control

PLUTO CONCEPT

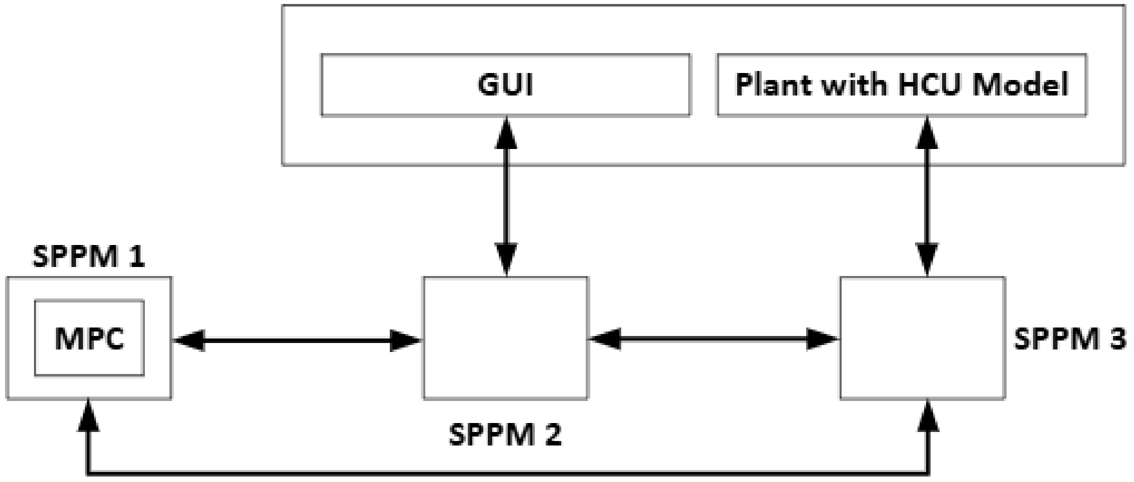
Using Redundant Processors for Thermal Balance

- Redundant units ⟹ not only backup, but active heat sources
- Controlled task activation balances payload temperature
- No extra heaters or hardware required
- Heat routing through predefined thermal paths
- Enables stable equilibrium and efficient subsystem layout



CONTROL SCHEME OVERVIEW

- Traditional control ⟹ reactive, heater-based, power-intensive
- PLUTO uses MPC for proactive thermal regulation
- MPC embeds physics-based model to forecast and minimize gradients
- Distributed processing across redundant SPPMs
- Synchronized memory ensures consistent global state

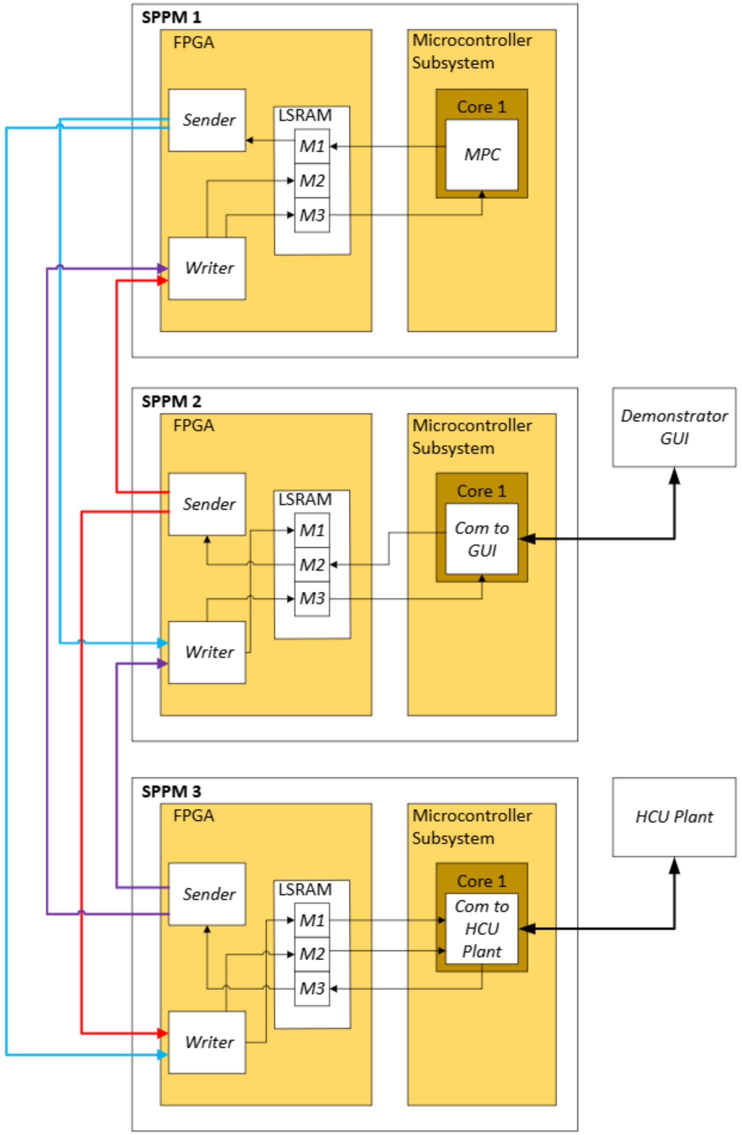


Smart Power and processing Module (SPPM)

- PolarFire SoC on each board
- Three dual-ported SRAM blocks (1024 x 32 bit each)
- Unidirectional UART (RS-485) links with 3 Mbit/s Baud rate
- Deterministic hardware structure – no shared cache

Interrupt-Driven Periodic Synchronization

- 100 ms timer interrupt triggers each cycle
- Fixed packet structure
- Dedicated unidirectional links ⟹ no collisions
- Timestamp in first register



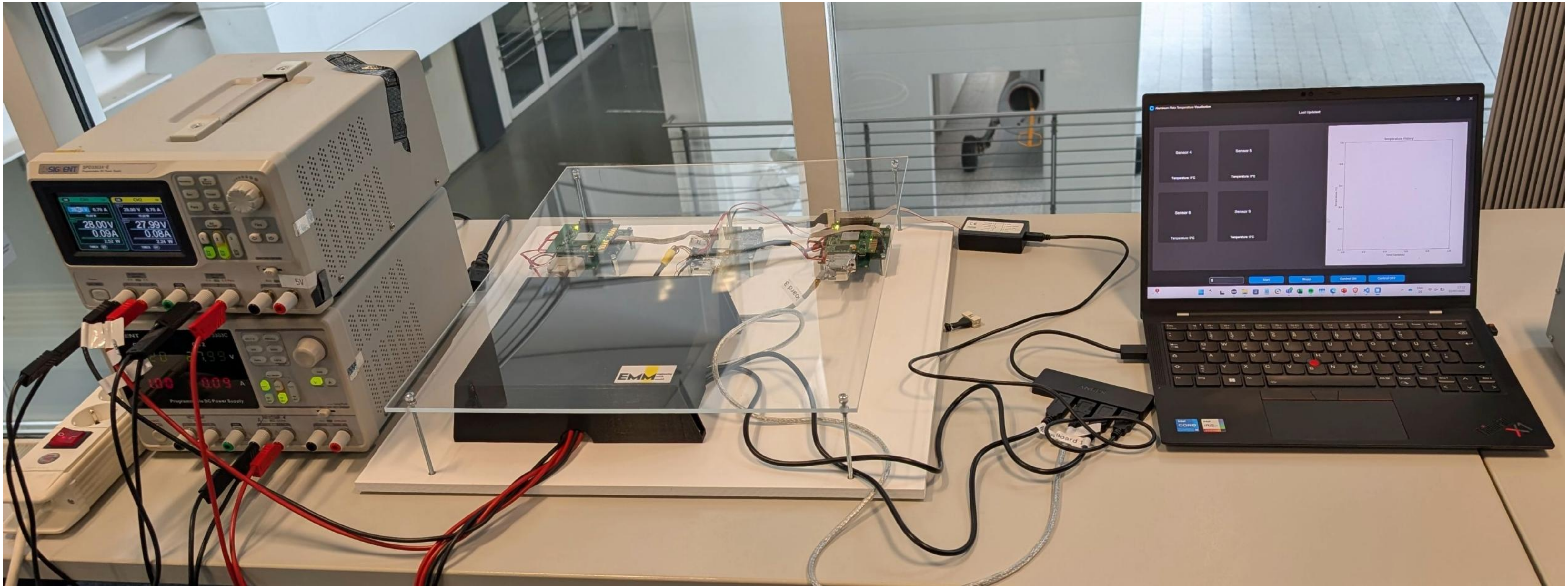
DETERMINISM VS. CACHE-COHERENT SYSTEMS

Design Priorities: Predictability vs. Programmability

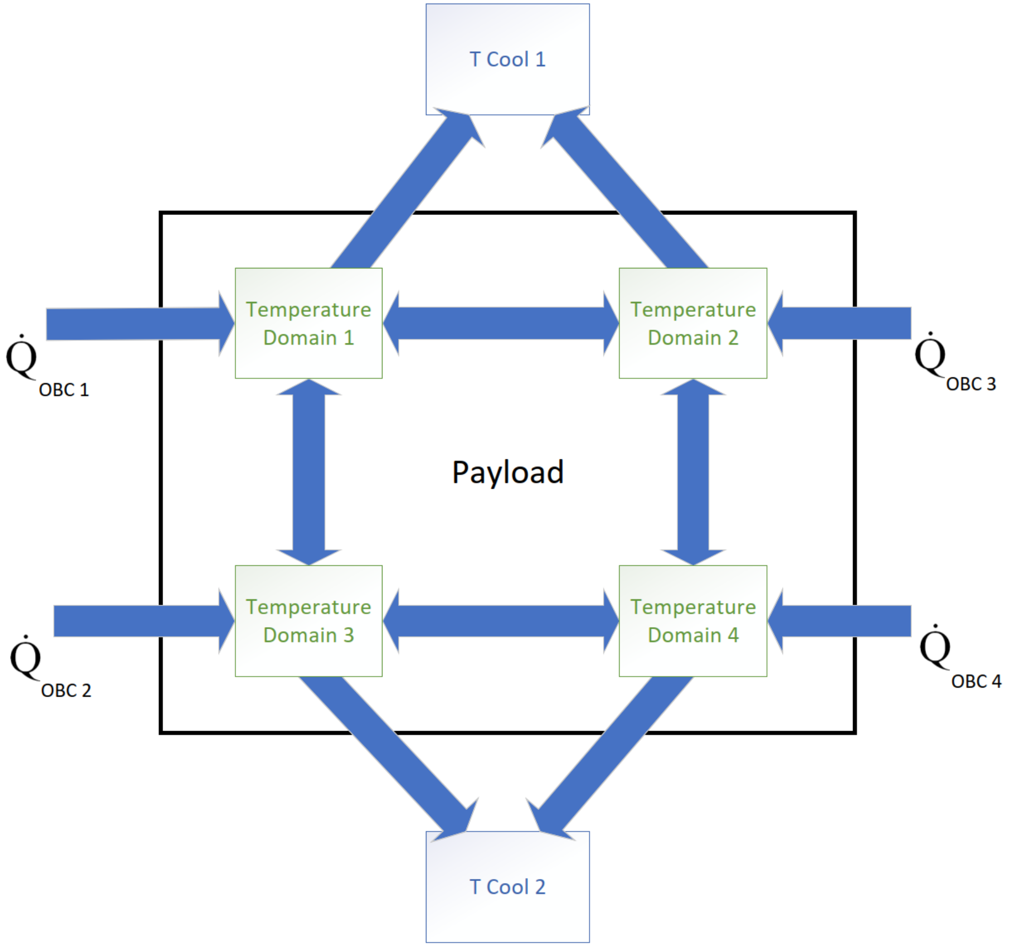
PLUTO synchronization	Coherent scratchpads (Yang 2014)
Periodic timer trigger	Event/driven, dynamic access
Fixed memory partitions	Shared cache domains
Minimal protocol overhead	Higher latency, flexible consistency models
Deterministic timing for FPGA SoCs	General-purpose programmability

Chosen for satellite payloads ⇒ **temporal predictability and reliability**

EXPERIMENTAL DEMONSTRATOR



THERMAL MODEL



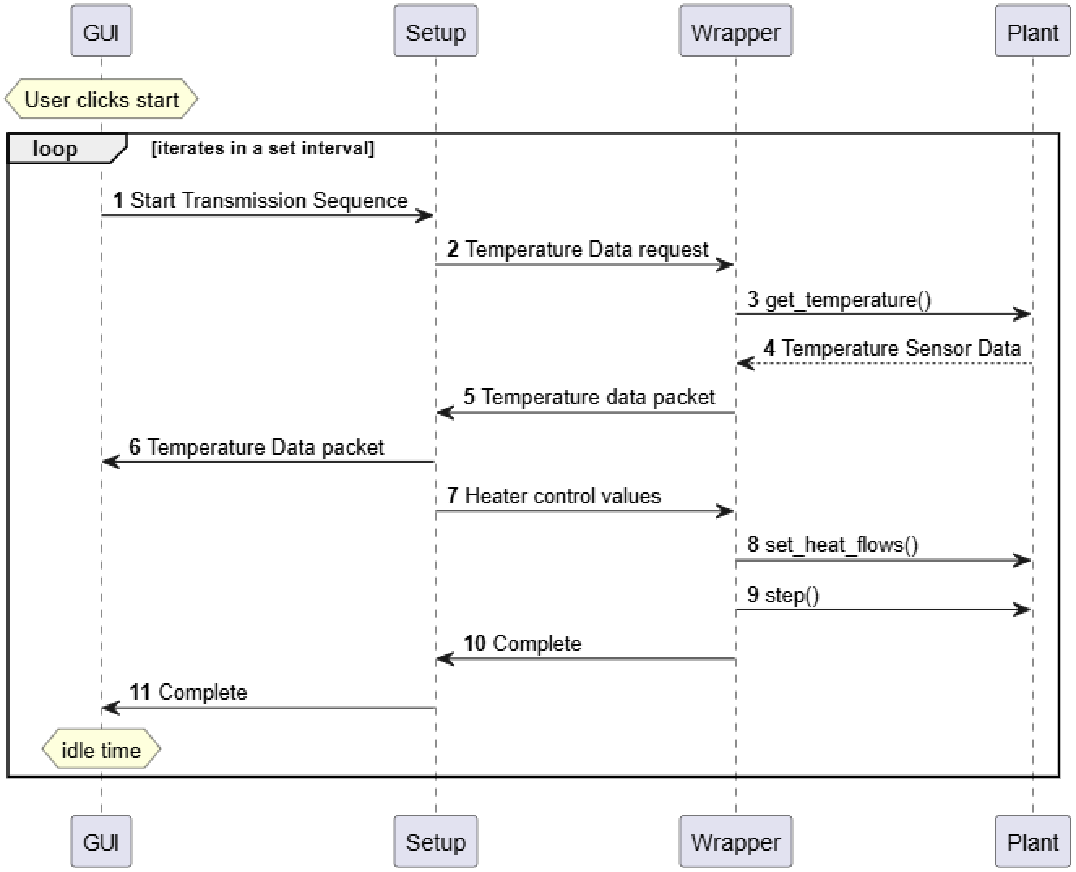
OBC	1	2	3	4
$\dot{Q}$	4W	1W	1W	0W

$$T_{\text{Cool1}}(t) = 5\text{K} \cdot \sin\left(\frac{2\pi}{90\text{ min}} \cdot t+\right) + 10\text{K}$$

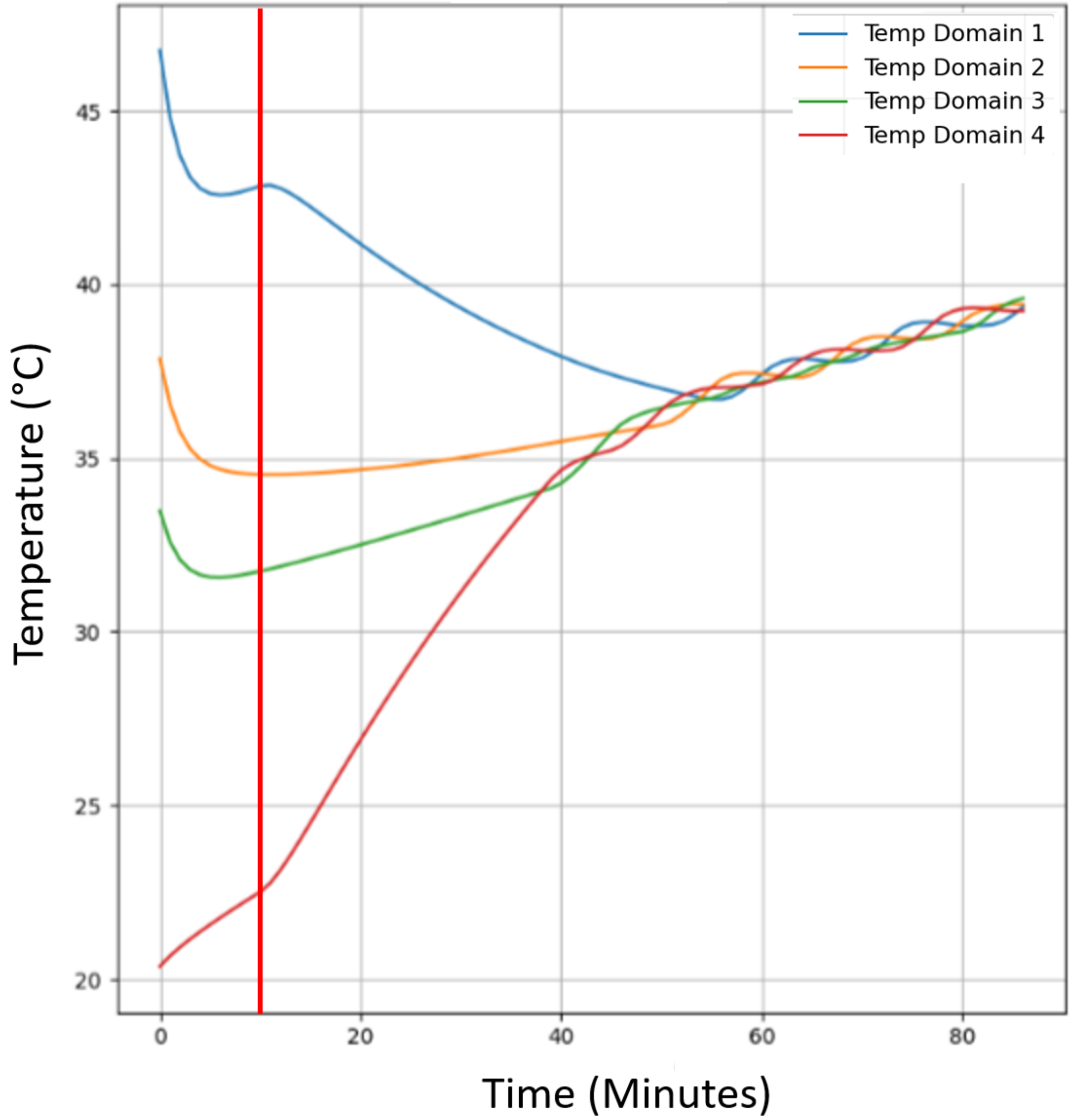
$$T_{\text{Cool2}}(t) = 5\text{K} \cdot \sin\left(\frac{2\pi}{90\text{ min}} \cdot t + \frac{\pi}{2}\right) + 10\text{K}$$

CLOSED-LOOP CONTROL CYCLE

- Control period $T_s = 3s$, integration step $\Delta t = 0.1s$
- Plant advances $60s$ per cycle (600 steps)



RESULTS AND OBSERVATIONS



Temperature Convergence and System Stability

- Controller enabled after 10 updates (20 min simulation time)
- Temperature converges to $39 - 40°C$ within 40 updates
- $dT < 1°C$ between domains
- Stable closed-loop operation ⟹ robust memory sync

SUMMARY AND OUTLOOK

System Evaluation and Future Improvements

- Design focus: functional correctness and low complexity
- Error handling and timestamp validation to be added
- CRC32 planned for transmission robustness
- Future interfaces: higher-speed serial links (SpaceWire, LVDS)
- Scalability to larger MPS architectures

CONCLUSION

- Deterministic, interrupt-driven synchronization for FPGA SoCs
- Efficient real-time data exchange without shared cache
- Demonstrated stable thermal behavior in simulation and low processing overhead
- Applicable to future small-satellite payloads

ACKNOWLEDGMENT

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THANK YOU FOR YOUR ATTENTION!