NanoXplore

N7 Development Strategy

NanoXplore

European Leader in FPGA, SoC FPGA & ASIC Design

- French Based Company : Paris, Montpellier, Grenoble
- 140+ Employees with more than 90% R&D Engineers
- Offer products for Hi-Rel markets
- 3 different products offering :
  - High reliable SoC FPGA
  - ASIC design services
  - Silicon IPs
- ITAR Free Technology
- Focus on Space & Defense markets

NANOXPLORE: a ‘One-Stop- Shop’ Solution Provider

NanoXplore

NanoXplore Design Services

FPGA

- Space proven products
- Tool chains

IPs

- Silicon proven IPs
- Tool chains

ASIC

- Turnkey Service for complex ICs

- Cryptographic & Security Services

- Sovereign Foundries
- Sovereign OSAT -Testing & Packaging
- ITAR Free & European Sovereignty

- All foundries

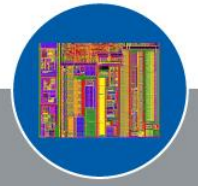
SERVICES & DIFFERENTORS

- Radiation Hardened
- Security
- European Supply chain

At the heart of the EU sovereign ecosystem

- Following the acquisition of Dolphin ASIC business, NX offers ASIC design service based on any process platform and N7 design platform particularly.
  - ISO9001 / EN9100 certified
  - Common Criteria MSSR certification in-progress
- Simplify the access to the N7 design platform for European partners.
- Flexible clear business model

● included
● optional



GDSII
From Concept to GDSII delivery

Know Good Die
From Concept to KGD delivery

Turnkey
From Concept to ASIC delivery

	GDSII	Know Good Die	Turnkey
Feasibility Study	●	●	●
Specification & architecture selection	●	●	●
System-level design	●	●	●
Circuit-level design	●	●	●
Prototyping (MPW)	○	●	●
Qualification	○	●	●
Packaging	○	○	●
Production	○	○	●
ATE (HW & SW)	○	○	●
Supply chain management	○	●	●
MCM/SoC integration/Board	●	●	●

N7 Platform - Key Considerations

Increasing complexity of Satellite payloads

- Large Data Processing capabilities
- Future proof solutions
- Mission Flexibility & Reconfigurability

➔SoC FPGA leveraging UDSM nodes is a suitable solution to tackle the above requirement.

Key Consideration

Fine pitch process to address the upcoming challenges

- Objective is to design high-reliable (hardened, space mission profile) UDSM components
  - Secure the technology necessary for next-generation space exploration and satellite constellations.
  - Remain at the forefront of space innovation and autonomy.
- No possibility to use commercial IP blocks without hardening / characterization effort
- Leverage as much as possible existing commercial technologies and EU design know-how to set up the right ITAR free design platform
  - Don’t recreate the wheel when possible…

Key Consideration

N7 Platform and Ecosystem requirements

- Key components and IP requirements requiring a large and diverse European ecosystem:
  - Processor (RISC V)
  - Accelerator (GPA)
  - Fabrik eFPGA (ULTRA7)
  - ADC/DACs
  - RF Rx/Tx

- **Not a single country in Europe has the technical capability to design such platform -> good time to team up !!**

Current funding update

- Various projects already started to support the design platform development

DUROC (3M€)

PUMA (3M€)

RCS (CNES) (1,6M€)

UDSM Fr (Etoile project) (9M€)

GSTP 102 (1st submission done > 20M€)

N7 design platform overview

Analog & Digital IPs and blocks.

Hard Block IPs

- Foundation (digital cells, memory blocks, IOs) Library
- Analog Building Blocks (Thermal Sensor, P and Aging Monitors, Oscillator, PLL, …)
- Interfaces (LVDS, …)
- High Speed Serial Link (Long & short Range) PHY
- RF ADC and DAC
- eFPGA fabric
- DDR4/5 PHY memory interface
- UCIe die to die Interface

Digital IPs

- JESD204 and SpF controller
- DDR4/5 controller
- General Purpose Processor (RISC-V based)
- General Purpose Accelerator (RISC-V based)
- PCIe controller
- Ethernet controller
- SpW controller

- **All commercial SW IPs can be bought from commercial IPs vendors -> hardening done by end-users using rad-hard foundation libraries**

Hard blocks IPs development strategy

- Selection of various IPs blocks development strategy based on the following criteria by order of priority:

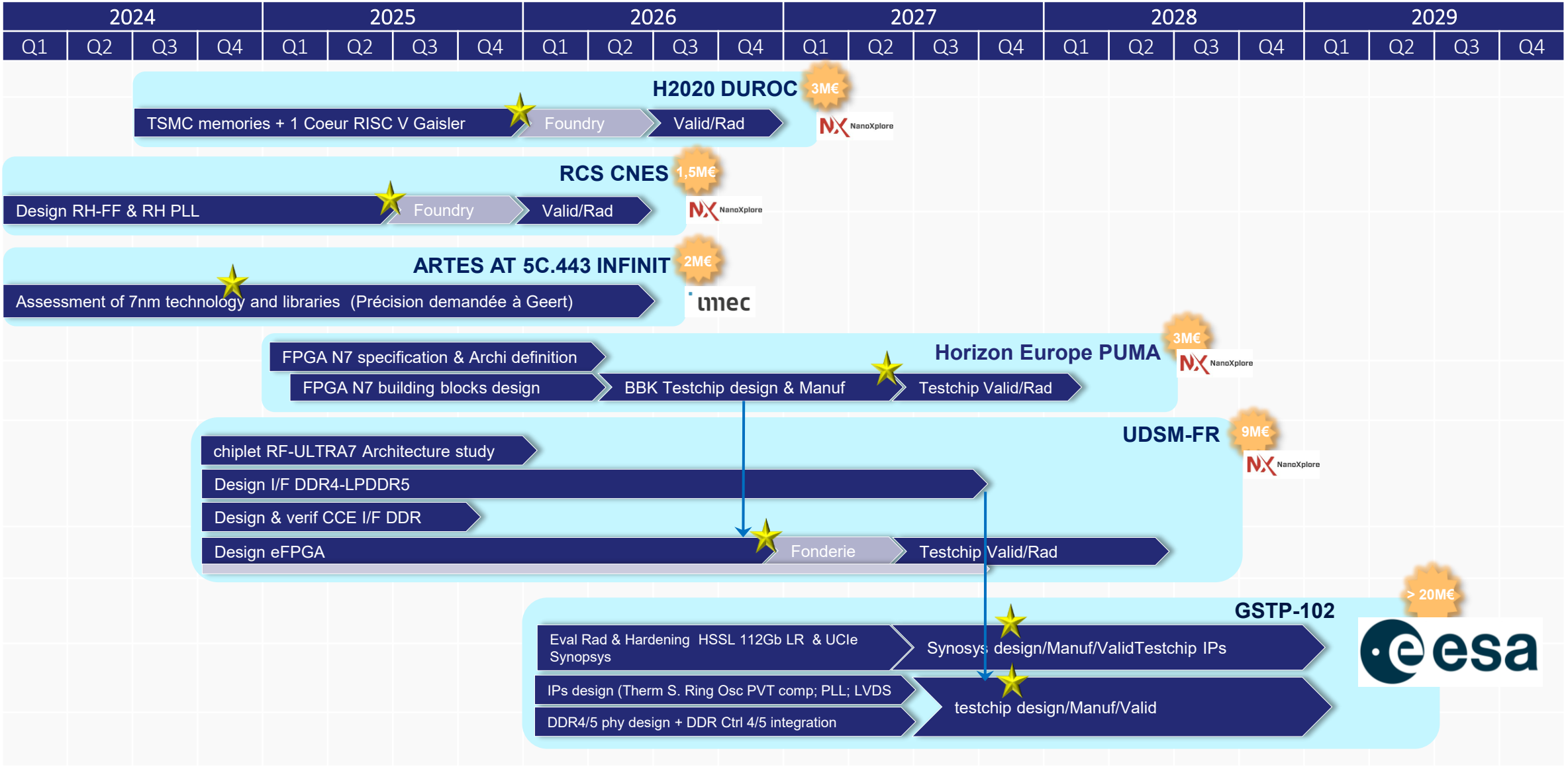
1. Technical capabilities, silicon proven know how
2. Existing commercial version to be hardened
3. Design from scratch with evidence of technical know how
4. ITAR free
5. Based in Europe
6. Already part of the European Space Ecosytem

- Need to grow knowledge and competency in Europe on critical IPs (HSSL, UCI-e, …)

N7 design platform – Hard block IPs funding strategy

Hard block IPs	DUROC	PUMA	RCS	Etoile	GSTP102	Not funded yet	Partners
Foundation digital cells library	✓		✓				NX, IMEC
Thermal Sensor, P and Aging Monitors, Oscillator, PLL			✓		✓		University of Pisa, NX
LVDS					✓		University of Pisa, NX
112Gbs HSSL long range					✓		Synopsys
112Gbs HSSL short range							Synopsys
FPGA fabric		✓		✓			NX
DDR4/5 PHY memory interface				✓	✓		NX, TAS, ADS
UCIe die to die Interface					✓		Synopsys
RF ADC and DAC						✗	

N7 Platform Development gantt chart



Thank you