



On-orbit data processing utilizing FPGA-accelerated deep learning models

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Agenda

1. Motivation & Challenges
2. SDK Overview
3. Model Deployment
4. Applications & Results
5. Data Processing Unit
6. IP Cores
7. Missions & Roadmap

Challenges

High-resolution sensors

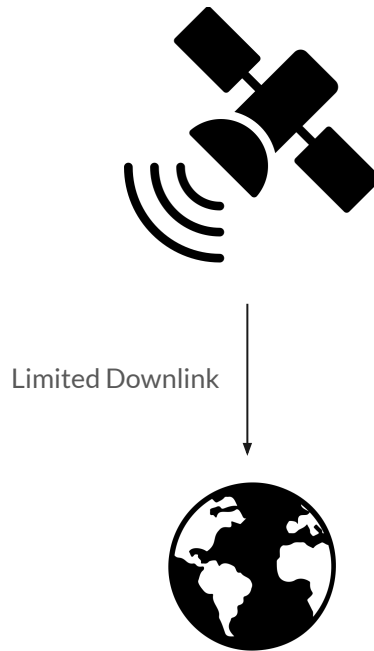
Even small satellites can generate terabytes of imagery, quickly exceeding onboard storage capacity.

Downlink bottlenecks

Limited bandwidth creates a growing gap between data acquisition and data return.

Lost value

Critical data is often delayed or discarded, reducing mission responsiveness and impact.



Onboard processing

Save bandwidth. Cut costs. Enable autonomy.

Efficient bandwidth use

Prioritize and downlink only what matters, drastically reducing data volume.

Lower mission costs

Minimize ground segment load, shorten analysis cycles, and reduce operational expenses.

Autonomous Operations

Enable real-time onboard decision-making for time-critical events.

Faster, Smarter Missions

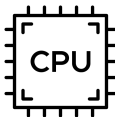
Deliver insights directly from orbit — not hours or days later.



Why FPGAs

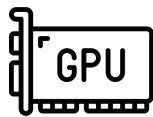
Inherent limitations

Selecting the right hardware for on-orbit AI requires balancing high throughput with a constrained power budget



CPU

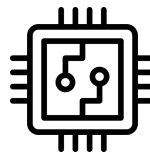
Not parallel enough for high performance



GPU

High parallelization performance

Prohibitive power consumption for some satellites



FPGA

Custom parallelism

Low power consumption

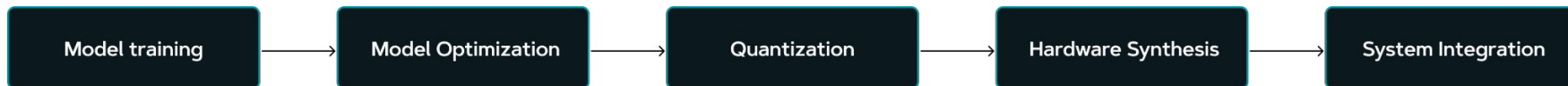
Reconfigurable

Space heritage

End-to-end SDK Pipeline

Deployment of AI models

This requires domain knowledge from both the data science domain and hardware engineering with emphasis on FPGA development. It's a multi-step process that represents a significant knowledge barrier for satellite developers, requiring specialists in both fields.



Supported models and hardware

Supported FPGAs

AMD Zynq 7000 series

AMD Zynq UltraScale+ MPSoC

AMD UltraScale

AMD 7 Series

Supported AI/ML models

Classification

- ResNet – CNN with residual connections

Segmentation

- ResNet/UNet, FCN – pixel-wise mapping

Object Detection

- YOLO, SSD – real-time multi-scale detection

Super-Resolution

- ESPCN – efficient image upscaling

Lightweight Models

- MobileNet – optimized for low-power compute

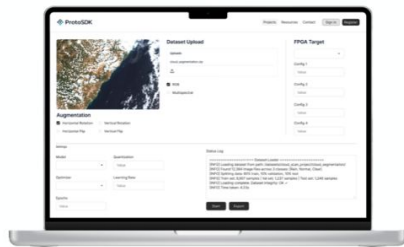
How it works

SDK

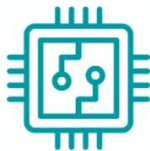
SDK is a low-code software framework for deployment of AI models on FPGAs.

Data Processing Unit (DPU)

Data Processing Unit runs AI models onboard and enables seamless integration of AI capabilities into satellite systems.



ProtoSDK



FPGA chip



**DPU with FPGA
chip**



**Integration to the
satellite**

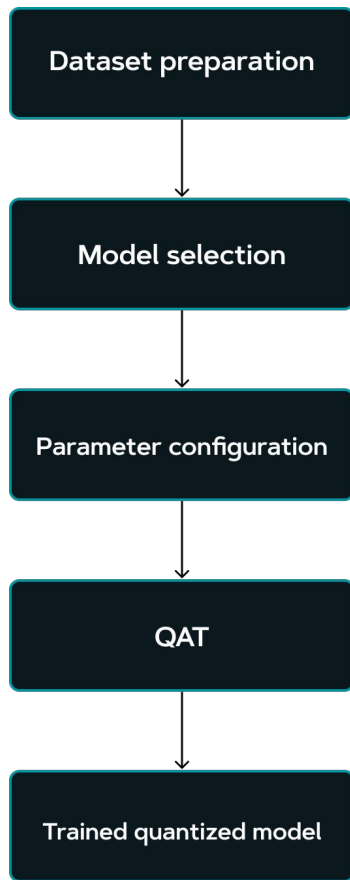
How it works

Model training and quantization

- Core functional block of the SDK
- Parse user configuration
- Augment dataset
- Select model architecture
- QAT
- Exports into QONNX
- Creates necessary input artifacts

Output

Creates a QONNX neural network ready for further transformations



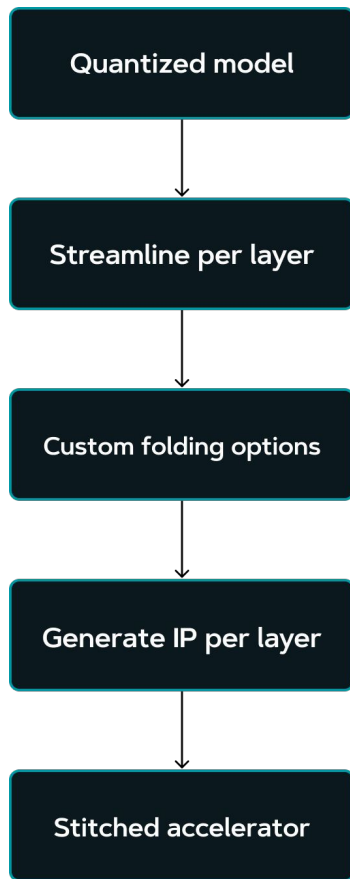
How it works

Custom FINN pipeline

- Manages transformation - Model to accelerator
- Converts quantized network into streaming dataflow
- Creates distinct IP blocks for each layer
- Modifications allow for custom resource utilization
- Individual IPs are stitched together to form accelerator core
- The core is designed to be added to integration templates

Output

Accelerator core ready to be added to integration template



How it works

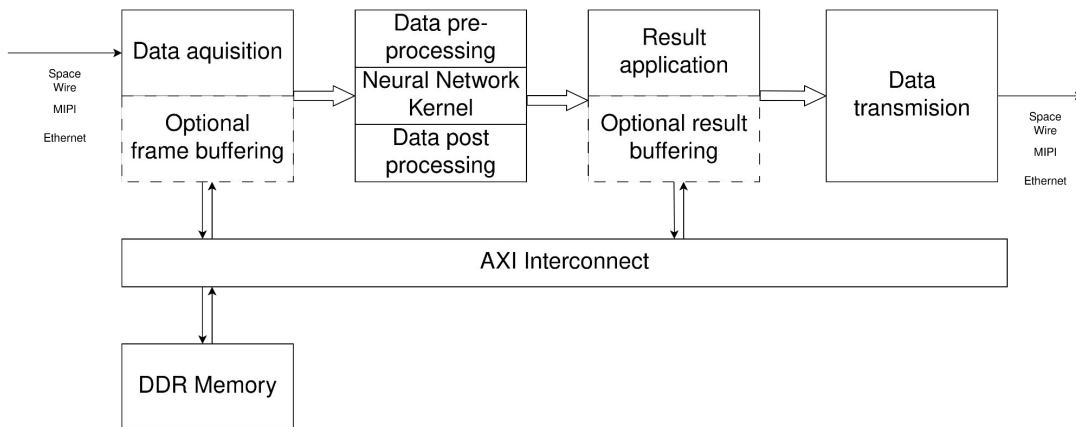
Integration templates

Templates define:

- External DDR memory
- AXI-based interconnects
- DMA engines and peripherals
- CPU firmware or Linux runtime

Prepared for:

- Zynq UltraScale+ SoCs
- Standalone FPGAs with soft CPUs



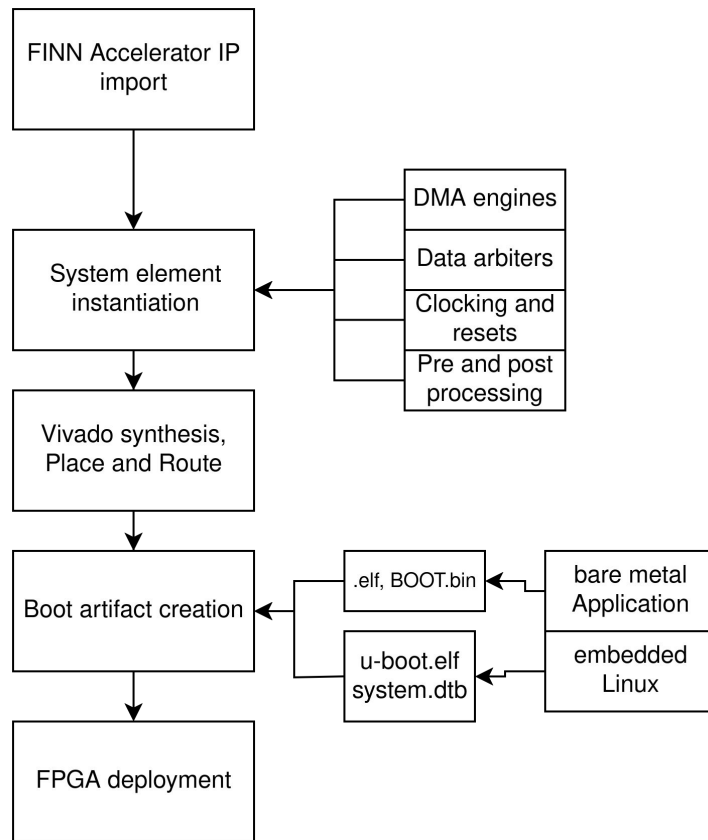
How it works

Integration process

- TCL-driven Vivado scripts
- Automates:
 - Import of kernel
 - DMA and AXI instantiation
 - Device-specific mappings
 - Control and data interfaces
 - Synthesis
 - Implementation
 - Bitstream export
- No GUI interaction needed

Result

Ready bitstream and hardware description



Use cases overview

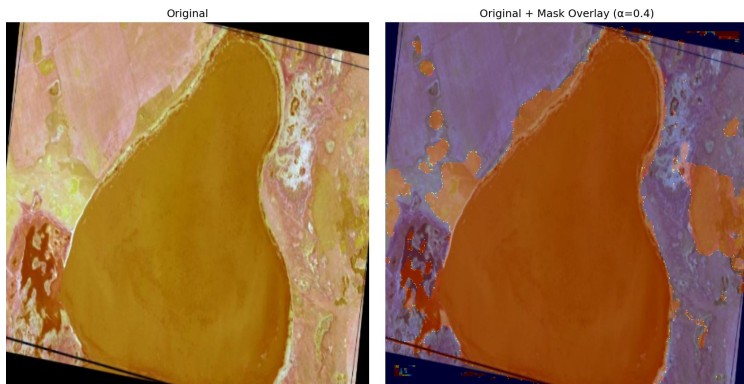
Water body segmentation

Description

U-Net trained on a custom dataset made from Copernicus data.

Quantization level

- 8-bit weights
- 8-bit activations



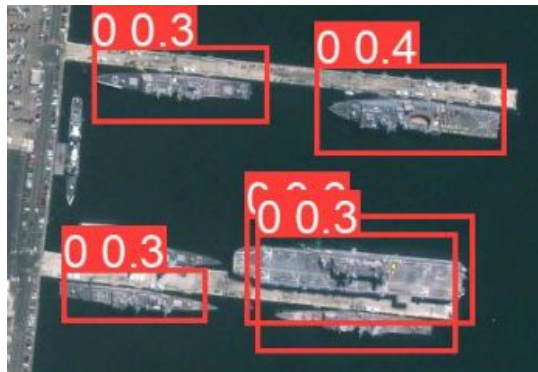
Ship detection

Description

YOLOv3-tiny trained on ShipRSImageNet dataset, the classes were modified to fit only ship class.

Quantization level

- 8-bit weights
- 4-bit weights

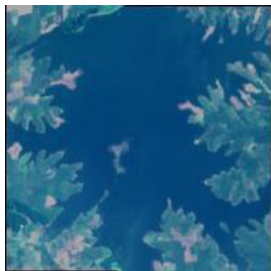


Results and discussion

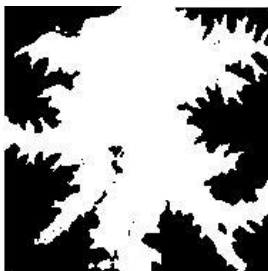
Water body implementation

- Post-implementation
- Default resource utilization strategy
- Can be further improved by custom folding

DEVICE	LUT	SRL	FF	BRAM_36K	BRAM_18K	URAM	DSP
ZCU104	112,157	616	63,162	20	2	0	103
KV260	112,728	609	63,897	20	0	0	103



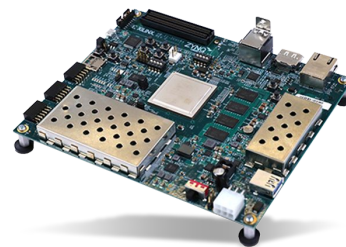
Input



Segmentation

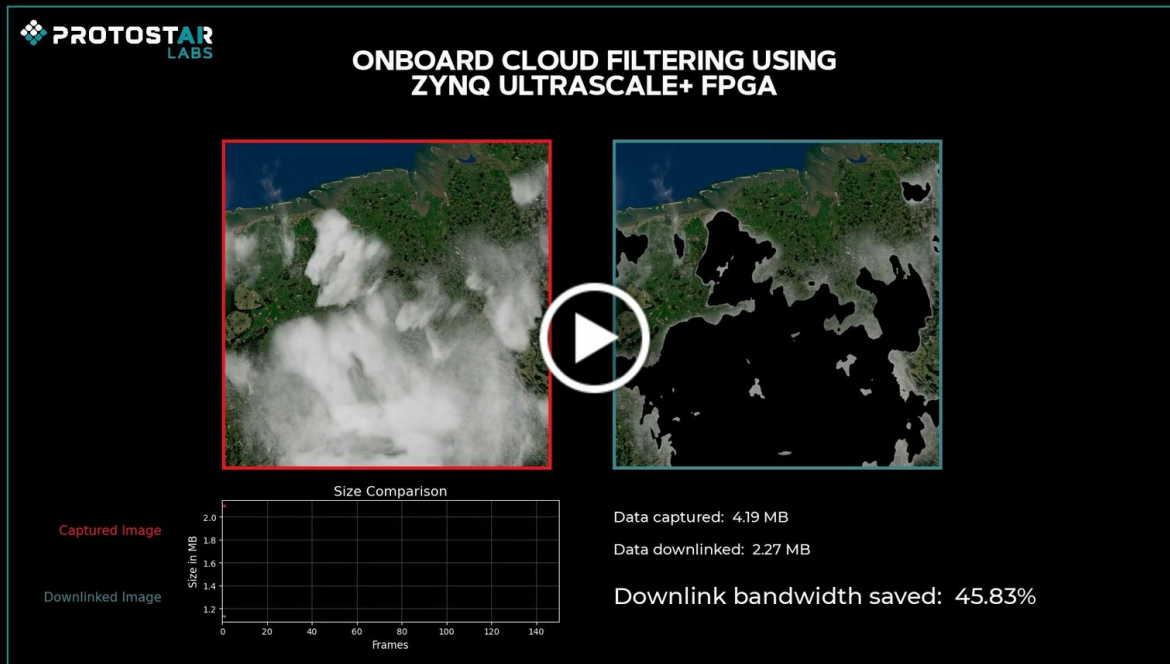


Protostar Labs' DPU (KV260)

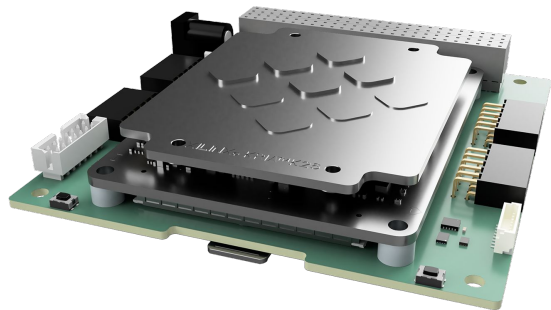


ZCU104

Other use cases



Data Processing Unit



Key Features



Onboard AI Capabilities

Run AI models onboard for real-time inference and detection.



Low-Power, High-Performance

Optimized for efficient processing in compact, power-limited platforms.



Modular and Standardized

PC/104 form factor for easy CubeSat integration and stacking.



FPGA Acceleration

Kria K26 (Zynq UltraScale+) enables software-defined hardware acceleration.

Designed for SmallSat-class platforms, the unit supports CAN, I²C, SPI, LVDS, and RS-232 interfaces. Fully compatible with the SDK, it enables fast, low-friction deployment of AI models to FPGA hardware.

Data Processing Unit

Technical Specifications

Feature	Value
FPGA Device	AMD Zynq UltraScale+ MPSoC
Dimensions	94 x 89 mm (Fits PC/104 standard)
Interfaces	CAN, I2C, SPI, LVDS, RS232
Connectors	PC/104 4x26 stackable connector 4x PMOD connectors JTAG header 2x 15-pin CSI camera connectors 14 PIN MOLEX UART debug connector
Other Features	Micro SD card slot 4x boot mode selector switches 12V active cooling with PWM control
Power Supply	12V @ 3A via 5.5 x 2.1 mm barrel jack
Power Consumption	~9-14 W

Use Cases



Cloud Segmentation



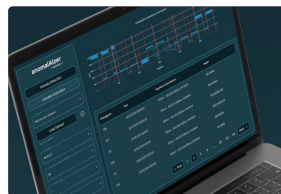
Super Resolution



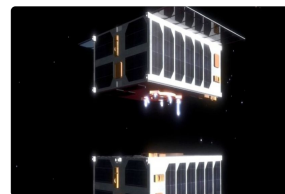
Object Detection



Object Classification



Anomaly Detection



In-Orbit Inspection

FPGA IP Cores

IP Core Portfolio

Video Processing

- **Video Fault Supervisor (VFS):** Monitors integrity of input/output video streams
- **Video Image Resize (VIR):** Resizes video to target resolutions

Data Handling

- **Data Encryption (DENC):** Secure transmission over untrusted media
- **Image Data Compression (IDC):** Reduces bandwidth/storage with selectable algorithms
- **SpaceWire (SWire):** Standard-compliant LVDS data transfer protocol

Image Intelligence

- **Cloud Segmentation (CloudSeg):** Identifies clouds in orbital imagery
- **Object Detection (OD):** Detects mission-relevant objects in imagery
- **Change Detection (CD):** Highlights differences across consecutive frames



Space Missions

ESA OPS-SAT Space Mission



Goal

The goal of this mission was to port our proprietary algorithms for **anomaly detection** to the onboard FPGA (Field Programmable Gate Array) and run the algorithms on the OPS-SAT telemetry data.

Solution

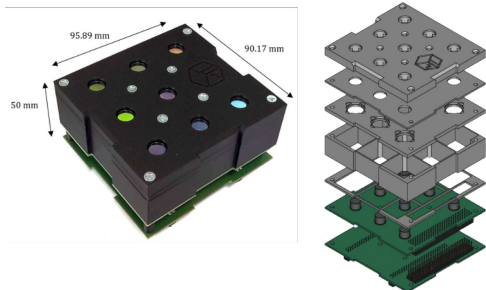
Porting the needed algorithms to their VHDL equivalents for the onboard **Intel Cyclone V** and feeding the needed data to the FPGA using ARM.

Current developments

- FPGA-based Anomaly Detection
- On-Orbit FPGA Reconfiguration
- Real-Time Telemetry Analysis

Current Status - COMPLETED

LPCM: Light pollution characterization from the Low Earth Orbit



Goal

To address the issue of light pollution by designing and developing a **satellite module to monitor light emissions** from the Earth. We are building a satellite module equipped with **single-pixel detectors** for analyzing light sources from LEO.

Solution

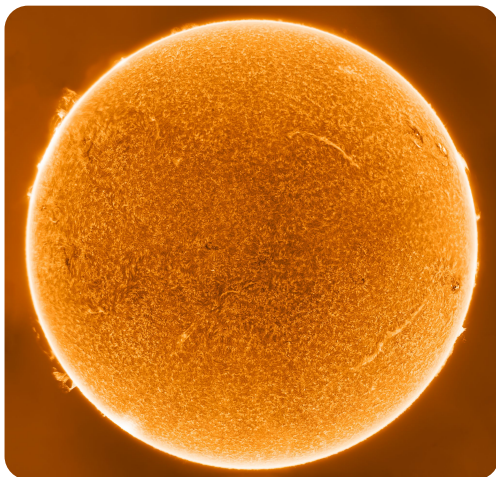
Protostar Labs is responsible for **electronics design and onboard software**. Besides that, we are developing a **mission planning and execution** software.

Current developments

- hardware development and verification underway
- onboard software progressing with adaptive control features

Current Status - IN PROGRESS

ChROmosphere Monitoring InStrument (CROMIS)



Goal

Provide reliable **space weather monitoring** to support satellites, astronauts, GNSS, and power grid operations. The onboard processing of solar images will be handled by the **SDK and DPU**.

Solution

A dedicated **H α space telescope** delivering **full-disk, high-resolution, high-cadence solar images**. Continuous, publicly available data stream for both scientific and commercial applications.

Expected Results

- enhanced space weather forecasting services for government, industry, and operators
- positioned as the first Croatian space science instrument, boosting technological capability and integration into ESA

Current Status - IN PROGRESS

About Us

2019
Founded

50+
Projects

24
Team Members

- Croatian space tech company, based in Osijek
- Expertise: **onboard data processing systems, fault-tolerant electronics, optical payloads, AI/ML**
- Our vision is to pioneer Croatian technology in space and other critical industries on Earth



Thank you for your attention! Questions?



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