

EDHPC 2025

Design and Development of a Redundant Ethernet Switch for Small Satellites

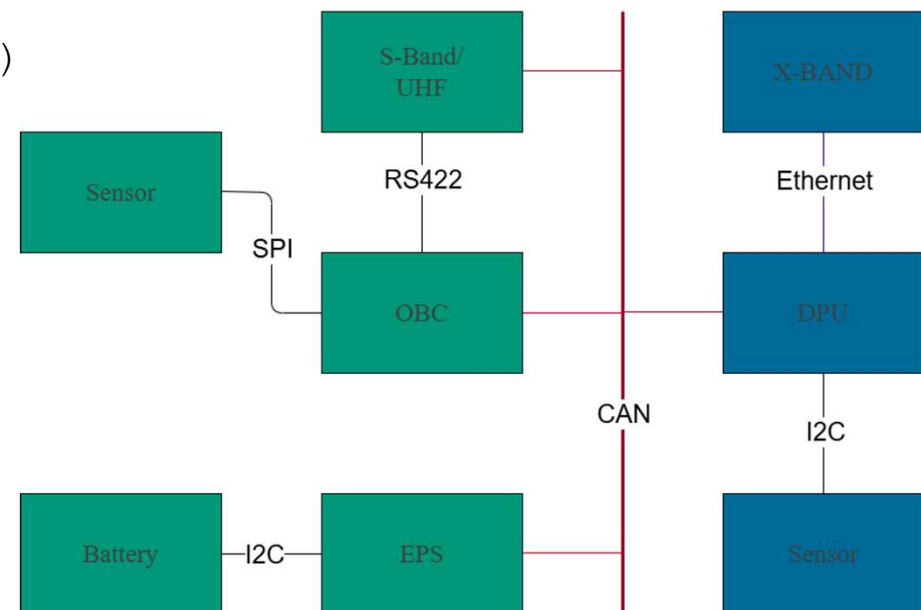
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Motivation

Gaps in current SmallSat buses

- Most Common busses used in “New Space” SmallSats:
 - I2C, RS485, CAN, SpaceWire, Ethernet
- Developed for different purposes (Sensors, Controllers, Space,...)
- SmallSats often use COTS components with standard interfaces
- Current SmallSats have multiple buses:
 - telemetry/telecommand: CAN
 - Low data rate payload& transmitters: RS422/485
 - high data rate payload & transmitter: ethernet
 - high reliability & data rate payloads: SpaceWire
- Routing happens on protocol level (e.g. CSP)
- Some nodes are gatekeepers → single points of failure
- Complex and untransparent data paths with many dependencies

→ Proposed solution: redundant, multi-standard, multi-speed ethernet switch complemented by Time-Sensitive Networking (TSN)



Requirements

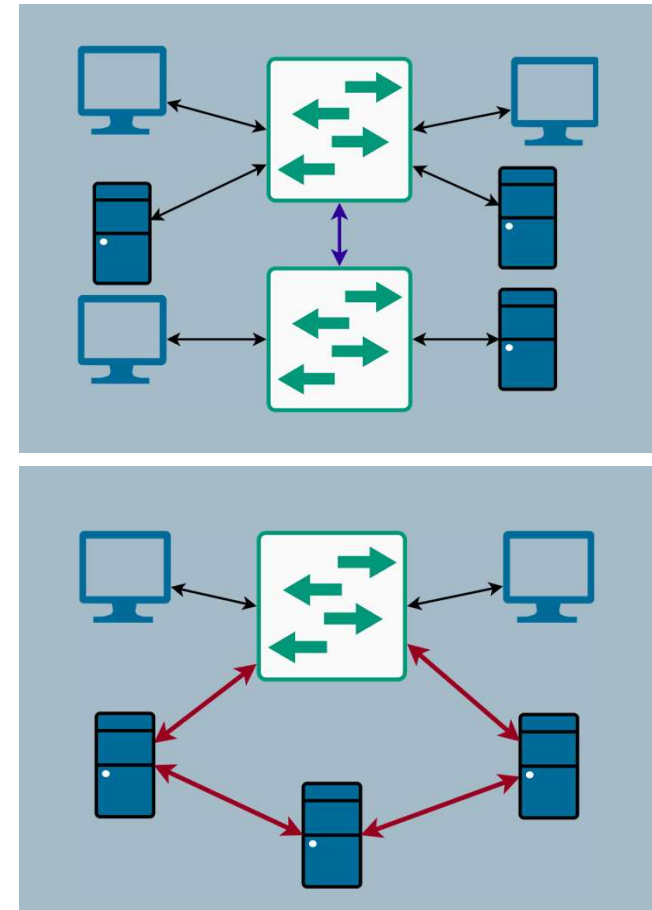
Design Targets

- Functional:
 - Common, switched Layer-2 fabric for command and data across platform and payload of a Small Satellite.
 - Multiple 1000BASE-T ports for DPUs, cameras, and radios.
 - Redundant 10BASE-T1 buses for microcontroller-class endpoints.
 - VLANs isolation with priority code point.
 - Management port for diagnostics.
 - Per-flow schedules for critical traffic, e.g. IEEE 1588 profile suitable for TSN.
- Non-functional
 - Redundancy concept to eliminate Single Points of Failure (SPOF).
 - Fault-Detection, Fault-Isolation and Recovery (FDIR) capabilities.
 - Minimal packet loss under any single link/node failure.
 - Fit Small Satellite power and thermal envelopes.
 - Redundancy concept for nodes with only a single port.
 - Reconfigurable in flight.
 - Basic switching functionality without external configuration.

Topology options

Overview

- Classic star or tree
 - One central switch or chain for 10/100/1000BASE-T
 - Commonly used at home
 - Switch is a single point of failure
 - Link to switch is single point of failure
- Ring topology:
 - Possible with High-availability Seamless Redundancy (HSR)
 - No switch required/can be built with multiple switches
 - Packets from source nodes are duplicated and sent in both directions
 - Upon arrival packets are deduplicated
 - Switch or dedicated hardware acts as Reduction Box (RedBox)
- Bus topology:
 - Not possible with common 10/100/1000BASE-T
 - Automotive/Embedded solution: 10BASE-T1(s)
 - Single LVDS, low data rate, no switching needed

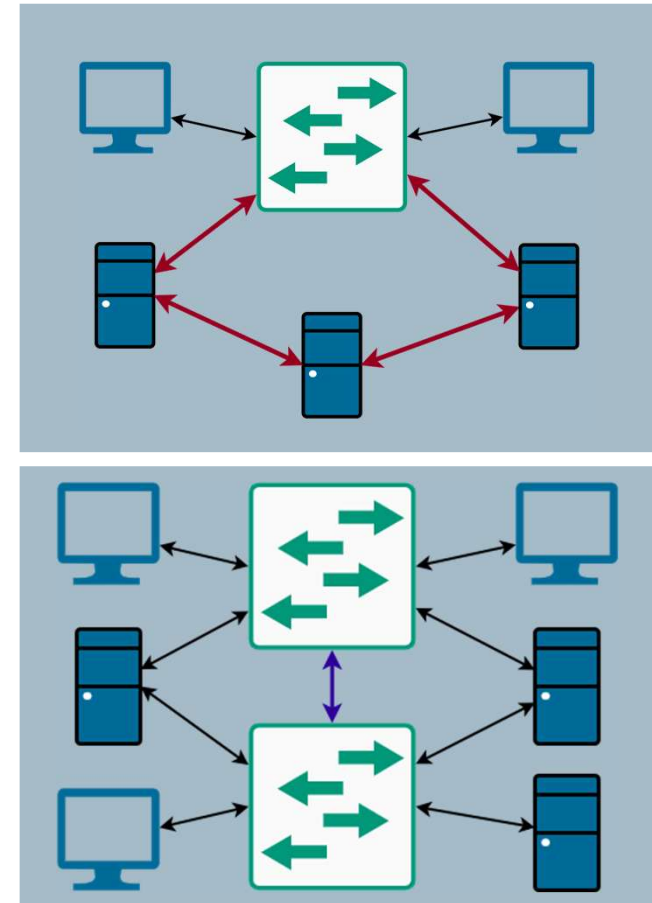


Topology options

Candidates

- HSR Ring
 - Multiple nodes/switches form a ring
 - Switches act as RedBoxes for attached devices
 - Pros: seamless failover
 - Cons: dual-homing complex, traffic doubled, RedBox activity is expensive
- Dual Switch
 - Two switches are connected via Inter Switch Link (ISL)
 - Routing via Spanning Tree
 - Pros: easy implementation, hot or cold redundant, straightforward dual-homing
 - Cons: no seamless failover, ISL may be a bottleneck

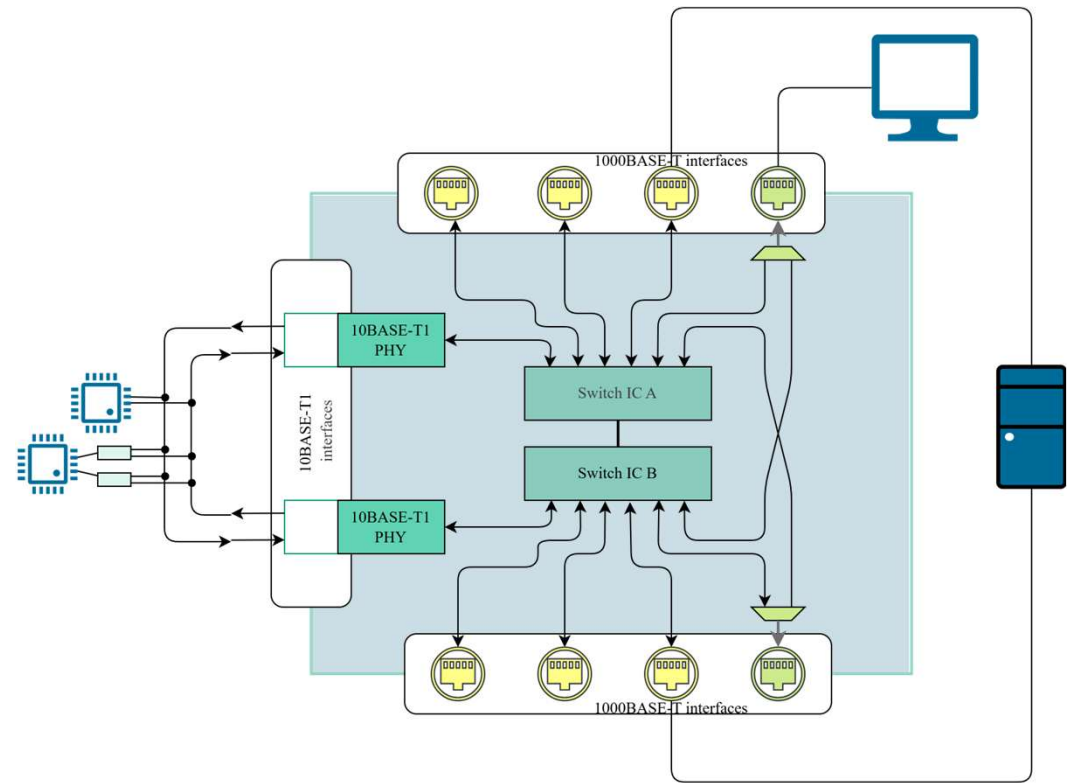
→ Decision for first prototype: Dual-Switch with mixed media ports



Prototype System Design

Connecting legacy and low power nodes

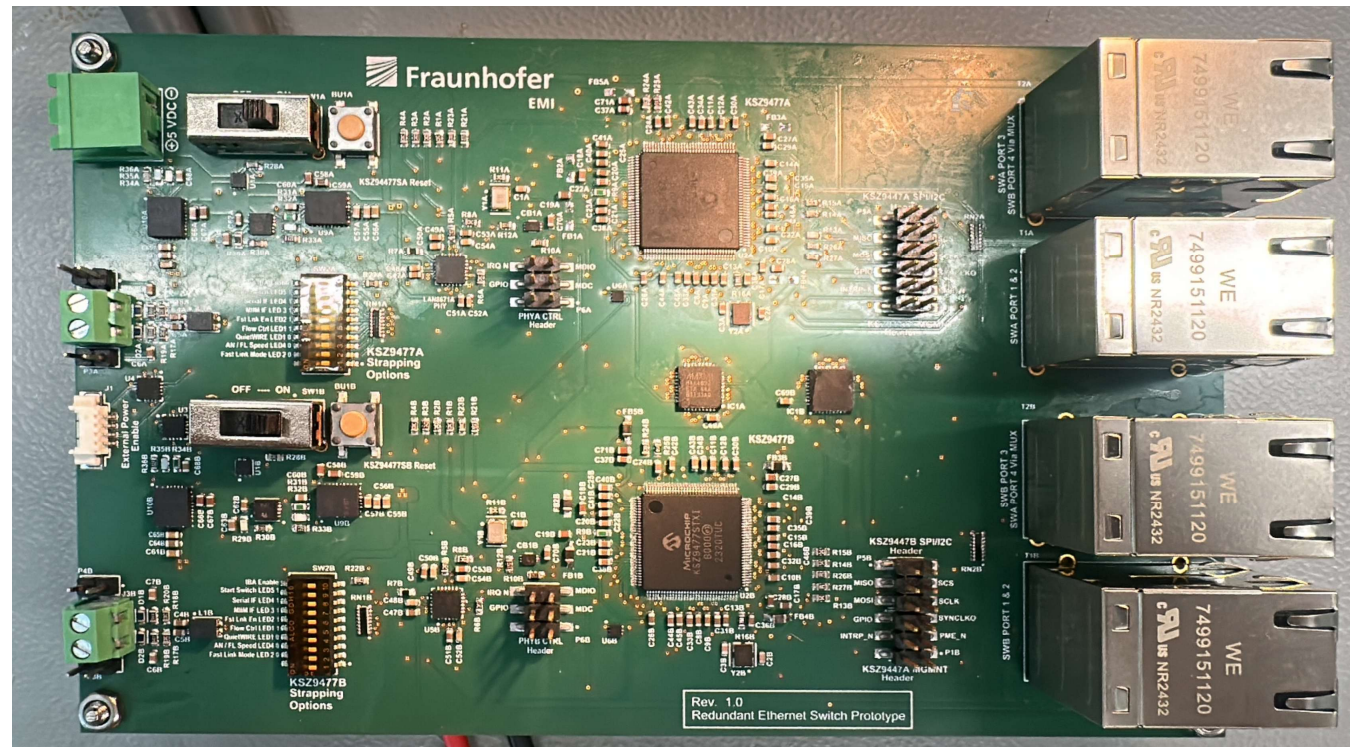
- To achieve redundancy, nodes must be connected to both switches
 - Most ethernet devices have only one port
 - Link is single point of failure
 - No truly redundant solution possible (Point to Point)
 - Our solution: Analog Multiplexer (MUX)
 - Likelihood of MUX failure lower than switch failure
 - Heritage in previous mission
 - Microcontrollers must be integrated via 10Base T1(S)
 - RMII capable microcontrollers connected via PHY
 - MAC-PHY solutions with SPI exist
 - Redundant PHY/MAC connection (similar to CAN)
 - Redundant Buses possible, or
 - 10BASE-T1 bus connected to both Switches
- L2-Loop!! must be configured in spanning tree protocol!!



Hardware Platform

Prototype

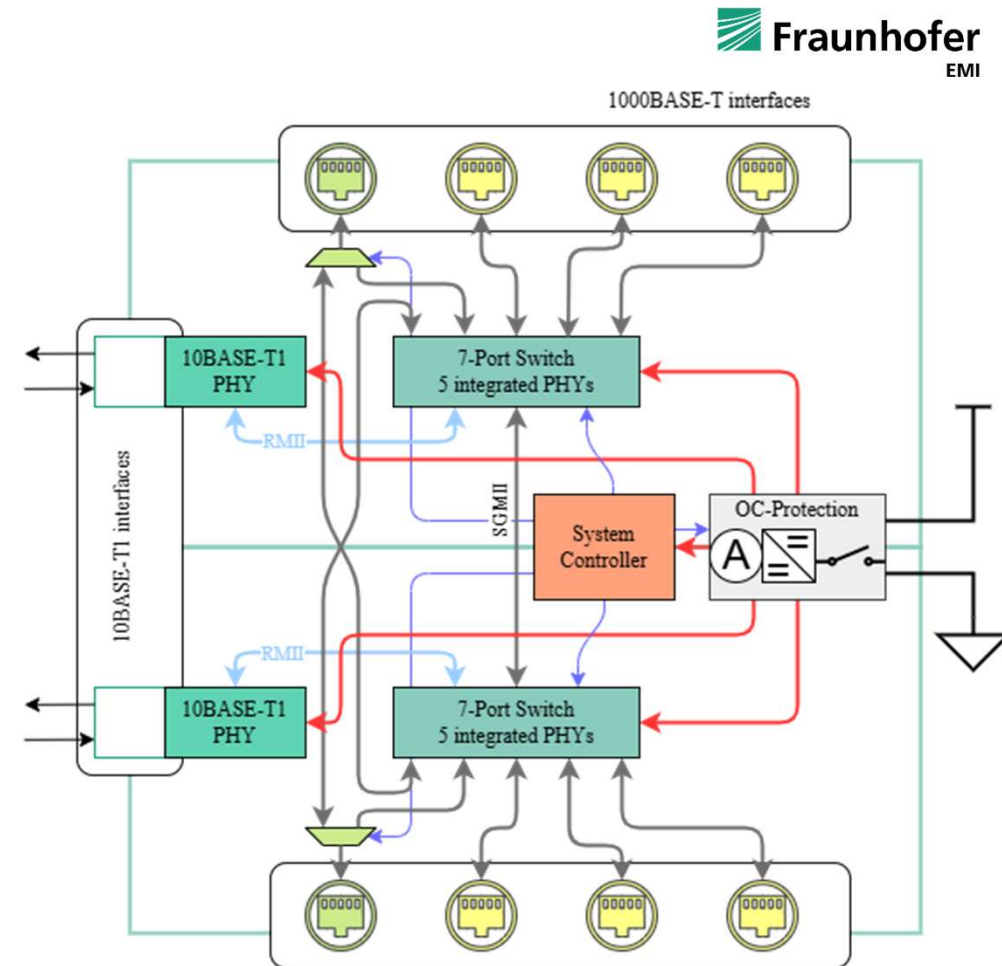
- Two KSZ9477S as 7-port switches
 - 5 integrated 10/100/1000BASE-T PHYs
 - RGMII interface to 10BASE-T1 PHY
 - SGMII interconnect
- 2 x 10BASE-T1 PHYs
- MAX4890 high-speed analog switch as MUX
- 8 RJ45
 - 6 x standard ports
 - 2 x multiplexed ports
- Power supply, strapping resistors, reset
- No System Controller
 - SPI interface of KSZ9477S
 - MDIO interfaces of PHYs
 - Both connected to RaspberryPi



Reliability and FDIR

Redundancy and Switchover

- Supervisor needed for Fault Detection, Isolation and Recovery
- Adaptive overcurrent protection reasonable:
 - Power consumption dependent on operation mode and traffic
 - Static protection can't distinguish a latchup from traffic spike
- Supervisor connected to management ports for:
 - Link status surveillance
 - Switch status surveillance
 - Switch reconfiguration
- Switched Ethernet isolates many failure modes like
 - malformed frames rejected at ingress
 - "babbling idiot" containment via scheduling/queues
- Supervisor ideally part of 10BASE-T1 bus



Determinism

Features of the KSZ9477S

- Goal: deterministic latency/jitter using standard hardware.
 - Enable features on 100/1000 Mb/s links; treat 10 Mb/s (10BASE-T1S) as unsynchronized control bus.
- sub-microsecond time alignment on high-speed links, stable latency/jitter for scheduled/control flows.

Feature (KSZ9477S)	Functionality	Effect vs. plain switching
Time synchronization (IEEE 1588 / 802.1AS)	Common time base across nodes	Windows stay aligned; no drift; consistent release times
Time-Aware Scheduler (time-gated egress; 1 queue/port)	Reserve a protected transmit window	Lower classes cannot block scheduled traffic; deterministic release
Credit-Based Shaper (per queue)	Smooth jitter of payload streams	Removes burstiness; steadier egress than FIFO
Strict priority with 4 egress queues	Protect safety/control frames	Control bypasses best-effort under load
VLAN tagging + priority mapping (PCP)	Consistent class handling end-to-end	Predictable queue selection and isolation
Optional cut-through on scheduled ports	Reduce hop latency when conditions fit	~0.9 μ s at 1 G vs store-and-forward delay

Expected performance

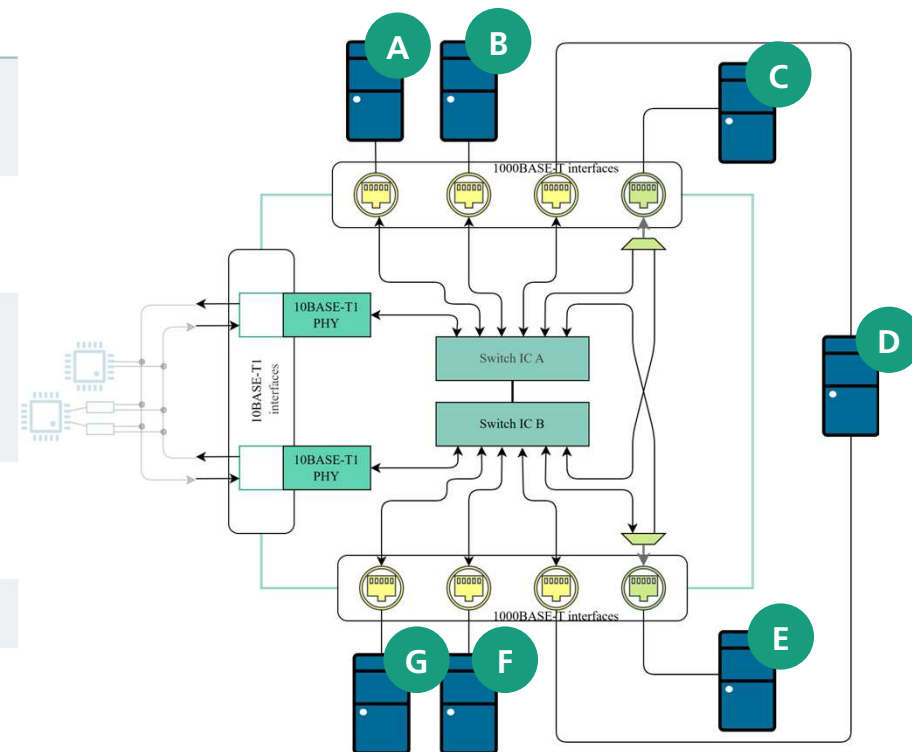
Preliminary requirement evaluation

Requirement	Validation	Result
F1: Common, switched Layer-2 fabric	Test	Ok , connectivity and speed test for 10/100/1000BASE-T TBD , for 10BASE-T1
F2: Multiple 1000BASE-T	Analysis	Ok
F3: Redundant 10BASE-T1	Analysis	Ok
F4: VLANs isolation	Analysis	Ok , selected switch ICs support VLAN
F5: Management port	Inspection	Ok , port status read, configurations applied via SPI
F6: Per-flow schedules	Test	TBD
NF1:Single Points of Failure	Analysis	No , Muxes are SPOD for single port nodes
NF2: Fault Detection Isolation and Recovery	Test	TBD , Disrupt links, power off ICs → assert link recovery Ok for dual homed nodes
NF3: Minimal packet loss	Analysis	Partially , packet loss occurs at muxes and bond links →HSR(?)
NF4: Small Satellite power and thermal	Inspection	OK , power is at ~5W while switching, thermal for next revision
NF5: Redundancy concept	Analysis	Partially , see SPOF
NF6: Reconfigurable in flight	Analysis	Ok , see Management Port
NF7: Basic switching without external configuration	Inspection	Ok

Validation

Test plan and preliminary results

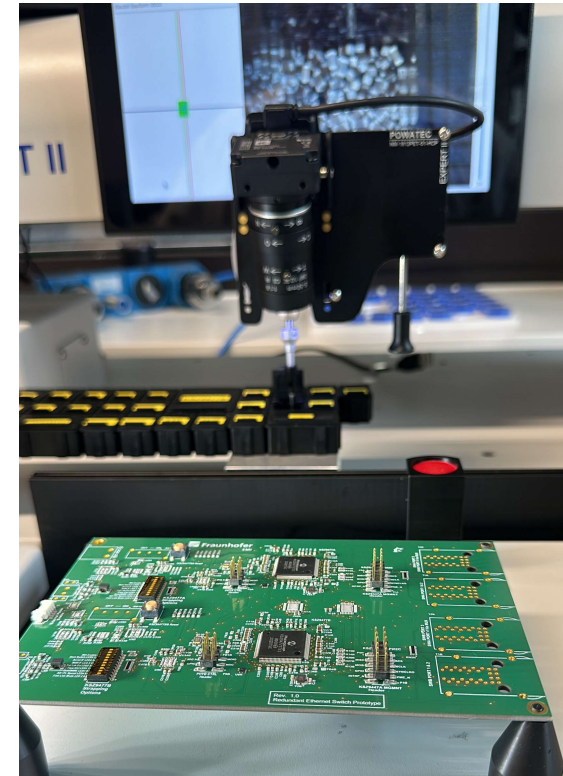
Test	Setup	Result
T1	Two nodes on same switch (A&B,F&G)	OK, Gbit, bidirectional
T2	Nodes on each switch, SGMII ISL (A&G,F&B)	OK, Gbit, bidirectional
T3	Nodes on mux and directly connected (A/B/D/F/G&C/E)	OK in all power states; mux selects active side
T4	Dual-homed node (bond) and mux node (D&C,D&E)	OK, packet loss on switchover
10BASE-T1	Multiple nodes, topologies	TBD
Timing	Jitter, Latency on all ports under load	TBD
Determinism	Priority & traffic shaping	TBD



Roadmap

Next steps

- Test 10BASE-T1:
 - Testing with different nodes (Microcontrollers, CSP-bridge,...)
 - Testing with different topologies
 - Testing failover mechanisms
 - Timing measurements
- Qualitative testing
 - Measure timing, jitter, throughput in different configurations
- Design and build next revision:
 - Integrate system controller
 - Integrate overcurrent protection
 - Environmental Testing
- ...
- Build an FM, fly it....



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