From Zynq™ UltraScale+™ to Versal™ AI Core based High Performance Processing solutions

EDHPC 2025
A.MEGE
B.LEROY
BARRAL Christophe

AIRBUS

Section 1 (not applicable in France, please go to section 3)

This document contains Technical Information :

Yes ☒ No ☐

If No to section1: please complete Section 2
If Yes to section1: please complete Section 3 as applicable

Section 2 (not applicable in France, please go to section 3)

I confirm the document does not contain Technical Information and is « **Not-Technical** »

Name:

Date:

Section 3

3a. National and EU regulations Export Control Assessment

This document has been assessed against applicable export control regulations in

☒ France ☐ Germany ☐ Spain ☐ UK ☐ Other

☒ and does not contains Controlled Technology[1] and is therefore **« Not Listed / Not Controlled »**

☐ and contains Controlled Technology with export control classification

☐ **Note:** Any transfer of this document in part or in whole must be made in accordance with the appropriate export control regulations. Prior to any transfer outside of the responsible legal entity, confirmation of an applicable export licence or authorisation must be obtained from the local Export Control Officer (ECO).

3b. US (ITAR/EAR) Export Control Assessment

☒ This document does not contains US origin Technical Data (Technology)

☐ This document contains « Technology » which is controlled by the U.S government under [USML category number / ECCN] and which has been received by [Legal entity] under the authority of [Licence number / ITAR exemption / EAR licence exception / NLR]

☐ This document contains technology which is designated as EAR99 (subject to EAR and not listed on the USML/CCL.)

Note: Any re-export or re-transfer of this document in part or in whole must be made in accordance with the appropriate regulation (ITAR or EAR) and applicable authorization. If in any doubt please contact your local ECO.

3c. Technical Rater Information

This document has been assessed by the following Technical Rater :

Assessed and classified by: A.MEGE

Date classification completed: 2025-10-10

[1] "Controlled Technology" is defined as any Information necessary for the design, development, production, use, operation, maintenance or repair of export controlled goods. Examples of such Information are blueprints, plans, diagrams, models, engineering designs, manuals, requirements specifications and instructions etc. If in any doubt please contact your local Export Control Officer (ECO)

Space Electronics portfolio

Electric Propulsion

Power Distribution & Regulation

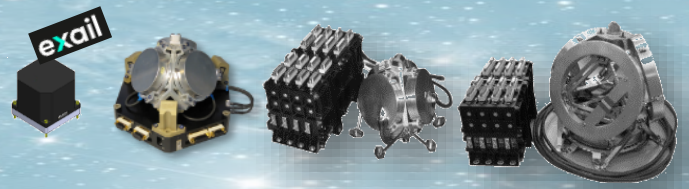
Power & Propulsion Units

On-board Computers

Security

Payload Data Handling

Platform & Payload Processing Units



Fiber Optic Gyroscopes

Control Moment Gyrroscope

Sensors & Actuators

www.airbus.com/en/products-services/space/equipment

AIRBUS

Motivations and stakes

On board processing for earth observation (Optical / Radar / …IA) :

- Computational Power : FPGA Cores + AI Engines + Software Framework
- Memory Throughput (IA)

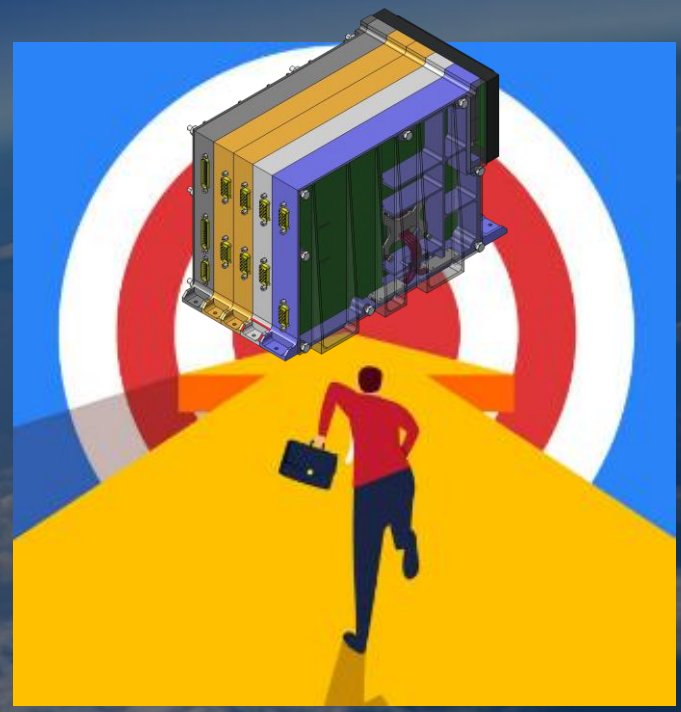
Different applications ->
various usage of the processing core

LEO Telecommunications / 5G :

- ADC/DAC Interfaces : Many High Speed Serial Links, 25Gbps+
- Computational Power : FPGA + AI Engines + Processor : > 90W dissipated by FPGA
- Routing Interfaces : PCIe3x8 (co-processing) , 10Gb & 100Gb Ethernet

Science :

Mass Correlators / Computational Power: FPGA + Internal FPGA Memories



Hardware equipment with VERSAL

Real technical challenges :

- Power density - heat dissipation
- Processing core supply : high current - low voltage
- Data throughputs
- Technologies assembly & manufacturability
  (components pitches / high pin counts / PCB technologies …)

Keeping the constraints of space design

- Conductive cooling
- Radiations
- Reliability
- Etc…

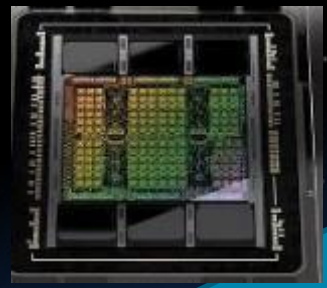
Technical challenges must be addressed for a flight usage of the Versal chip

Power density

VERSAL
20W/cm²

RTG4
2W/cm²

NVIDIA AI GPU
85W/cm²



H200 © NVIDIA

Nuclear power plant
55W/cm²

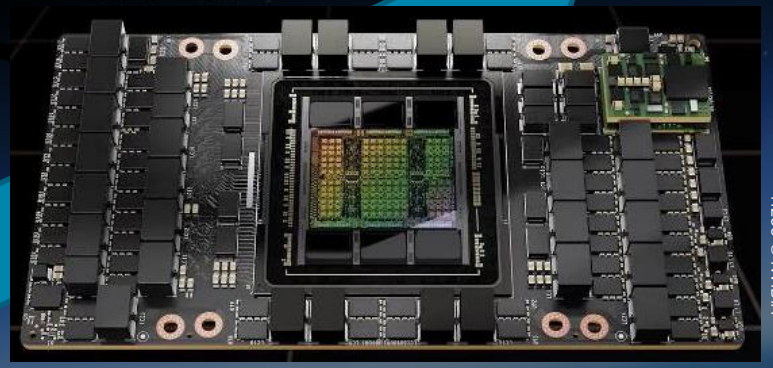
Electric stove
6W/cm²

Air fans, CC BY-SA 4.0 <https://creativecommons.org/licenses/by-sa/4.0>, via Wikimedia Commons
Emmelie Callewaert, CC BY-SA 4.0 <https://creativecommons.org/licenses/by-sa/4.0>, via Wikimedia Commons

AIRBUS

Current

NVIDIA AI GPU H200
800A+



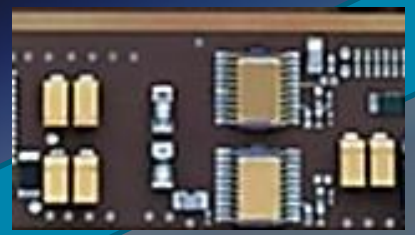
H200 © NVIDIA

20 phases, 40A+ per phase

VERSAL 100A+

4 phases, 25A per phase
GaN transistor

RTG4 12A



2 Phases, 6A per phase

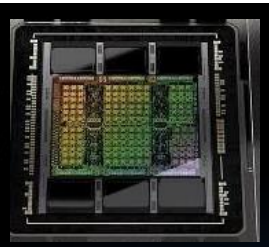
AIRBUS

Data throughputs (per lane)

SpaceWire
~100 Mbit/s, 1995

RTG4
3 Gbit/s, 2016

VERSAL
25 Gbit/s, 2020



H200 © NVIDIA

H200
100 Gbit/s,2022

PCIE 7.0
128 Gbit/s, 2025 (planned)

PCIE 6.0
64 Gbit/s, 2022

PCIE 5.0
32 Gbit/s, 2019

PCIE 4.0
16 Gbit/s, 2017

PCIE 3.0
8 Gbit/s, 2010

PCIE 2.0
4 Gbit/s, 2007

PCIE 1.0
2 Gbit/s, 2003

MIL-STD-1553
1 Mbit/s, 1975

AIRBUS

High Performance Processing Space Electronics

Year	Project	Key Features	Innovations	Applications	View
2019-2021	**ZUP**	**Zynq UltraScale+** MPSoC • Modular extended **6U VPX format** **2xFMC+** digital/mixed mezzanines	**DDR4** introduction at 1,866Gsps **High-speed links 10Gbps** • **16 Layers stack up** (1156pin SoC)	TELEO(1) **GEO optical atmospheric feeder in-flight demonstrator** (1) : **successful in-orbit**	

High Performance Processing Space Electronics

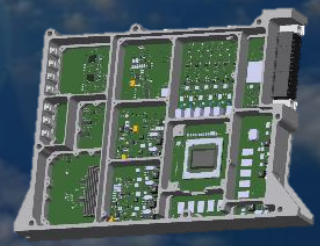
Year	Project	Key Features	Innovations	Applications	View
2019-2021	**ZUP**	**Zynq UltraScale+** MPSoC • Modular extended **6U VPX format** **2xFMC+** digital/mixed mezzanines	**DDR4** introduction at 1,866Gsps **High-speed links 10Gbps** • **16 Layers stack up** (1156pin SoC)	TELEO(1) **GEO optical atmospheric feeder in-flight demonstrator** (1) : **successful in-orbit**	
2020-2022	**KUP**	**KU060 Kintex UltraScale** • **SEL and SEU protection** • Modular extended **6U VPX format** **2xFMC+** digital/mixed mezzanines	**HSSLs signal integrity simulations** • Backdrill introduction • **DDR4** tested at **2.4Gsps** • **22 Layers stack up (1517p SoC)**	• Sunrise **Laser LCT modem technology development** • **Hi-side Hyperspectral compression demonstrator**	

High Performance Processing Space Electronics

Year	Project	Key Features	Innovations	Applications	View
2019-2021	**ZUP**	**Zynq UltraScale+** MPSoC • Modular extended **6U VPX format** **2xFMC+** digital/mixed mezzanines	**DDR4** introduction at 1,866Gsps **High-speed links 10Gbps** • **16 Layers stack up** (1156pin SoC)	TELEO(1) **GEO optical atmospheric feeder in-flight demonstrator** (1) : **successful in-orbit**	
2020-2022	**KUP**	**KU060 Kintex UltraScale** • **SEL and SEU protection** • Modular extended **6U VPX format** **2xFMC+** digital/mixed mezzanines	**HSSLs signal integrity simulations** • Backdrill introduction • **DDR4** tested at **2.4Gsps** • **22 Layers stack up (1517p SoC)**	• Sunrise **Laser LCT modem technology development** • **Hi-side Hyperspectral compression demonstrator**	
2023-2026	**VIP**	**VERSAL SoC** Ready for conduction cooled • **SEL and SEU protection** • 6U VPX format • **High-speed links :** x16 @ 12Gbps+ on backplane 2x12 @ 25Gbps on 2xFMC+ • **Optical links 4x25Gbps**	• Advanced power and thermal management **90W@core and >150W at board** • **24 Layers stack up (2192 p on SoC)** • **Intensive signal integrity simulations** • **Power integrity simulations**	• **Technology demonstrator (3)** • **Use cases and applications developments**	

AIRBUS

High Performance Processing Space Electronics

Year	Project	Key Features	Innovations	Applications	View
2019-2021	**ZUP**	**Zynq UltraScale+** MPSoC • Modular extended **6U VPX format** **2xFMC+** digital/mixed mezzanines	**DDR4** introduction at 1,866Gsps **High-speed links 10Gbps** • **16 Layers stack up** (1156pin SoC)	TELEO(1) **GEO optical atmospheric feeder in-flight demonstrator** (1) : **successful in-orbit**	
2020-2022	**KUP**	**KU060 Kintex UltraScale** • **SEL and SEU protection** • Modular extended **6U VPX format** **2xFMC+** digital/mixed mezzanines	**HSSLs signal integrity simulations** • Backdrill introduction • **DDR4** tested at **2.4Gsps** • **22 Layers stack up (1517p SoC)**	• Sunrise **Laser LCT modem technology development** • **Hi-side Hyperspectral compression demonstrator**	
2023-2026	**VIP**	**VERSAL SoC** Ready for conduction cooled • **SEL and SEU protection** • 6U VPX format • **High-speed links :** x16 @ 12Gbps+ on backplane 2x12 @ 25Gbps on 2xFMC+ • **Optical links 4x25Gbps**	• Advanced power and thermal management **90W@core and >150W at board** • **24 Layers stack up (2192 p on SoC)** • **Intensive signal integrity simulations** • **Power integrity simulations**	• **Technology demonstrator (3)** • **Use cases and applications developments**	
2024-	**VHIPER**	• **VERSAL SoC** • **1xFMC+ connector** • **Conduction cooled** • **Rad-Tolerant**	• **Radiation hardened power solution**	• **Earth Observation** • **Science** • **Telecom / Optical Coms modems**	

AIRBUS

VIP Board technology demonstrator

Modular Format extended 6U VPX

> 90W available on the FPGA

HSSL links

Backplane :

- Connector VPX RT3
- x16 @ 16Gbps+ (target)

FMC+ : 2x12 @ 25Gbps (target)

Backdrill, microvias

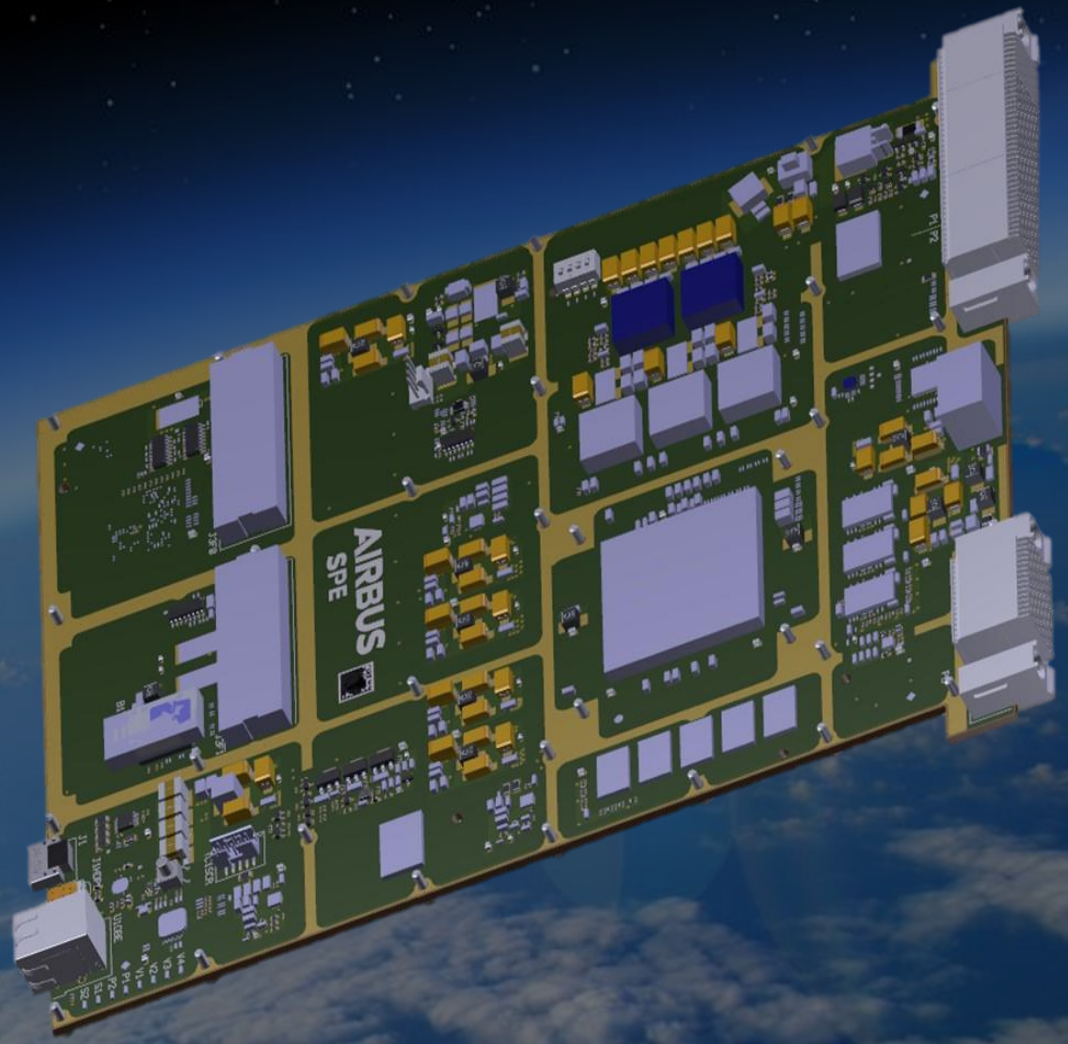
Memory DDR4, 2 banks:

2GBytes DDR4 with ECC, >2.4Gbps x (64bits + 8 bits ECC)

2GBytes DDR4 with ECC, >2.4Gbps x (64bits + 8 bits ECC)

Optical links

module 4x25 Gbps TX/RX



VIP Board technology demonstrator

FMC1 slot

FMC2 slot

Ethernet (GbE)

VPX interface (Power, std IO, High speed)

Commercial Point Of Load

Versal

DDR BK0

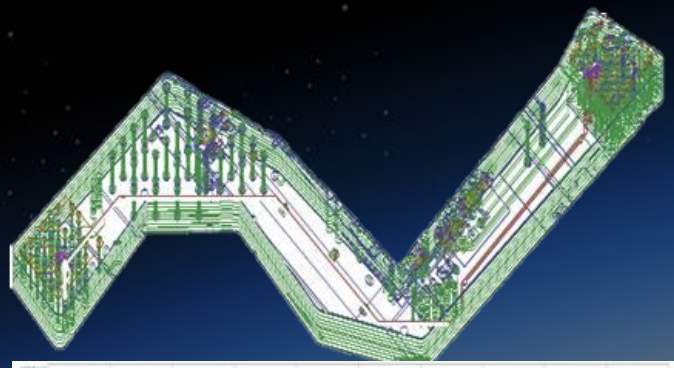
DDR BK1

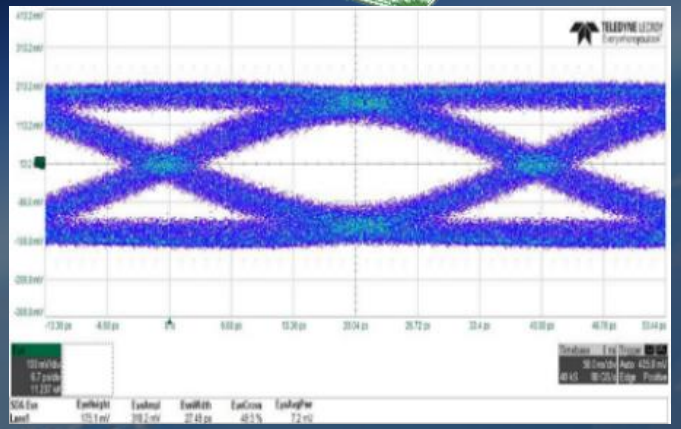
De-risking activities

Versal assembly prototyping (Report & X-rays)

High-Speed Links

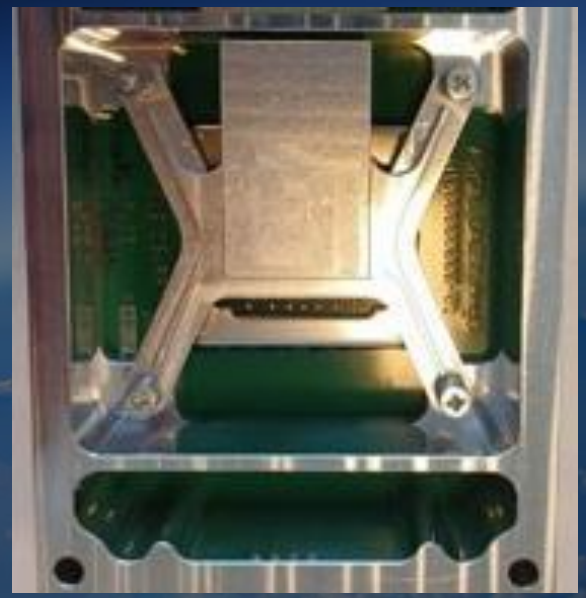
3D PCB Signal Integrity Simulation



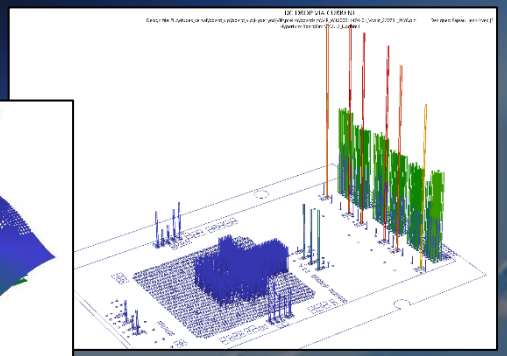


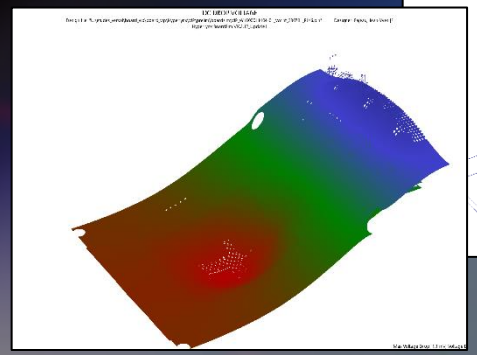
Thermal Dissipation

Mechanical Mockup



Power Integrity





AIRBUS

De-risking activities

EM Board New Space Components GaN Technology Transistors

Output: 800 mV, 100A+

Tested at :

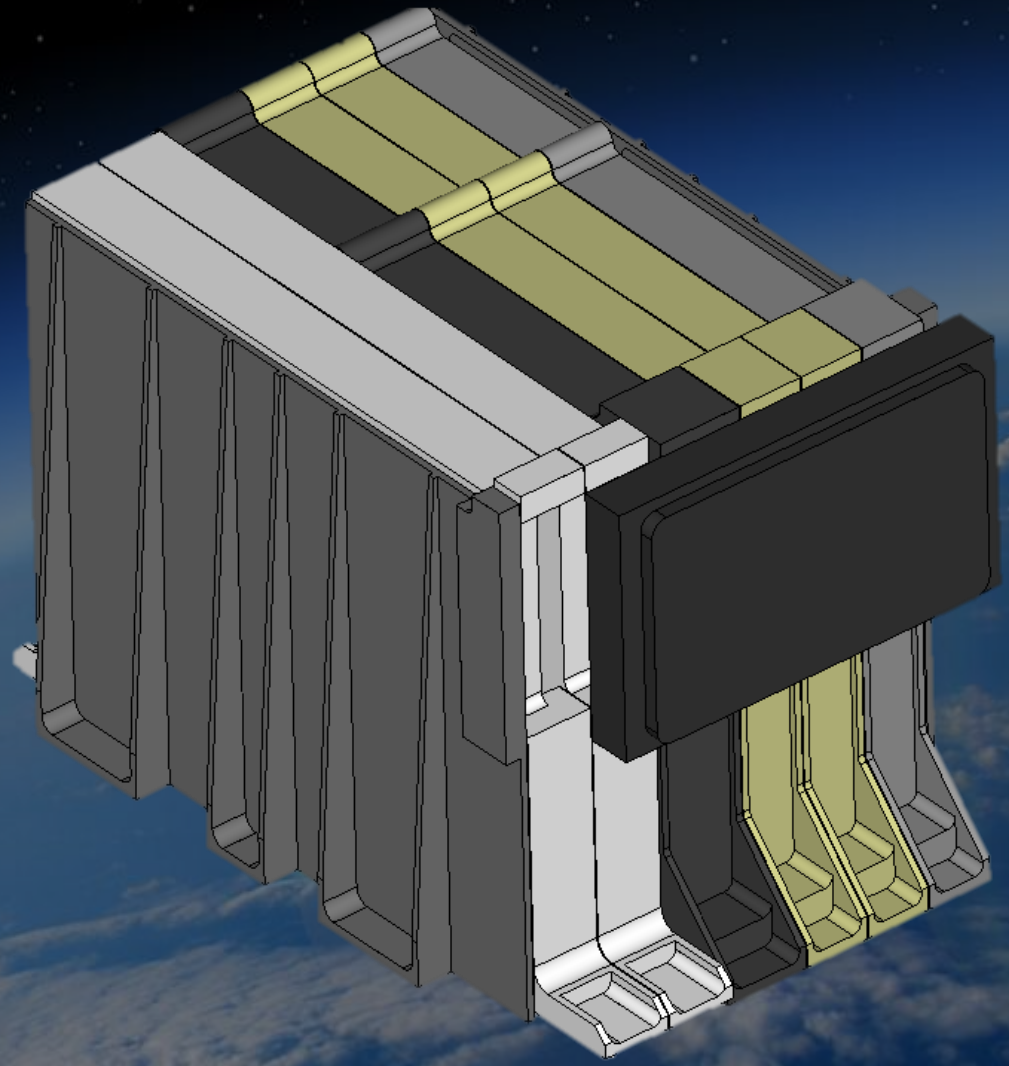
- **Continuous: 100A, 80W DC**
- **Transients: +25A, 200ns rise/fall time**

VHIPER : An operational product EM

Derived from

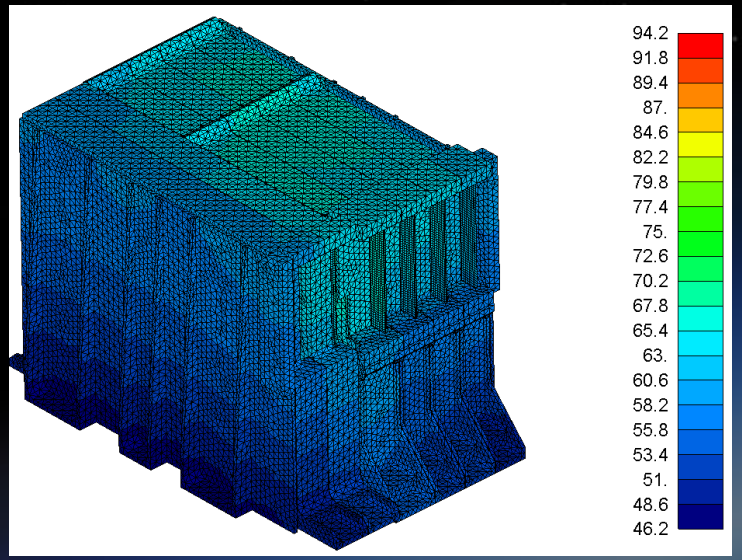
- VIP demonstration
- De-risking activities

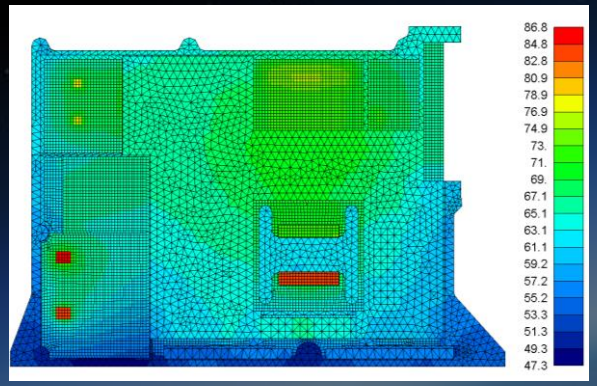
Preparing 1st Versal-based EM product

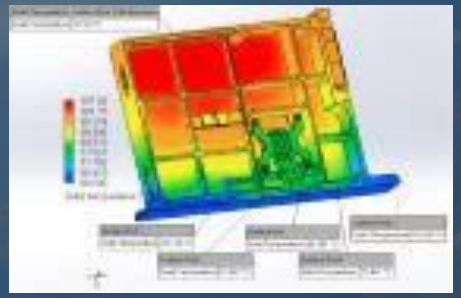


VHIPER EM preparation

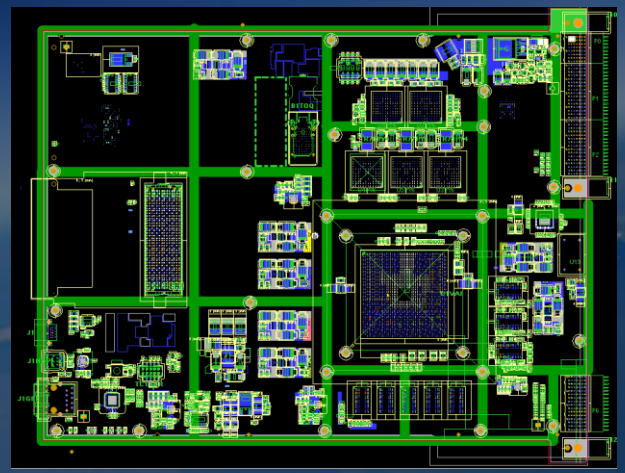
Detailed thermal bord and equipment architecture



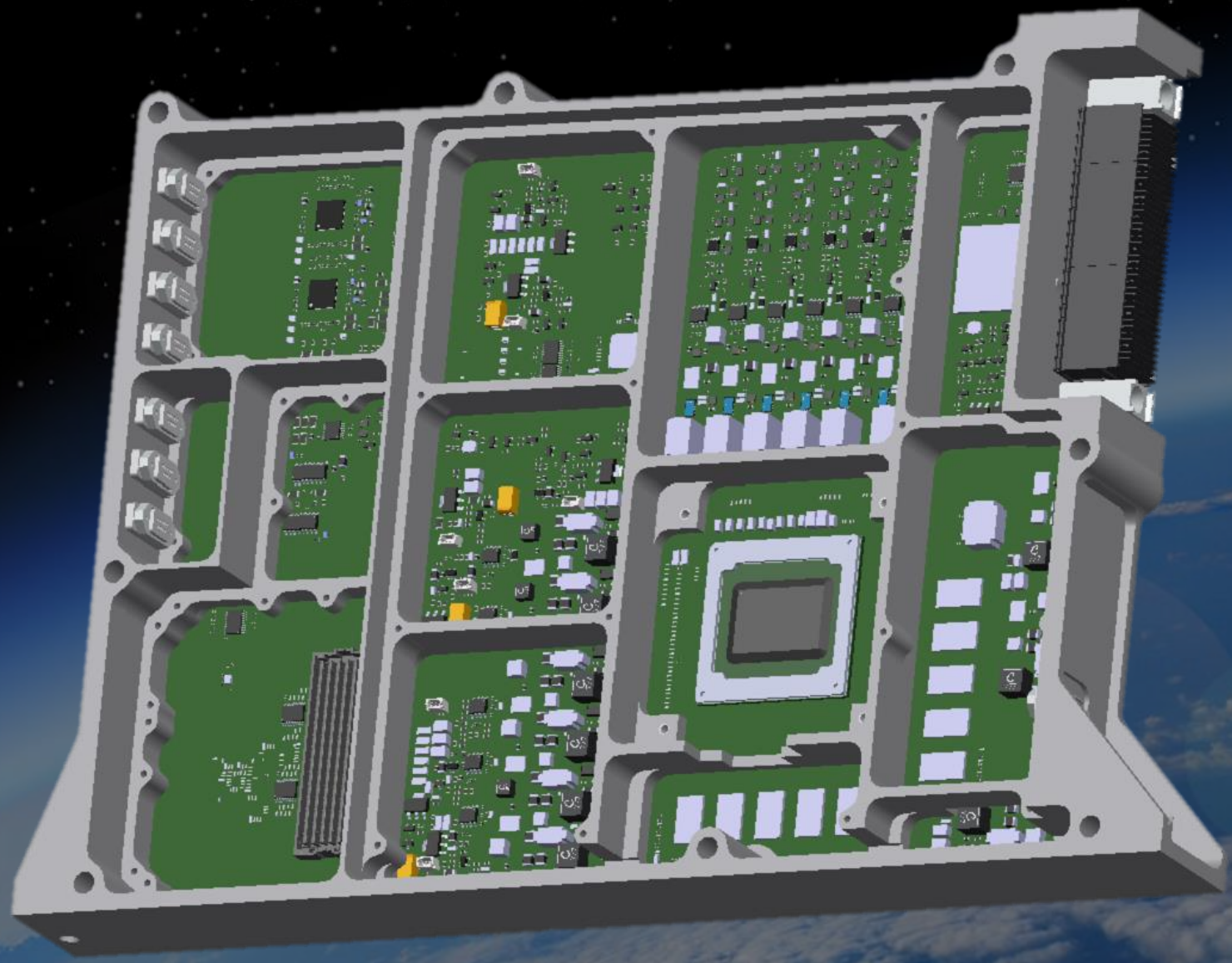




Boards layout



VHIPER EM preparation



Thank you

AIRBUS