

LEOSG: : RFSoc Based Navigation Payload Signal Generator Demonstrator for a Future LEO-PNT System

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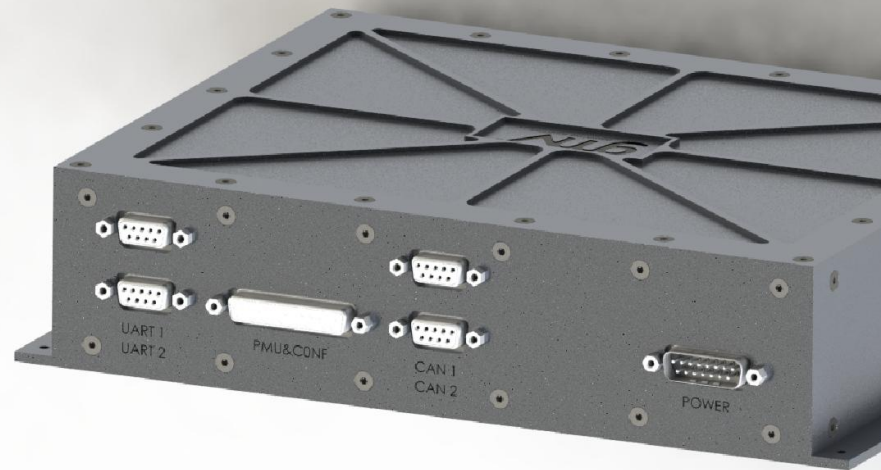
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Contents

Introduction

Background

Roadmap

Innovation aspects

Environmental assessment

Conclusions and future work

GMV: A global technology group

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Multinational
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**Private
capital**



Headquarters in
Spain (Madrid).

**Subsidiaries in
12 countries**
(ops in 70+)

+3,500
employees

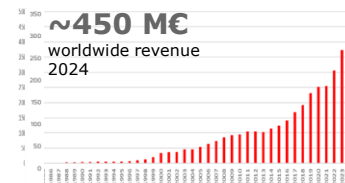


Roots tied to the
Space and
Defence industry

Engineering,
development and
integration of systems,
software, hardware,
specialized products
and services



Aeronautics, Space, Defense
& Security, Cybersecurity,
Intelligent Transport
Systems, Healthcare,
Banking & finances, and ICT
industries



Space



Aeronautics



Defense &
Security



Telecommunication



Cybersecurity



Intelligent Transport
Systems



Healthcare



Public Sector and Corporate
ICT



Banking &
Finances

GMV Space Technological Leadership



#1 Worldwide

Satellite Control Center provider to commercial telecom operators.

Primary SST technology and Operation Centers



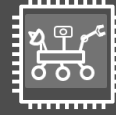
Space Segment

GNC technology leader
On-board Autonomy
On-board SW
Space Equipment

Test Facilities



Prime role in **European GNSS Systems** and its safety critical systems (EGNOS and Galileo)



Leading European Space Robotics technology, growing Microelectronics, HW Avionics and Technology Transfer



Excellence in Flight Dynamics, Mission Analysis, E2E Simulators, EO Data Processing and downstream geospatial services

Introduction

LEO-PNT constellations

Low Latency

Reduced signal travel time compared to MEO/GEO systems.

Higher Bandwidth

Supports more data-intensive applications.

Stronger Signal Power

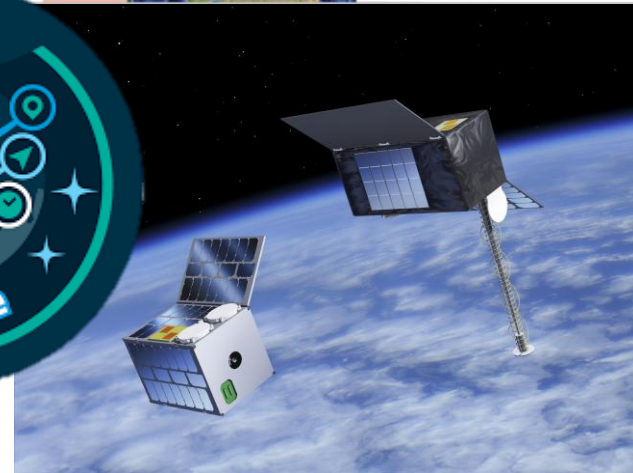
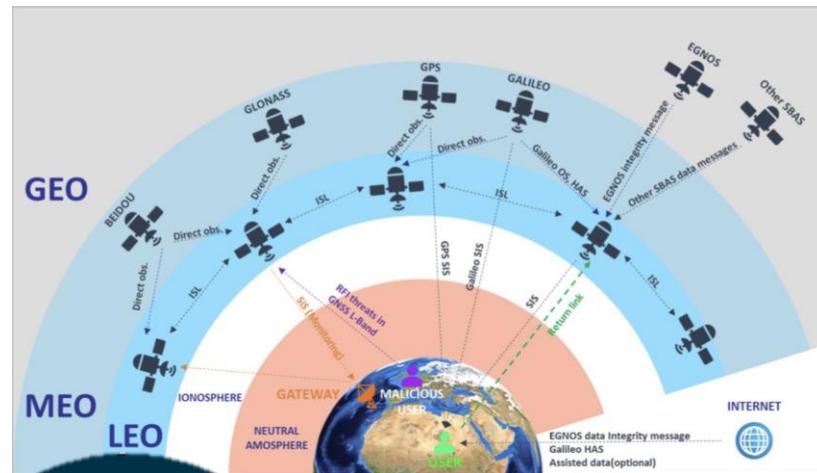
Improved link budget and robustness.

Reduced Noise

Better signal-to-noise ratio for navigation.

Improved Accuracy

Enhanced positioning performance for PNT services



Traditional SDR vs RFSoc Architecture

Traditional navigation uses SDRs and analog circuits, while RFSoc integrates digital and analog components in one chip.

Traditional SDR Approach	RFSoc-Based Architecture
Separate FPGA/SoC + external DAC/ADC modules	Integrated DACs/ADCs on the same silicon as FPGA and CPU
Requires additional analog circuits (mixers, PLLs)	Direct RF output up to 6 GHz (no external upconversion)
Higher size, weight, and power (SWaP)	Lower SWaP and footprint
Increased design complexity and latency	Real-time signal parameter reconfiguration, reduced latency and interface overhead
Limited real-time reconfigurability	Real-time signal parameter reconfiguration

LEOSG EM Signal Generator

Core Platform:

Xilinx Zynq UltraScale+ RFSoc (ZU48DR)

Key Features:

- Integrated DACs/ADCs for direct RF output up to 6 GHz.
- Real-time reconfigurability for emerging signals and modulations.
- On-board monitoring and error mitigation mechanisms.

Architecture Highlights:

- Processing System (ARM cores) for control and telemetry.
- Programmable Logic with Versatile Signal Generator (VSG) IP
- Embedded RF data converters and high-stability clock subsystem.

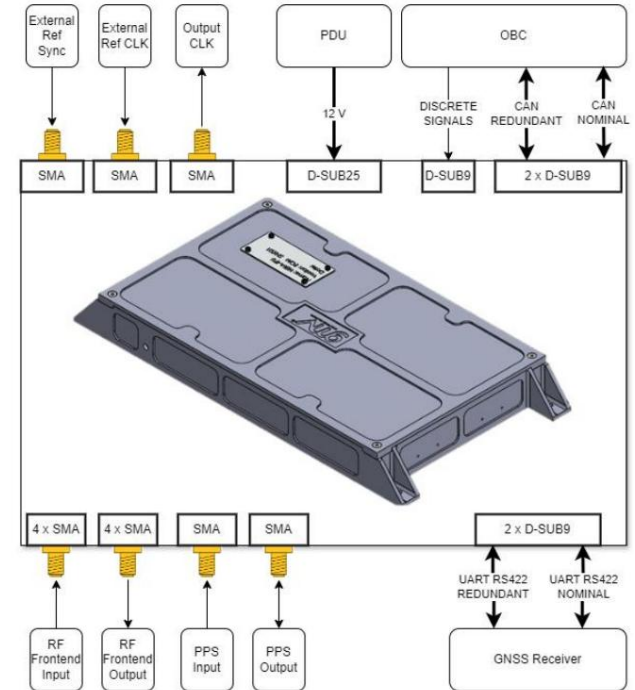
Flexibility:

Supports L-band, S-band, and configurable for UHF.

TRL Goal:

From EM (TRL6) toward EQM/FM (TRL8).

High-performance RF signal generator for LEO-PNT navigation payload signal generation.



Background

Overview of SING Project

- **Purpose:**

- Demonstrate a single-chip GNSS signal generator for E1, E5, and E6 bands.

- **Platform:**

- Xilinx ZCU208 board with Zynq UltraScale+ RFSoc (ZU48DR).

- **Key Features:**

- High flexibility for future signals and modulation schemes.
- Optimized for power consumption in navigation payloads.

- **Capabilities:**

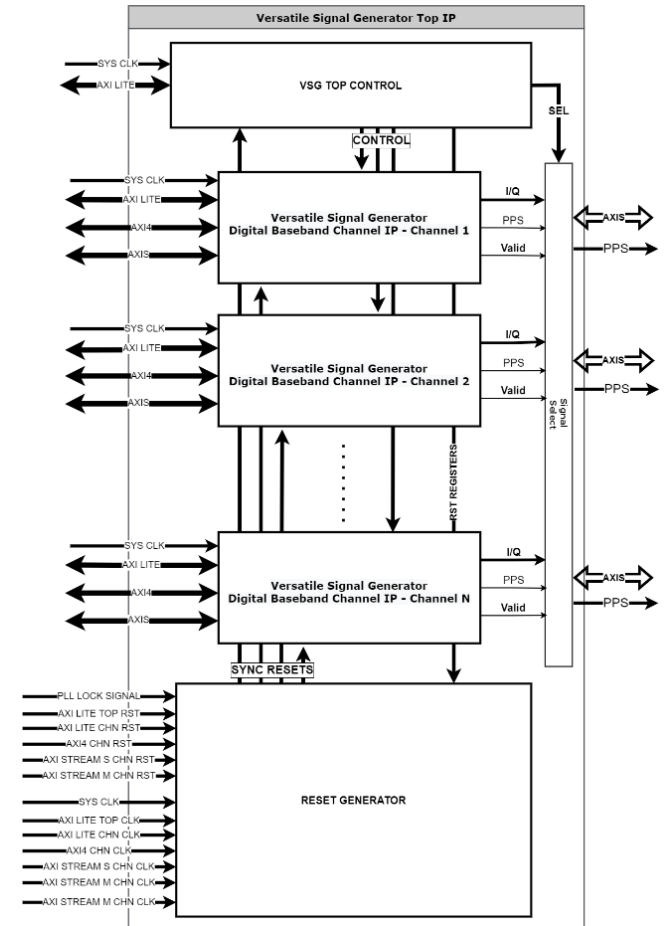
- Generation of up to 128-QAM signals and GNSS-specific signals at baseband and RF.

- **Identified Limitations:**

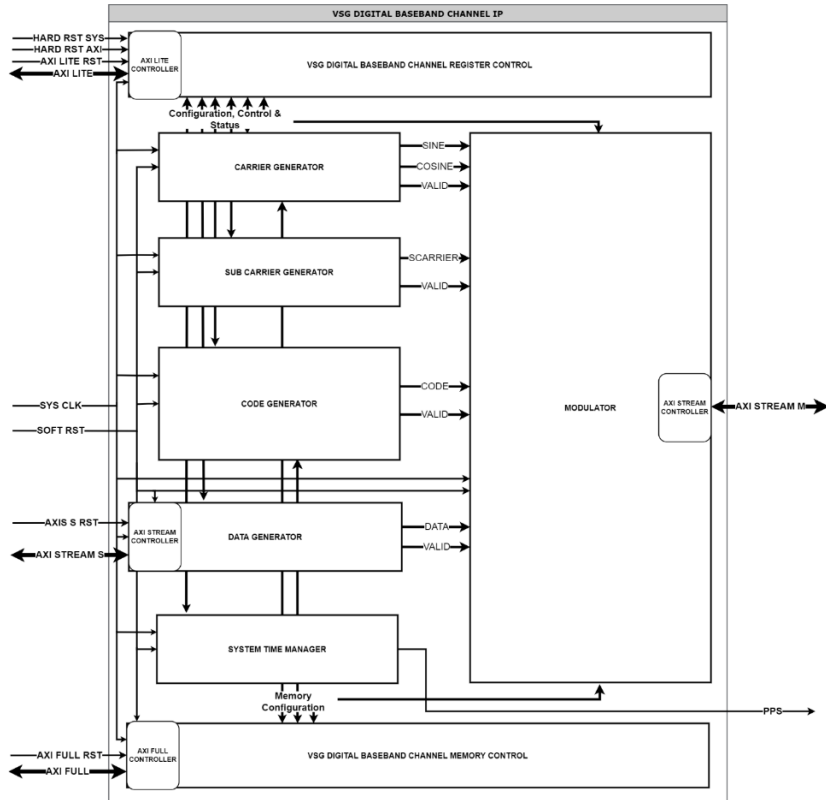
- Limited real-time reconfigurability.
- Degraded SNR due to hardware constraints.
- Suboptimal FPGA resource allocation → higher power consumption.

Overview of VSG IP in SING

- VSG top IP vendor agnostic design
- Parametrizable design by generics to adapt to application and device requirement
- Support for different clock domains for each channel/interface
- Scalability from 1 to N VSG digital baseband channels
- Easy control of the N channels through a single AXI interface
- Vectorized inputs and outputs to automatically generate interfaces



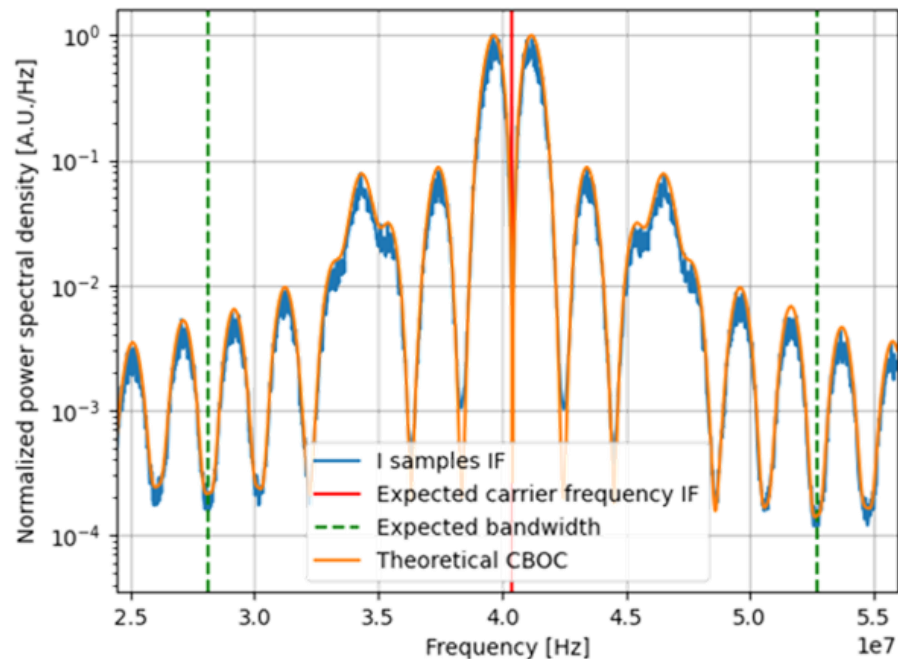
Overview of VSG IP in SING



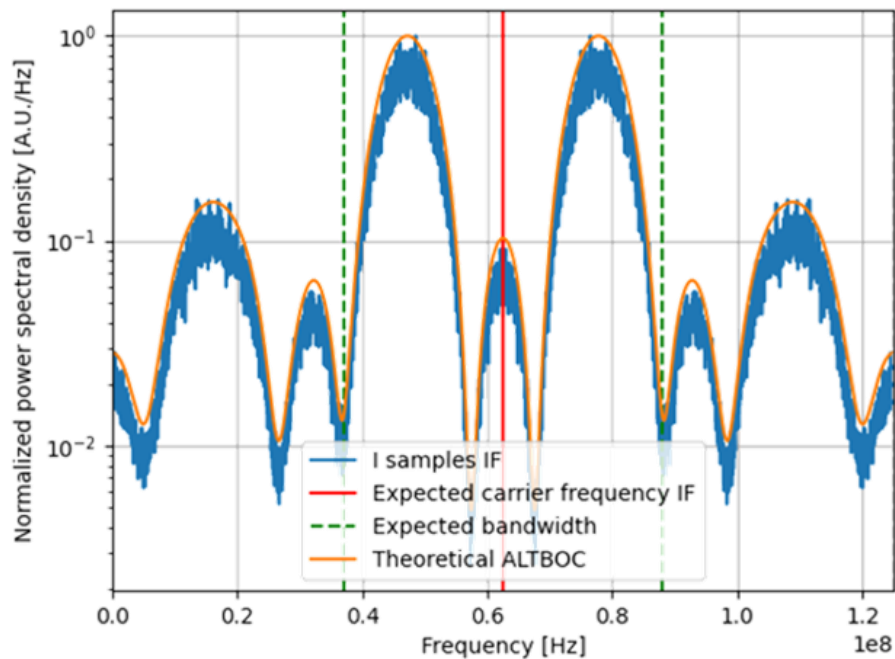
- Fully configurable VSG Digital baseband channel through AXI Interfaces
- AXI Lite for register configuration, AXI4 for internal memory transaction, AXI Stream for Navigation data input and Modulated output to RF chain
- Programmable Carrier (NCO, LUT values and gain)
- Programmable Sub Carrier (NCO, size and period)
- Programmable Code generator
- 7 (by default) simultaneous code bits for 128QAM modulation support
- XOR combination of Primary LFSR, Secondary LFSR, Primary LUT and Secondary LUT
- Configurable code NCO, Primary and secondary Periods, initial Periods, Polynomials, seeds and initial seeds
- Code independent enables
- Pilot XOR Data independent configuration
- Programable Navigation Data Generator (NCO and periods)
- Programmable Modulator (Number of modulation bits, configurable Pilot&Code combination, configurable subcarrier modulation bits, Configurable LUT symbol map)

Achieved results with SING

Galileo E1 baseband spectrum



Galileo E5 baseband spectrum



Roadmap

Roadmap

- **Project Development Stages**

- The LEOSG project progresses from the initial EBB model to the Engineering Model and future qualified models.

- **Technology Readiness Levels**

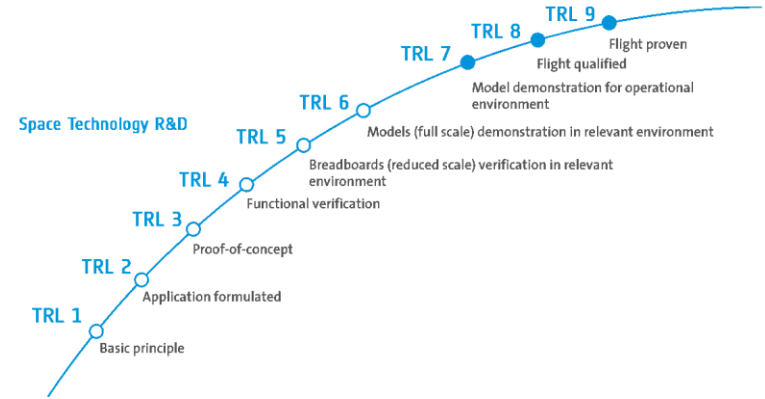
- The roadmap follows ESA's TRL framework, advancing from TRL4 to TRL6 and aiming for TRL8 for space qualification.

- **Technical Refinements**

- Key developments include consolidating RFSoc knowledge, refining hardware design, and optimizing GNSS Signal Generator IP.

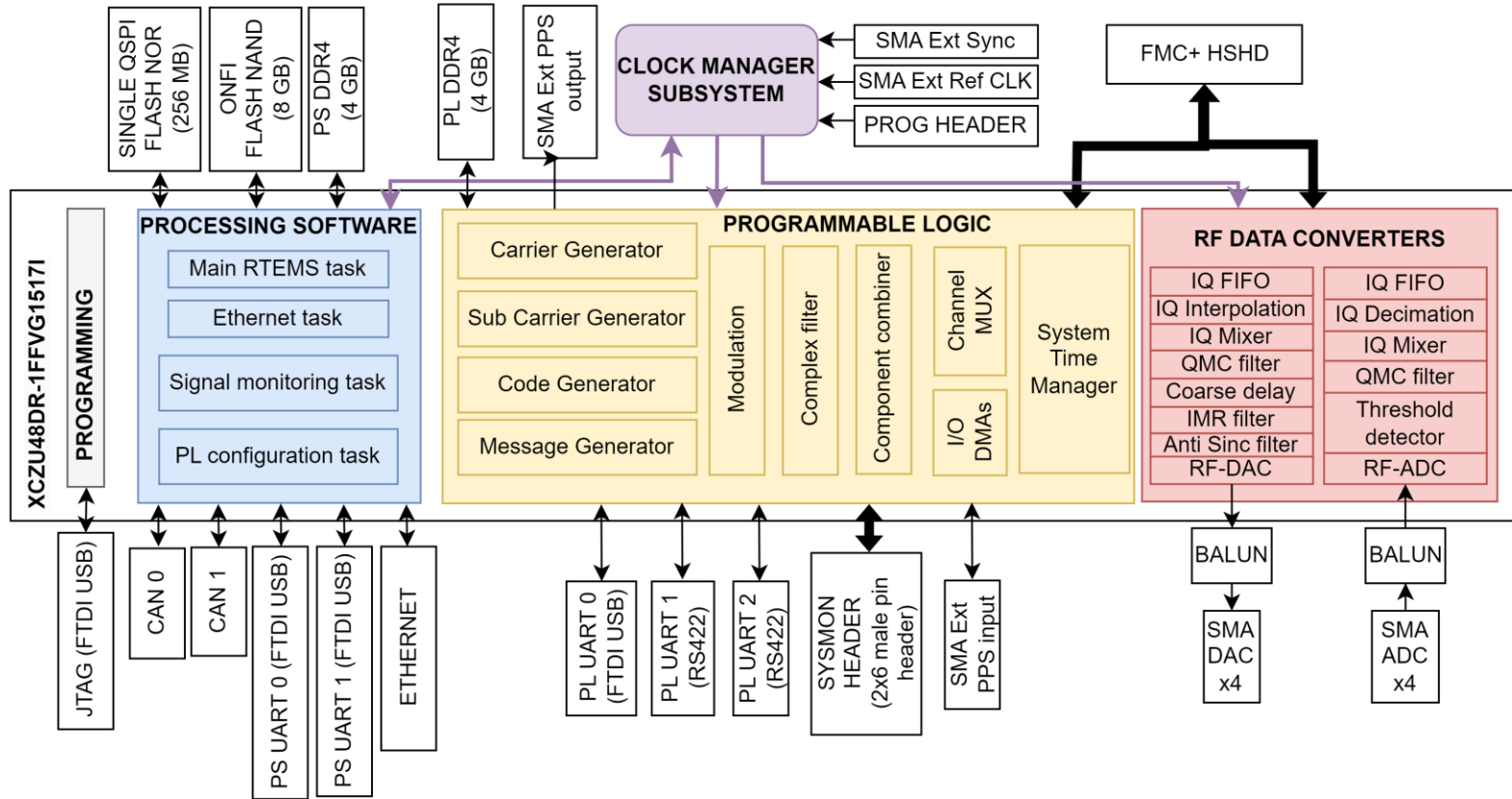
- **Mission Qualification Goals**

- Strategic steps ensure LEOSG meets requirements for LEO-PNT space mission deployment and qualification.



Innovation aspects

LEOSG architecture



Processing software



Role of PS Software

- TM/TC Communication with the OBC (CAN -> CSP -> PUS)
- Real-time operational control of signal generation.
- Low-latency, high-throughput communication with PL (same RFSoc device).

RTEMS-Based Implementation

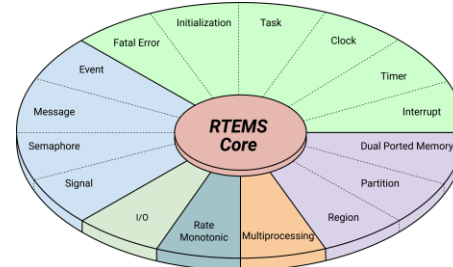
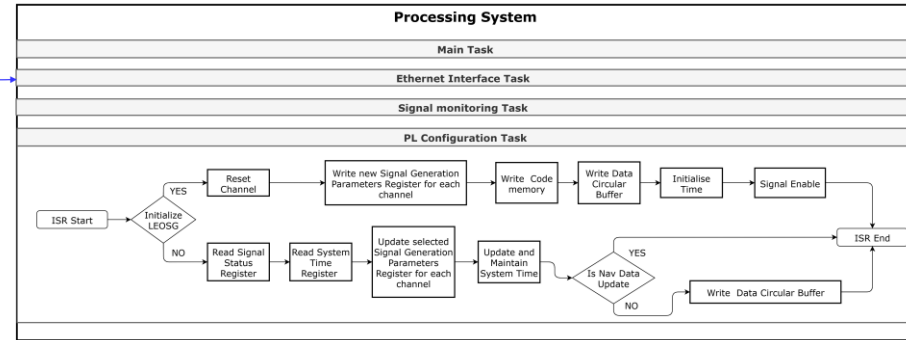
- Thread-safe design for precise timing and safe HW access.
- Xilinx RF data converter, clock management, and drivers ported to RTEMS.

Runtime Flexibility

Allows dynamic modification of complex IP configurations.

Key Features

- Initialization of LUTs for carriers, codes, and modulation symbols.
- Control register configuration with transparent memory management.
- Signal and system monitoring for quality assessment.
- Configuration memory, PS and IPs integrity
- Mutual exclusion for hardware access (thread safety).
- Periodic navigation data delivery.



Programmable logic

Architecture Basis:

- Built on Versatile Signal Generation (VSG) IP (GMV VHDL-based).
- Integrated with XCZU48DR RFSoc RF data converters.

Origin & Validation

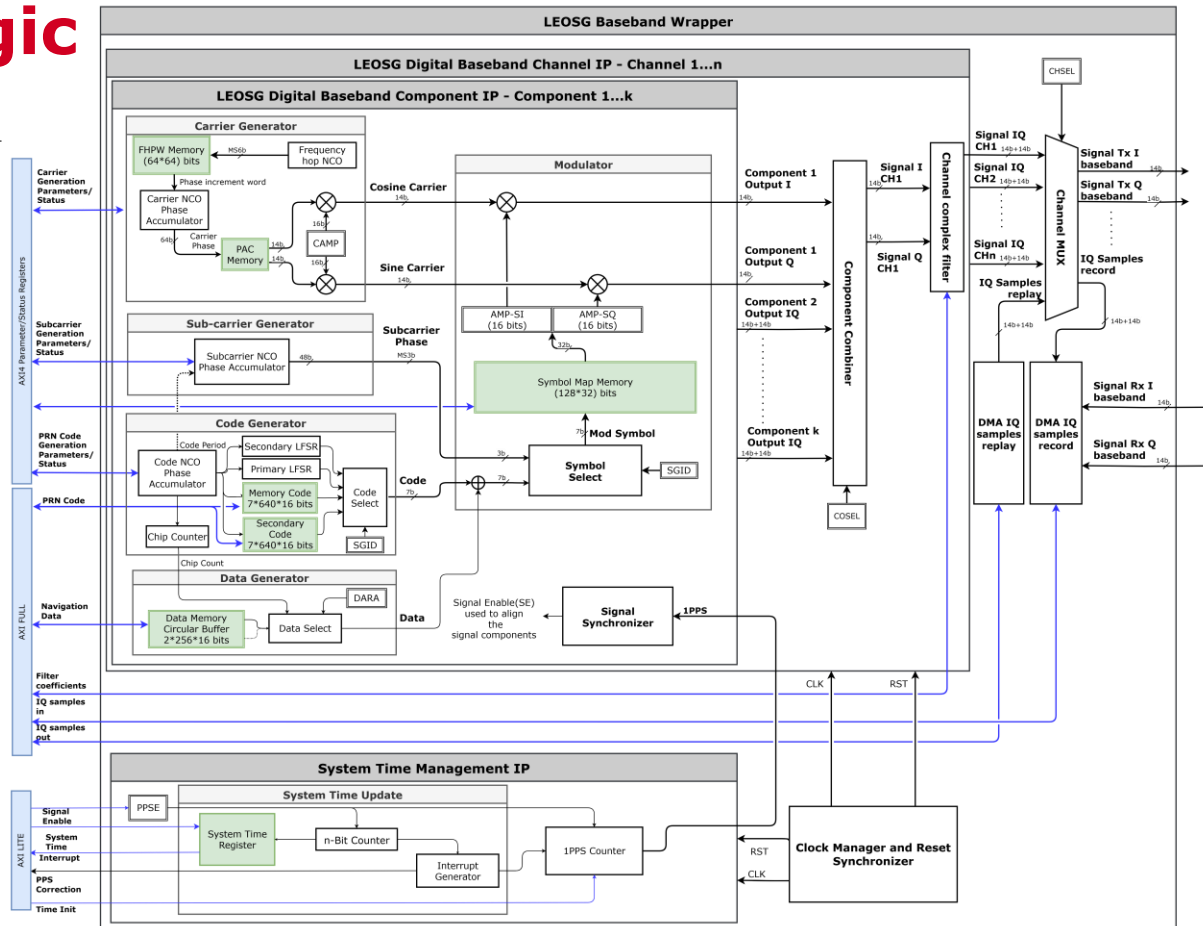
Developed under SING project, validated on Xilinx ZCU208 board.

Primary Objective

- Generate LEO-PNT GNSS signals in L-band and S-band.
- Flexible configuration → supports UHF band (per LEO-PNT SIS ICD).

VSG updates form SING:

- Carrier Generator: Digital sine/cosine carriers, NCO with FHSS support.
- Channel organization (each channel is composed on 3 baseband component generators + component combiner)
- System Time Manager (STM): STU + 1PPS generator for synchronization.
- Component Combiner: Summation of signal components.
- Channel Multiplexer: Routes IQ streams to DACs.
- Complex modulation on I and Q
- Channel Baseband complex Filter: Band-pass filtering & distortion pre-compensation.
- DMA Modules: IQ sample injection/retrieval for testing & monitoring.
- AXI interface optimization (the entire design uses 1 AXI + 1 AXI Lite + N AXI Stream {one per channel})



Clock manager subsystem

Precise reference input clock

10 MHz OCXO: Holdover $\pm 1.5 \mu$ sec over 8 hours, PhaseNoise10kHz [dBc/Hz] -154 dBc/H

External reference clock

Possibility to switch between OCXO and external reference clock input

Dedicated Clock Input per Tile

Each RF-ADC or RF-DAC tile has its own clock input.

No Additional Clock Buffer Required

Current-Mode Logic (CML) clock input buffer already integrated in tile architecture.

Clock Input Usage

Can serve as sampling clock or PLL reference for the tile.

CML Clock Characteristics

On-die differential termination of 100 Ω .

On-Chip Clock Distribution

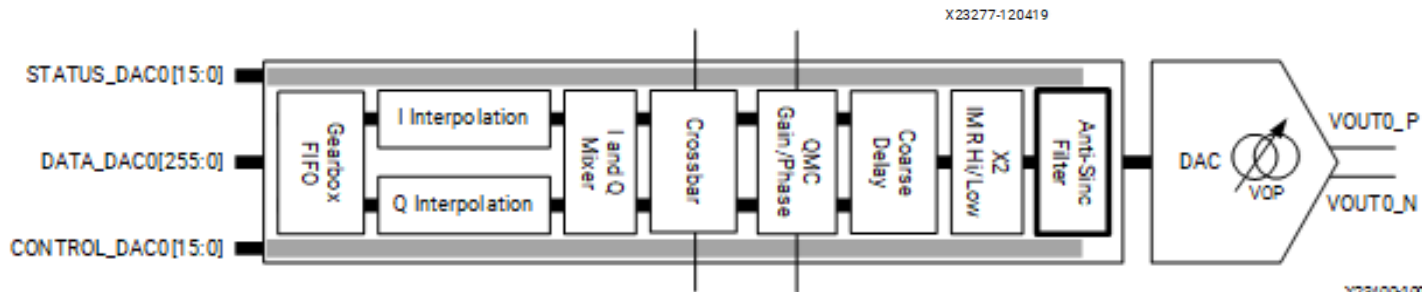
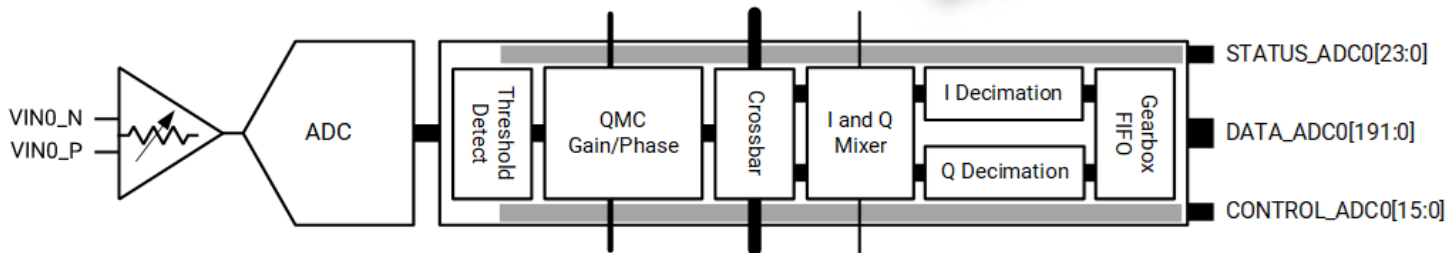
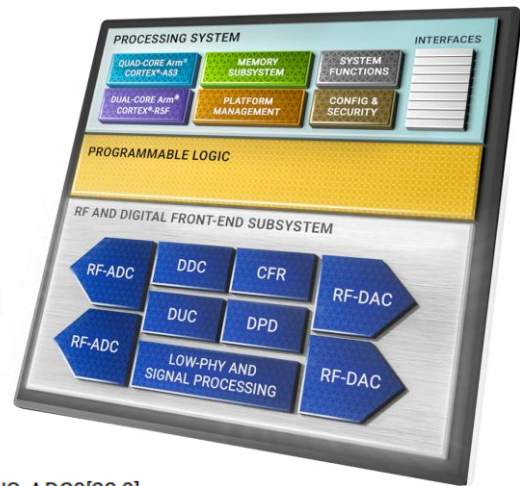
Enables forwarding of clock signals between adjacent tiles within converter groups.

Clock Source Options

Forwarded clock can be external reference or PL-generated.

RF-Data converters

LEOSG integrates high-speed DACs and ADCs within the same silicon die, reducing complexity, latency, and power use.



Proposed EQM optimizations

EQM modifications

Hardware and VHDL design optimizations that can decrease size, weight and Power consumption up to 60%

- Fit the hardware design to LEOPNT requirements reducing processing capabilities
- Remove the DDR4 of the PL and reduce the performance of the DDR4 of the PS
- Remove Debug interfaces as PS/PL UARTS and ethernet
- Replace OBC CAN communication interface by SpaceWire
- Currently in progress optimizations in AXI infrastructure and configuration registers will significantly decrease the logic resources and the power consumption of the RFSoc

Replace COTS component by Low power Space Qualified counterparts

Applies ECSS-Q-ST-70C in manufacturing and assembly processes

Environmental assessment

Environmental Assessment

Suitability for Space Missions

RFSoc devices are evaluated for use in LEO space missions with low radiation tolerance and short duration.

Digital and Analog Component Analysis

Radiation tests show promising digital component results, with further analysis required for the analog RF chain.

Fault Mitigation Strategies

Ongoing campaigns focus on fault mitigation to ensure reliability of RFSoc devices in harsh space environments.

Conclusions and future work

Conclusions & Future Work

Project Feasibility Demonstrated

LEOSG proves RFSoc technology is effective for navigation payload signal generation in LEO-PNT systems.

Engineering Model Features

Incorporates real-time reconfigurability, adaptive modulation, and low SWaP for space mission viability.

Future Work and Testing

Focus on RF characterization, radiation testing, multi-channel support, and frequency band expansion.

Advancing Towards Flight Models

Aims to achieve TRL8 flight models for resilient navigation payloads in next-generation LEO constellations.

Thank you