PrAICC : A Predictible Inter-Core Communication Model for AMP Systems

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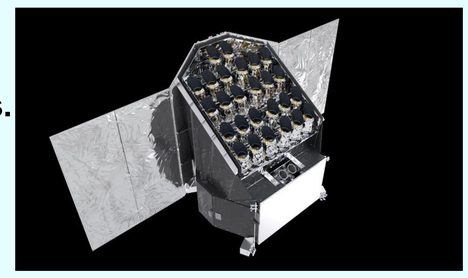
1 - Plato

OBJECTIVE:
Detect and characterize exoplanets by accurately monitoring changes in the brightness of hundreds of thousands of stars.

- **Data from the 24 N-cameras is handled onboard by dual-core GR712RC boards.**
- **GR712RC software is implemented in an AMP architecture with GERICOS.**



2 – Asymmetric MultiProcessing (AMP)

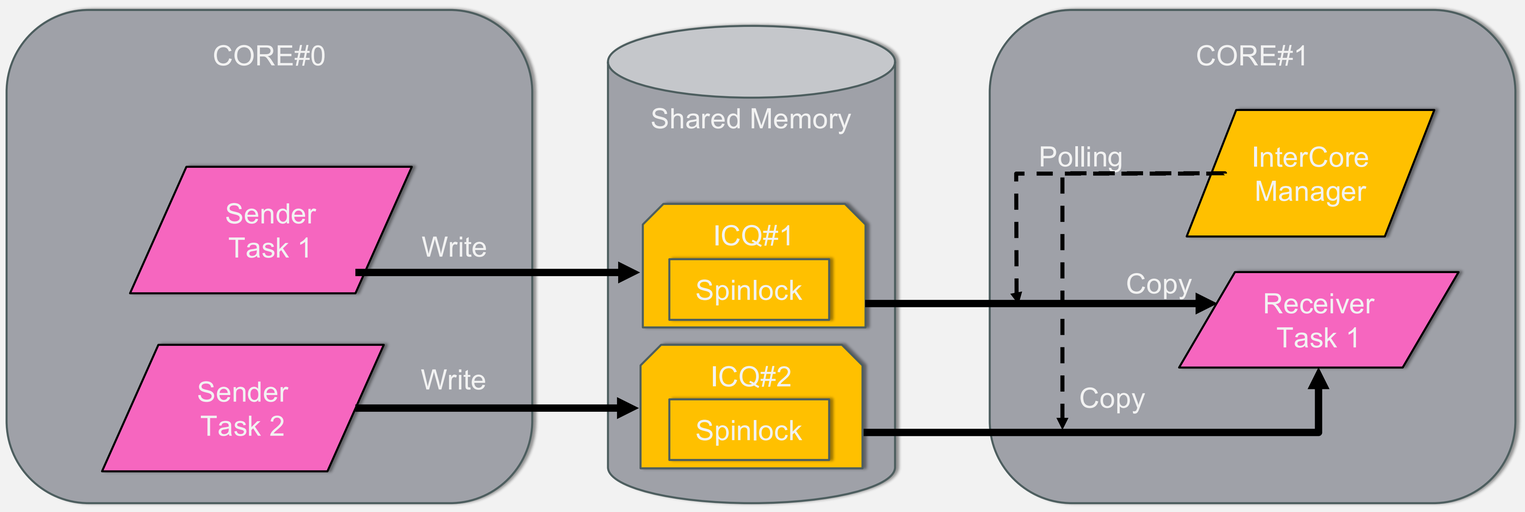
- **Each core is independent and has its own application and Operating System (OS).**

Resource Management	Complex Development
Heterogeneity of cores Memory Management Suitable for hard real-time systems	Applications must coexist on the same hardware (sharing resources and memory space). Inter-core communication requires mechanisms not provided by OS. OS are independent, so FIFO and priority-ordered spinlock cannot be used.

3 – Problem Statement

- **OS may differ from core to core, then the inter-core communication model must be OS-independent.**
- **The architecture and the analysis assume unordered spinlock.**
- **PrAICC: a predictable and portable inter-core communication model for n-core AMP architectures.**

4 - PrAICC



Unordered Spinlock Analysis Approach

Only 2 tasks can lock the spinlock of an ICQ (sender task or ICM).

The task A owns the spinlock, and the task B waits. The locking instructions are atomic (CASA), so they guarantee that the next owner task will be task B, even if task A tries to relock it immediately.

Task B spinning time is bounded by the critical section time of the task A.

InterCoreQueue (ICQ)

ICQ stores inter-core messages between a sender and a receiver. Protected by an unordered spinlock.

InterCoreManager (ICM)

ICM periodically checks the ICQs (polling) of its receiver tasks and forwards messages to them.

Metrics to predict

1. $WCRT_{ICM}$ = f(spinning time, message number to handle).
2. $WCRT_{Sender\ task}$ = f(message size, spinning time).
3. Best inter-core communication latency = f(ICM period).
4. Worst inter-core communication latency = f(ICM period, $WCRT_{ICM}$).

5 – Evaluation

- **Objective: Predict the WCRT of the ICM depending on its period**
- **Environment**
  - **Quad-core GR740 (radiation hardened multicore, Gaisler).**
  - **Core 0: 1 InterCoreManager + 3 receiver tasks.**
  - **Core 1, 2 and 3: For each receiver, one sender task is placed on each core that will send it a message.**

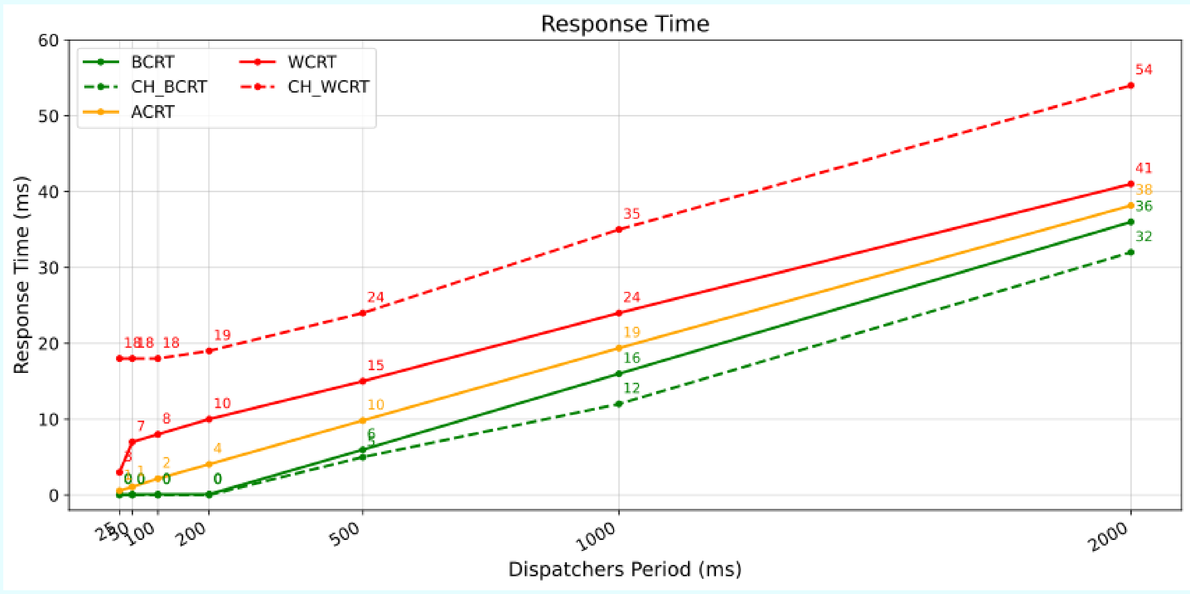
- **Analysis**

$$WCRT_{ICM_k} = max(spin_{ICM_k(i)}) + MaxDispMsg_{ICM_k(i)} + WCET_{ICM_k}$$

Maximum spinning time
+
Maximum time to handle messages at each execution
+
Worst case execution time with no message to handle

$$BCRT_{ICM_k} = MinDispMsg_{ICM_k(i)} + BCET_{ICM_k}$$

Minimum time to handle messages at each execution
+
Best case execution time with no message to handle



Results

1. Measurement of the response time on GR740 are lower than $WCRT_{ICM}$
2. $WCRT_{ICM}$ pessimism is related to the maximum spinning time

6 - Conclusion

- **A predictable OS-independent inter-core communication model for n-core AMP architecture.**
- **Evaluations demonstrate the predictability of PrAICC. $WCRT_{ICM}$ pessimism is related to the maximum spinning time.**

7 – Future Works

- **Extend PrAICC with n–to-n communications.**
- **Implementation and experiments with an heterogeneous SoC (e.g. Versal).**

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