INNOVATING NEW SPACE FRONTIERS

European Commission

Modeling Latency and Energy Trade-offs in Emerging Space Edge Computing Architectures

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ThalesAlenia Space · nano avionics · LSS Large Space Structures · mbi · cnrs · Universität der Bundeswehr München · Université de Rennes · Heriot Watt University

Current ecosystem and challenges

Telecommunication satellites face:

- Increasing amount of users
- Increasing diversity of users
- Increasing demand for low latency

Observation satellites face:

- Increasingly powerful sensors
- Sparse base stations

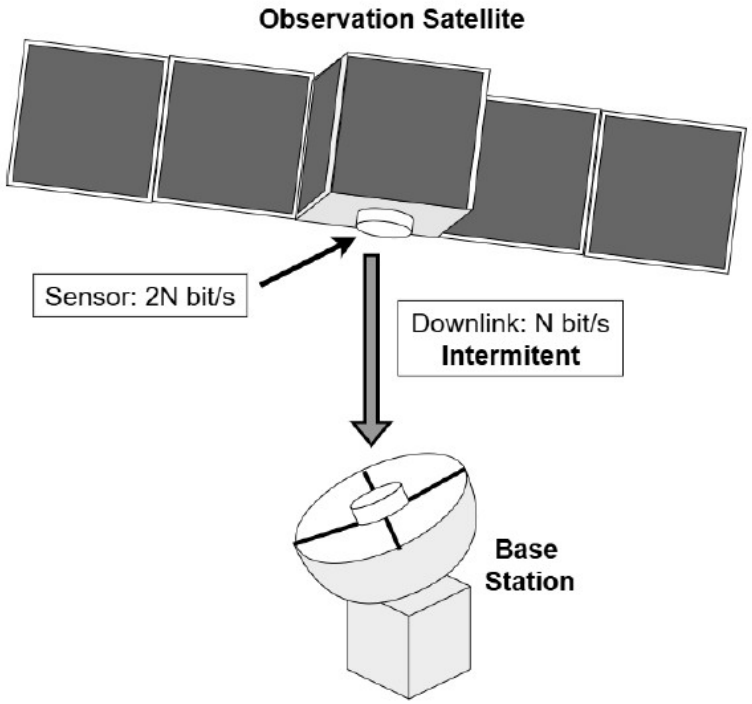


Figure 1: Downlink Bottleneck

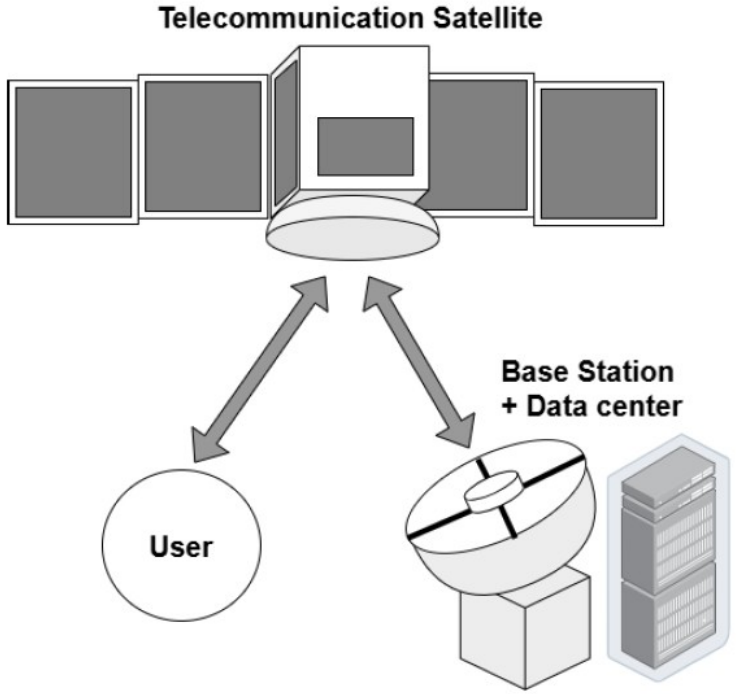


Figure 2: Bent-Pipe Limitations

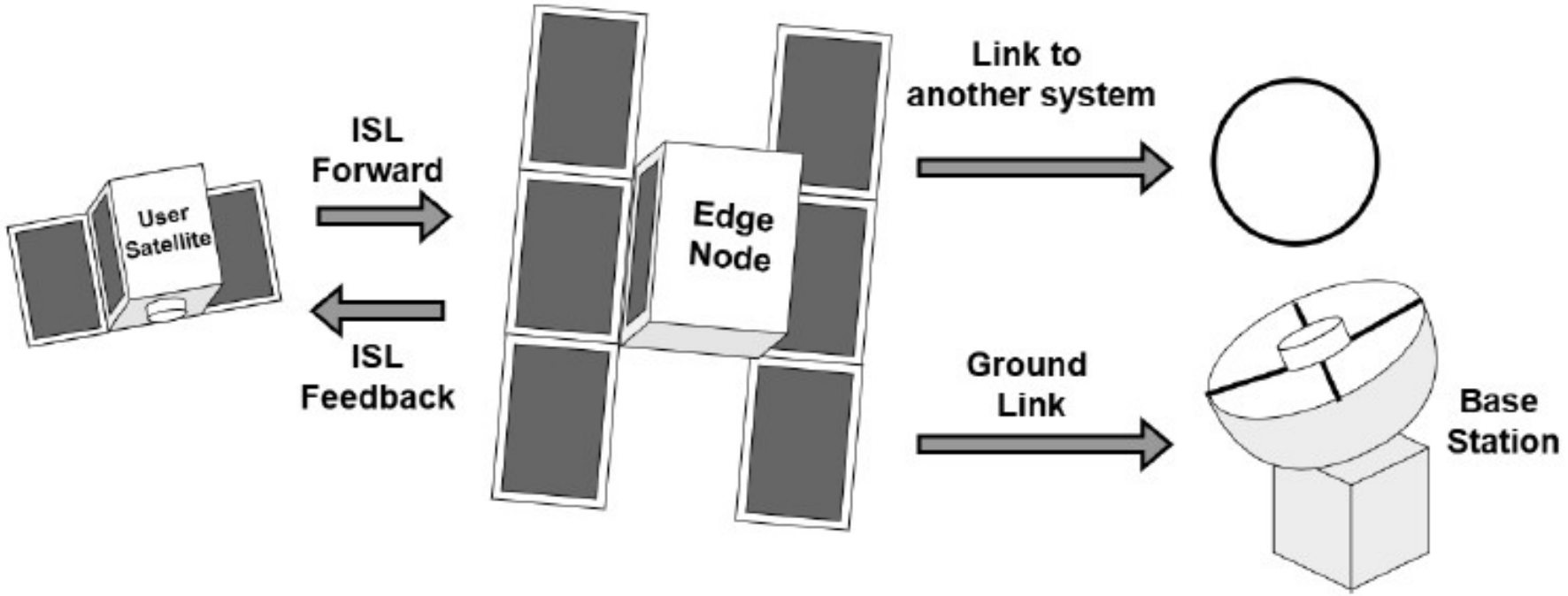
Additional challenge: Increasing processing power on-board a satellite increases constraints on SWaP

→ Space Edge Computing aims to bring more processing power in orbit, near the data sources

What does SEC bring?

Space Edge Computing relies on the concept of « Edge Node » (Computing as a Service)

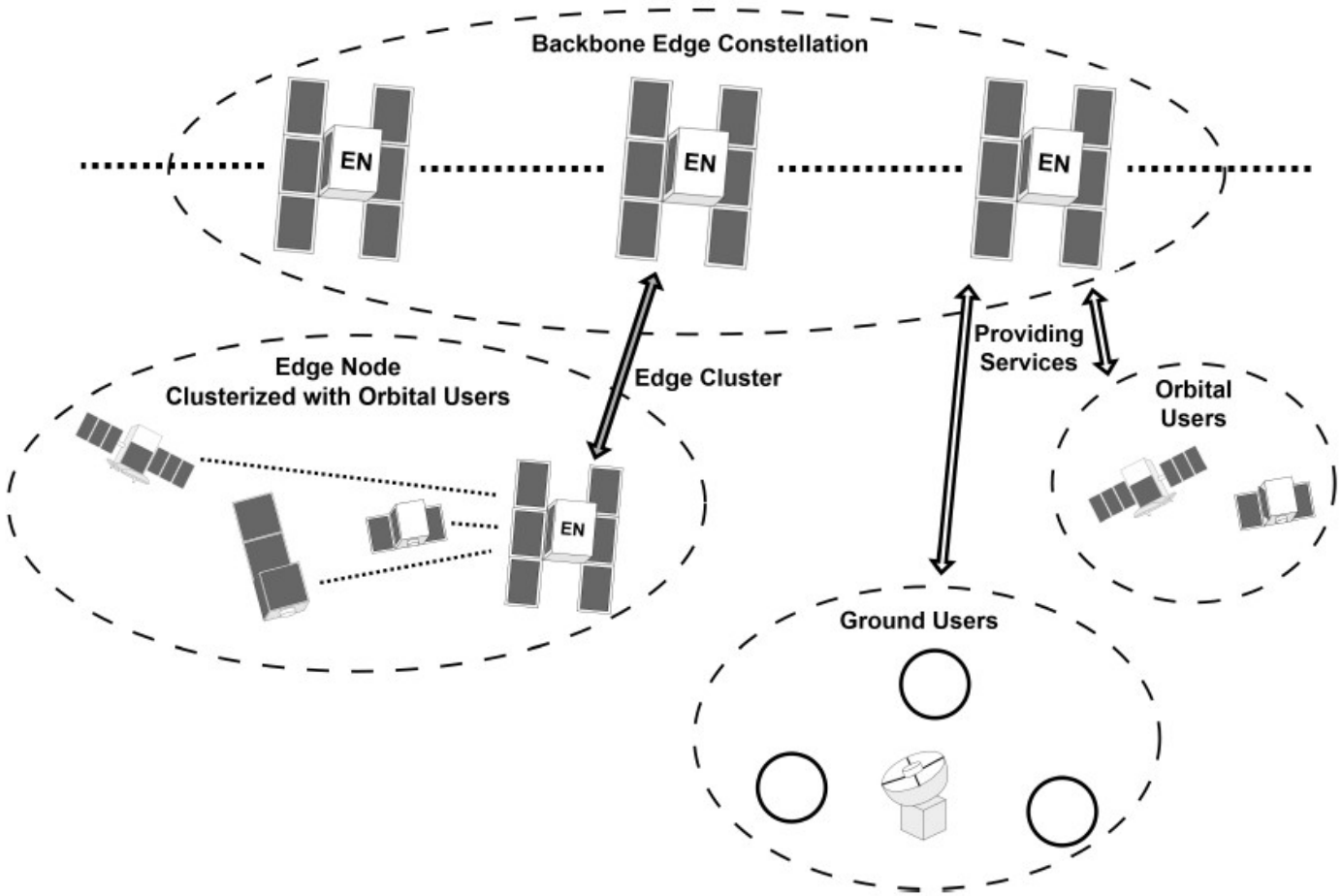
- Edge Nodes are satellites with large amounts of processing power as payload and enhanced connectivity
- Users can send data to edge nodes to perform processing and transmissions



Space Edge Computing for an orbital user using an Edge Node

What does SEC bring?

The architecture of future Space Edge Computing services will be highly distributed and complex.



Space Edge Computing as a Distributed Satellite System

Object and problematic

Current and future OBDH and data link technologies will play a role in future SEC services

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A Review on Inter-Satellite Links Free Space Optical Communication

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Feature Article:

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Towards the Use of Artificial Intelligence on the Edge in Space Systems: Challenges and Opportunities

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Architectures and Synchronization Techniques for Distributed Satellite Systems: A Survey

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GPU4S Bench: Design and Implementation of an Open GPU Benchmarking Suite for Space On-board Processing

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Our motivation is to define a tool enabling a fast modeling of complex SEC architectures to assess their technical requirements, strengths, weaknesses and feasibility

A hybrid data-centric approach

Macro Scale

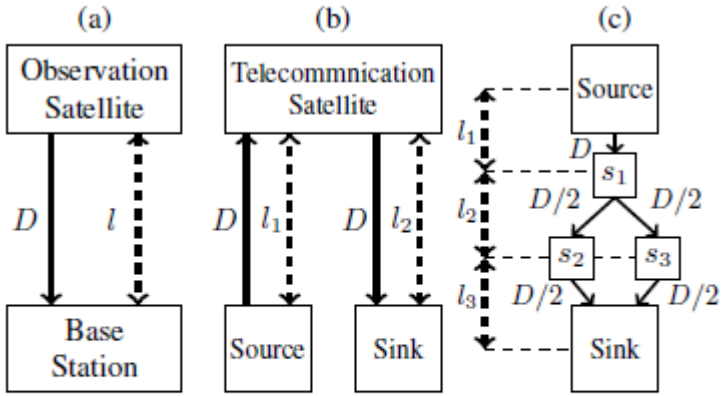


Fig. 1: Data flow and link lengths in typical satellite architectures: (a) standalone observation satellite, (b) bent-pipe telecommunication satellite between a source and a sink, (c) data flow in a DSS between a source and a sink

Micro Scale

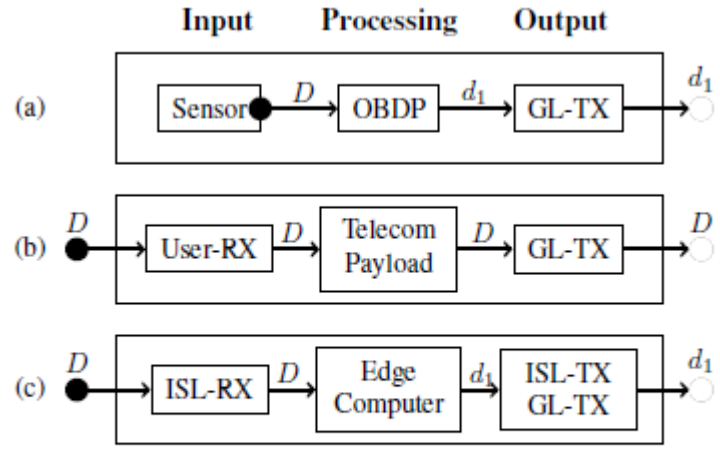


Fig. 2: Hardware Architecture of Typical Satellite: (a) observation satellite, (b) telecommunication satellite, (c) proposed architecture of an edge node

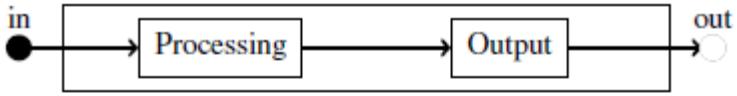


Fig. 3: Representation of a simple satellite as considered in the rest of this paper, without an input module. Input data reaches directly the processing module.

Hybrid Approach

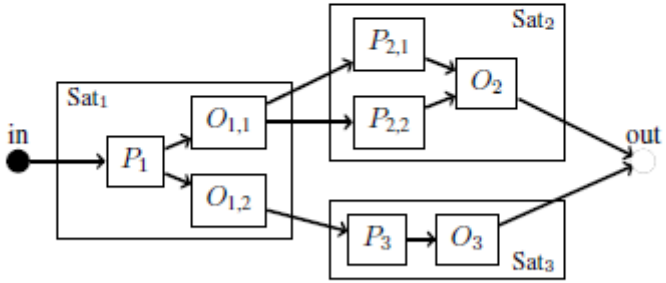


Fig. 4: Example of a DSS architecture represented with the hybrid model.

Formal graph modeling tool and definition of costs

Data processing modifies the size of the data packets flowing through the system.

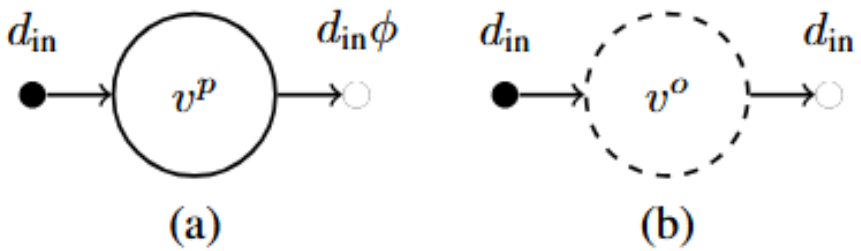


Fig. 5: Taxonomy of vertices: (a) a processing vertex altering the size of the data packets that pass through it (via a ϕ factor), (b) an output vertex that does not interfere with the size of data packets passing through it.

The path taken by a data packet through consecutive vertices from a source v_0 to a sink v_n is noted $\rho = (v_0, v_1, \ldots, v_n)$. Let ϕ_n be the ϕ coefficient associated to the n^{th} node of in the path,

$$\phi_n = \prod_{i=0}^{n} \phi_i \tag{1}$$

In a given path, with D the size of the data packet provided by the source v_0, the size of the data packet received by the vertex v_n can be expressed as :

$$d_n = D \cdot \phi_i \tag{2}$$

Formal graph modeling tool and definition of costs

Each type of vertex has its definition of costs calculated using the size of the data packets to handle and system specifications.

	Processing Costs	Output Costs
Time	$T(v^p) = \frac{d_{in}}{s}$	$T(v^o) = \frac{d_{in}}{s}$
Energy	$E(v^p) = e_{io} \cdot d_{in} + e_u \cdot T(v^p)$	$E(v^o) = e_o \cdot \log_{10}(l) \cdot T(v^o)$

Cost functions for processing and output nodes

Processing Vertex Specifications :

- ϕ : data packet size modification coefficient
- s : throughput (bit/s)
- e_io : energy efficiency for R/W (J/bit)
- e_u : energy consumption during uptime (W)

Output Vertex Specifications :

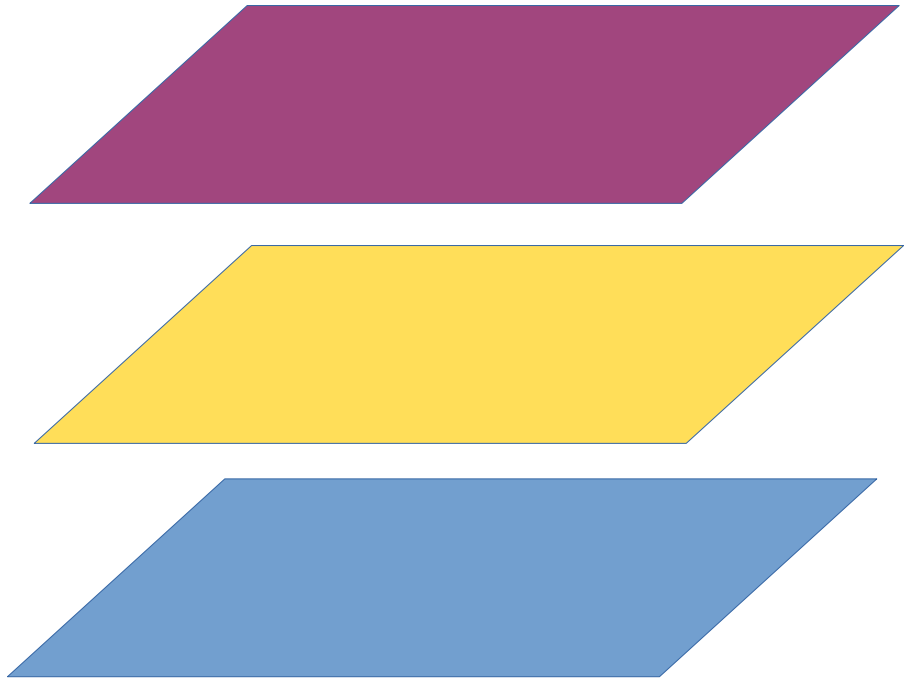
- s : data rate (bit/s)
- e_o : energy efficiency of the transmission (J/bit/km)
- l (little L) : link length (km)

The model stack

(2) Data packets

(1) System Specifications

(0) Vertices and interconnections



Case study

To demonstrate the use of the graph modeling tool, a case study is proposed.

The following problematics are addressed :

1 – Can the use of a SEC service provide lower costs than the typical standalone satellite architecture ?

2 – For a given user satellite, what are the minimal specifications for an edge node to provide improved costs ?

During this case study, two task offloading policies are investigated :

Partial offloading : the user satellite dispatches data processing tasks between itself and the edge node

Complete offloading : all data processing tasks are offloaded to the edge node (i.e no processing on the user satellite)

Cost Budget for a User Satellite

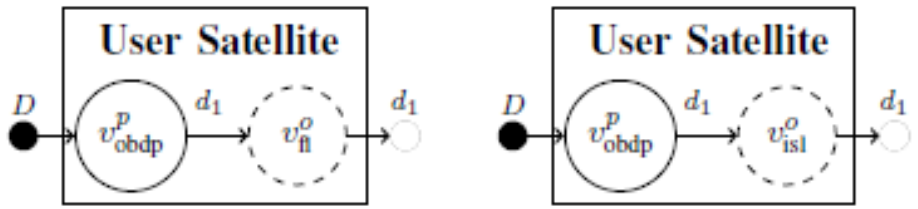


Fig. 6: User satellite architecture, (a) reference standalone architecture with a feeder link, (b) reference user satellite adapted for SEC with an ISL

Standalone Satellite						
OBDP				Feeder Link		
s	ϕ	e_{io}	e_{u}	s	l	e
30	0.9	0.001	1	10	800	5

TABLE I: System specifications for the reference standalone architecture

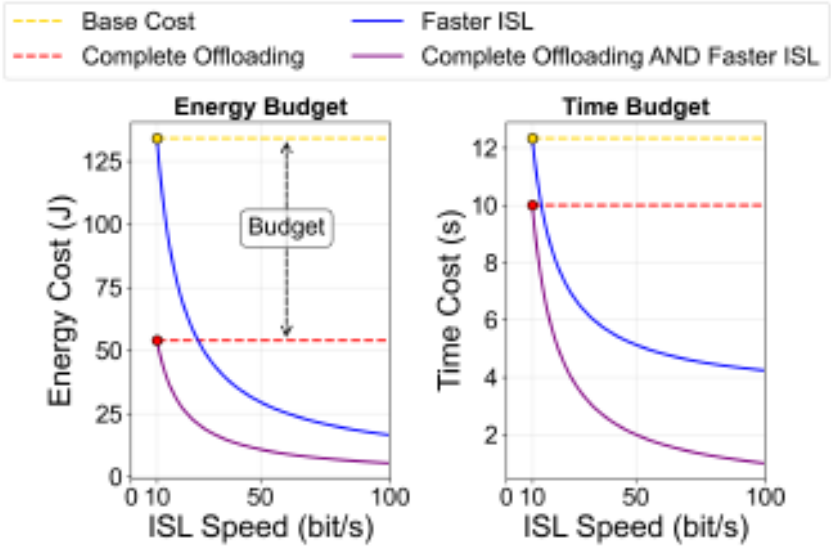


Fig. 8: Creating cost budget through the increase of the ISL's data rate and the use of a complete task offloading strategy

TABLE III: Time Cost Reduction (%)

ISL Speed (Mbit/s)	10	20	40	60	80	100
Partial Offloading	0.00	34.57	54.26	60.60	63.74	65.60
Complete Offloading	18.92	57.33	79.21	86.26	89.74	91.81

TABLE IV: Energy Cost Reduction (%)

ISL Speed (Mbit/s)	10	20	40	60	80	100
Partial Offloading	0.00	46.16	72.45	80.92	85.11	87.60
Complete Offloading	59.72	78.80	89.67	93.17	94.90	95.93

Specification Exploration for an Edge Node

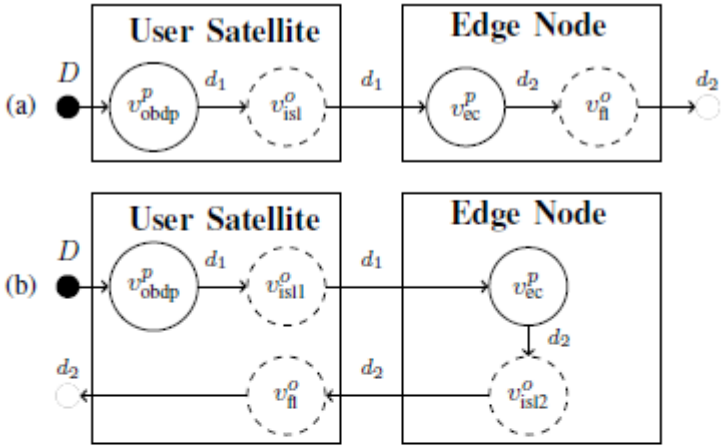
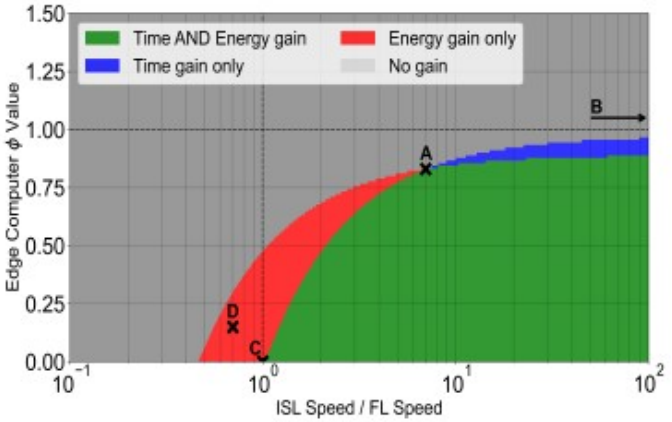


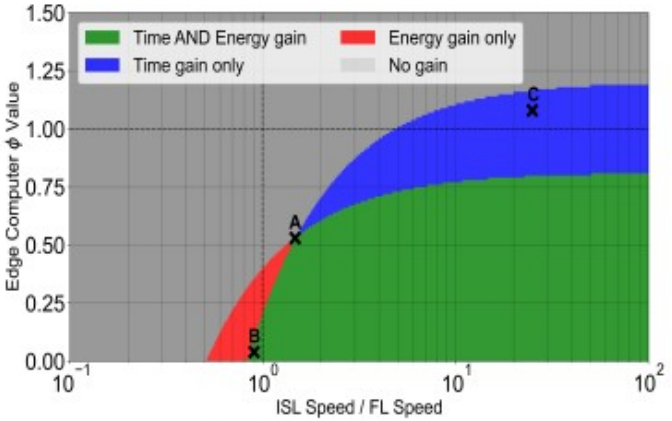
Fig. 7: Different scenarios: (a) standalone satellite, (b) edge node with ground link (c) edge node without ground link

User Satellite						
OBDP				ISL		
s	ϕ	e_{io}	e_u	s	l	e_o
30	0.9	0.001	1	?	100	3
Edge Node						
Edge Computer				Feeder Link		
s	ϕ	e_{io}	e_u	s	l	e_o
300	?	0.001	50	10	800	5

TABLE II: System specifications for the edge architectures

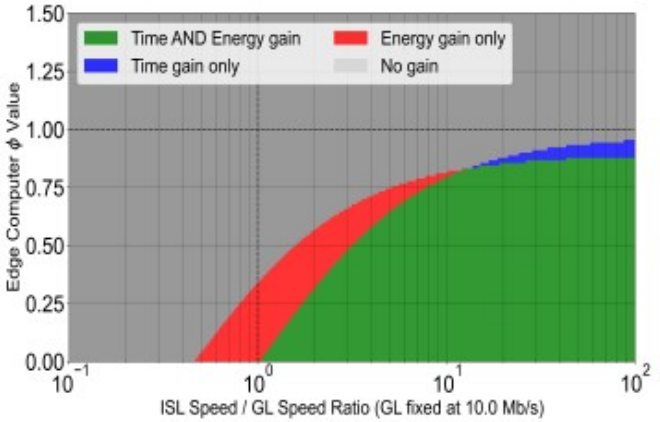


(a) Partial Offloading

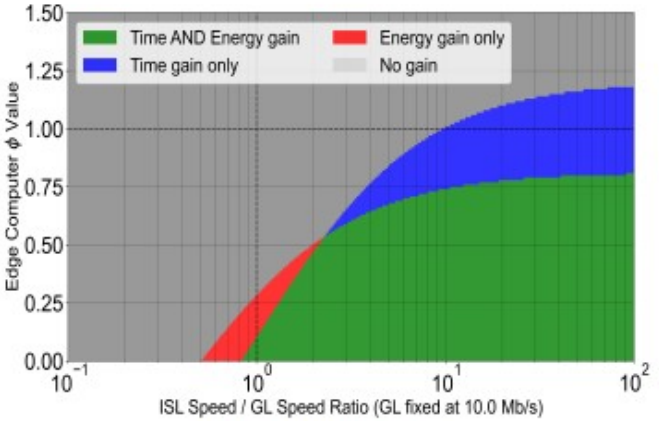


(b) Complete Offloading

Fig. 9: Specification exploration for an edge node with a FL



(a) Partial Offloading



(b) Complete Offloading

Fig. 10: Specification exploration for an edge node without a FL

Conclusion

The presented model

- Enables the representation of both macro and micro levels on the same scale without too much complexity
- Is scalable and can represent complex architectures easily for fast prototyping

Case study shows that according to the presented model:

- The use of a SEC service can present advantages in comparison with the traditional standalone architecture
- Different task offloading strategies are possible, complete task offloading can allow more flexibility
- The success of edge nodes heavily relies on the performance of ISLs

Weaknesses of this study

- Cost functions must remain heuristics → not as precise as a deep engineering study
- Fuzzy notion of “application”, no notion of networking and link availability

Future works

Future model Improvements

- Integrating input modules to the model
- Defining better energy cost heuristics based on ADC and DAC power consumption (+ link budget ?)
- Shifting the data processing costs from “throughput” (bit/s) to “OP/s”
- Clarifying the notions of “application” and “data processing”
- Integrating more costs to the model : memory usage, hardware usage, heat

Future works

- Developing a larger simulation tool that takes into account network routing and link availability
- Assessing costs related to the use of more elaborated task offloading policies

Thank you!

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