

## ADHA ON-BOARD COMPUTER MODULE (AOBCM)

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#### **SUMMARY**

- ADHA UNIT SYSTEM ARCHITECTURE
- FOCUS ON ADHA SYSTEM CONTROLLER
- TAS ADHA OBC MODULE (AOBCM)



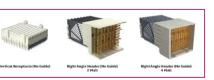
PROPRIETARY INFORMATION

#### ADVANCED DATA HANDLING ARCHITECTURE (ADHA) PROJECT

- The ADHA standardization is being developed in the frame of the (ADHA-2) project:
  - "ADHA Consolidation, Standardization, and Product Suite Development".
- ESA and Industry initiative to develop a modular, scalable and interoperable DH standard
- / Objective is to improve the cost and schedule figures of the DHS procurement, while improving its technical performances and budgets.
- I TAS & ADS primes of ESA double sourcing contracts, but most of European Space industry is involved (OHB, BG, DSI...)
- Based on evolution of cPCI-S-S standard backplane & mechanics (6U and 3U), press-fit connectors (e.g. AIRMAX VS)
- Demonstrators (ADHA-U1) at TRL-6 (EM) to be developed by primes (TAS, ADS) including Power + OBC + SSMM modules
- ADHA-U1 modules developed under ESA TDE ITT separate from ADHA-2
- I TAS is currently developing the ADHA OBC Module fo the ADHA-U





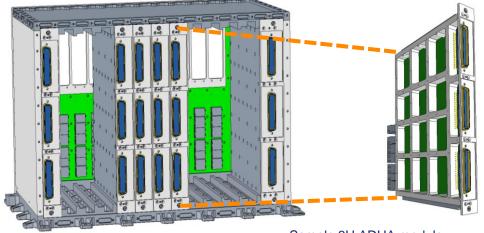


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#### **ADHA UNIT ARCHITECTURE (1/2)**

The ADHA architecture is based on the "Compact PCI Serial Space" (cPCI-S-S) standard, tailored to comply with System Requirements. The most relevant features of the ADHA unit architecture are the following:



Sample 6U ADHA module (6U extended - 220mm length)

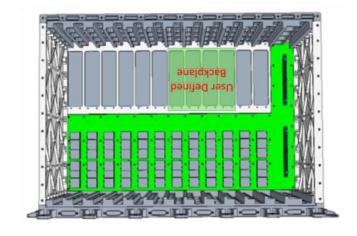
- Racked mechanics, to ease the (de)assembly;
- Boards format extended 6U (length 220 mm) or 3U;
- Boards pitch extended from 5HP to 6HP (for mounting the DSUB-78 pin connectors);
- I Fully redundant and cross-strapped system architecture (twin system slots and redundant links on the backplane);
- Standardized power module on dedicated slot;
- Wide range of links on the backplane.



#### **ADHA UNIT ARCHITECTURE (2/2)**

- Split Backplane and User Defined Backplanes:
  - Some redundant modules (e.g. the main and redundant boards of the OBC) are connected by a high number of cross-strapping connections;
  - These are much dependent from the specific design of the supplier and are not appropriate to include in the standard backplane;
  - Free space on the higher part of the unit can host one or more User Defined Backplanes;
- User Defined Backplane is only for specific links between different boards of the same modules; it is not allowed between different kind of modules to prevent the interoperability of the modules.
- It is possible to implement additional External Connectors in the rear side of the unit through the User Defined Backplane.

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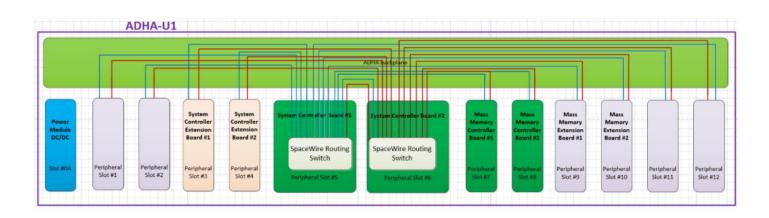




## **ADHA BACKPLANE DESCRIPTION (1/2)**

#### Power and Command & Control links:

- Power module on dedicated Slot 0 providing internal redundant secondary voltages: +28V, +12V and +5V;
- Modules' on/off/reset managed by dedicated links (PSON, Reset) connecting any of the two modules in System Slots (5-6) with any other module;
- Sync-Signals on dedicated lines for precise modules' time synchronization:
- Internal **C&C** of the unit is based on redundant **CAN** Bus and point-to-point **SpW** links connecting any of the two modules in System Slots (5-6) with any other module (double star topology);





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## **ADHA BACKPLANE DESCRIPTION (2/2)**

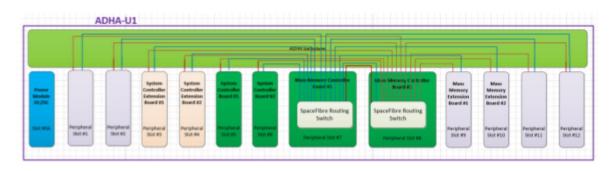
#### High Speed Data Processing Chain:

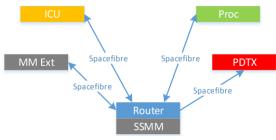
- Based on SpFi double star centered on Slots 7-8 (or alternatively 5-6);
- Net data rate for the SpFi links is 10 Gbps (over two lanes, in advance to 8B/10B encoding);
- Central hub continuous throughput 40 Gbps data rate;
- Data rate to PDTX may reach 20 Gbps if directly connected to the central hub through optical transceiver
- Support different processing paradigms:

Real time pre-processing:
ICU -> Proc -> MM Ext -> PDTX

Off-line processing:
ICU -> MM Ext -> Proc -> MM Ext -> PDTX

Real time post-processing:
ICU -> MM Ext -> Proc -> PDTX







#### **ADHA UNIT 1 (6U-ADHA-U1)**

The main objective of the ADHA program is to demonstrate the ADHA concepts and finally performances and functionality of two 6U ADHA Engineering Model units (called **6U-ADHA-U1**), which includes different type of modules:

- A Power Module
- / An On-Board Computer (OBC) Module,
- A Solid State Mass Memory (SSMM) module,
- Additional peripheral modules

integrated within an ADHA rack.

The OBC module is able to interface the ADHA standard backplane and to act as **system controller** to **configure, control and manage the entire unit**. For these purposes it implements:

- SpaceWire router acting as the center of the SpaceWire star networks in the ADHA unit
- I The control functions on the backplane, i.e. PS\_ON, RST, Health Management System (HMS), distribution of timing and synchronisation signals (SYNC), and bus master on the CAN busses.



## ADHA OBC MODULE (AOBCM) REQUIREMENTS

- **System level requirements**: ADHA is conceived to support a wide range of missions, environments and unit types, however the first targeted use case is related to LEO Earth observation missions. Hence the applicable System Requirements come from the Copernicus HPCM Missions:
  - HPCM Missions System Requirements Documents (SRD);
  - HPCM Operations Interface Requirements Document (OIRD);
- **AOBCM Requirements Specification:** Starting points have been:
- SAVOIR OBC Specification;
- OBC Requirements Specifications prepared by the two consortia in ADHA-1 contract, in line with:
  - → applicable system level requirements
  - → companies' heritage

The AOBCM specification is the outcome of extensive coengineering activity of all the Agency and Industry partners (ESA, TAS, ADS, BG);

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The final specification has been agreed by all partners after extensive review activity.



#### ADHA OBC MODULE (AOBCM) FACT SHEET

- AOBCM functionality and architecture in line with Savoir requirements;
- AOBCM design is evolutive with respect to well established TAS product IPAC/SMU-NG used in various HPCM missions (ROSEL, CIMR, CHIME), on G2SB1, etc...
- OBC processing capability of at least 1000 DMIPS / 30 MFLOPS;
- Compatible with X-band TT&C performance (TC at least 2 Mbps, TM at least 30 Mbps);
- The switch from S to X-band for TT&C supports reduction of Ground station
- Security based on CCSDS SDLS Protocol and Extended Procedures (TC authentication);
- File Based Operation based on Class-1 and Class-2 CFDP;

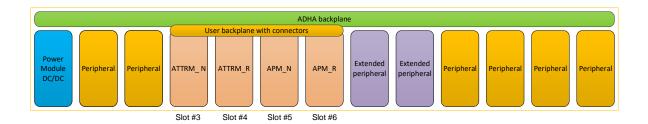


## **AOBCM DESIGN CHALLENGES (1/2)**

TASI is in charge to implement the AOBC module for the ADHA U1 unit.

Considering the high performance required, the functions need to be implemented on three 6U (233.35x220mm) boards:

- ADHA Processor Module (APM) boards (N+R) hosted in slots number 5 and 6
- ADHA TC, TM, Reconfiguration and Platform Mass Memory (ATTRM) boards (N+R), hosted in slots number 3 and 4



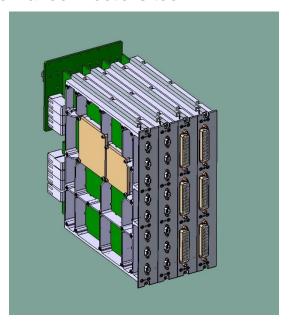
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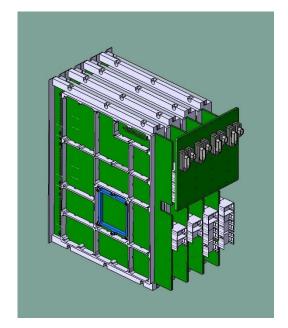
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#### **AOBCM DESIGN CHALLENGES (2/2)**

- The AOBCM boards needs to be interconnected by an high number of custom links (matched pair management between RMs, CLCW I/F, PPS from GNSS to OBRT, interrupts, X-straps, ...)
- I These links have been implemented through a properly designed **User Defined Backplane**, which host **external connectors** too







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#### ADHA OBC MODULE (AOBCM) EXTERNAL INTERFACES

Each OBCM redundancy provides following external I/F:

- 8 SpW links
- 1 1 connector (78 pin) providing TC input, TM output and PPS input I/F
- 1 1 connector (78 pin) providing external HPTM input and SYNC/ PSS output I/F
- 1 1 connector (78 pin) providing HPC (HL or LL) output I/F and ALARM input I/F
- / 2 CAN BUS I/F on the rear user backplane side
- / 1 MIL-STD-1553B (redundant) on the rear user backplane side
- 1 Test connector on the user backplane side to the APM for maintenance/test purpose
- 1 Test connector on the user backplane side to the ATTRM providing Configuration Upload Manager I/F and Key Injection Manager I/F)
- 1 1 Security module



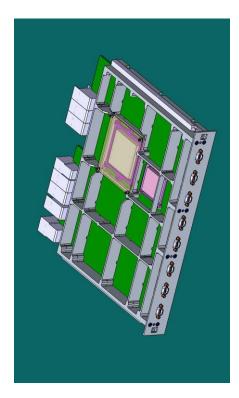
# ADHA OBC MODULE (AOBCM) INTERNAL STANDARD BACKPLANE INTERFACES

Each OBCM redundancy provides following internal I/F to the ADHA boards toward the standard backplane:

- **10 SpW links** (8 links to the peripheral slots 1,2,7,8,9,10,11,12 + 2 links between the system slots 5 and 6)
- Sync\_ 1 and Sync\_2 signals (bussed to all the peripheral slots)
- 8 PSON\_A + 8 PSON\_B signals (to switch ON/OFF peripheral on power A or power B)
- **10 RESET signals** (2 signals to each slots 1 and 2 which support 2FCG, 6 signals to slot 7,8,9,10,11,12)
- / HMS signals (2 address lines + 16 analogue acquisition lines including OBCM self monitoring)
- 2 CAN BUS



## **ADHA PROCESSOR MODULE BOARD (1/2)**



The **APM** is based on the **GR740** quad-core processor System-on-Chip and the "*Companion*" reprogrammable Microchip Rad-Tolerant High Rel RTG4 FPGA, memories, transceivers/drivers/buffers related to various external interfaces and local power distribution devices.

#### The FPGA *Companion* is intended to:

support the GR740 in the control of board internal devices

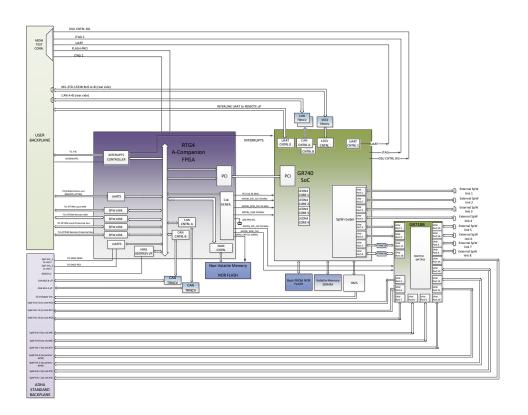
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provide additional interfaces

A section of the *Companion* FPGA implements the functionality of microprocessor interface, conditioning of input signals, calculation of input power level and noise floor level for each input samples pairs.



## **ADHA PROCESSOR MODULE BOARD (2/2)**



Due to the huge number of SpaceWire links to be managed in the ADHA system and being the links provided by GR740 SoC not enough (8 ports), one additional external FrontGrade Gaisler qualified 18-ports GR718 SpW router is added to expand the number of SpW links to provide the necessary links on the ADHA backplane.



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#### **ADHA TTRM BOARD – MAIN FUNCTIONALITY (1/3)**

The **ATTRM** board hosts the "Streamer" FPGA, based on reprogrammable space qualified RTG-4 which includes several functions:

- Telecommand function devoted to receive, decode and execute Ground Telecommands.
- I TM encoder and frame generation
- Internal and external HPTM data acquisitions
- Internal and external alarms surveillance and FDIR reconfiguration management (reconfiguration sequences execution)
- On Board Time Management
- Synchronization signals generation and synchronization with GNSS PPS
- PSON, Reset and SYNC signals management
- uplink and downlink of files according to CCSDS File Delivery Protocol (CFDP)



#### **ADHA TTRM BOARD – MAIN FUNCTIONALITY (2/3)**

The **ATTRM** is a **vital module**: since it implements the **Essential Telecommands** (processed without SW-interaction) and the **Reconfiguration Module.** 

These essential telecommands are either AOBC internal handled or dedicated to switch the power status of a module within the unit (done via PSON signals) or to release a high-powercommand sent to another external unit.

Since a vital module cannot interrupt its functioning under any condition, the entire ADHA-U1 is considered a "Vital Unit" powered through R-LCL that cannot be switched off.

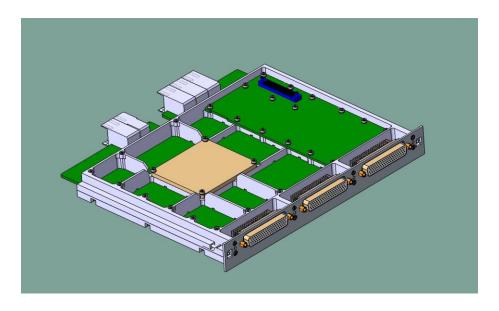


#### **ADHA TTRM BOARD – SECURITY FUNCTIONS (3/3)**

A **Security Extension Mezzanine**, plugged on the ATTRM mainboard, provides the security function:

- TC Authentication
- OTAR TC Decryption
- Deciphering Key management in NVM

The choice to house the security function on a mezzanine allow either to enhance the function itself guaranteeing the compliance to more demanding standards, or not to include this function (with cost saving) when encryption/decryption are not required.





#### CONCLUSION

- I The design activity performed in the frame of the AOBCM confirms the adequacy of the ADHA standard to support demanding Spacecraft Data Handling applications;
- In particular, it is being implemented on ADHA boards an OBC module fully in line with Copernicus Expansion/Extension missions requirements and Savoir architecture;

#### / Highlights:

- Increasing the boards pitch to 6HP has made possible usage of the 78 pin D-sub high density connector providing huge improvement in external lines budget (critical parameter for highly integrated and miniaturized Data Handling units);
- Adoption of "User Defined Backplane" has furtherly improved the external lines budget and segregated all custom connection between OBC boards outside of the standard backplane;
- It has been possible to implement all the OBC redundancy and cross-strappings;
- All requirements related to OBC vital functions are implemented
- All C&C connections between OBC and other modules implemented through the backplane.

