

ADHA On-board Computer Module (OBCM)

Kostas Marinis *, David Steenari *

Dario Pascucci †, Paolo Ciparelli †, Gianluca Aranci †

* European Space Agency (ESA), Noordwijk, Netherlands

† Thales Alenia Space (TAS), Italy

Abstract— The ADHA (Advanced Data Handling Architecture) program is an initiative of the European Space Agency (ESA) in collaboration with European industrial partners, for the development of a standardized, modular and scalable platform for data handling and data processing systems, based on interoperable and interchangeable electronic modules. In the frame of ADHA Consolidation, Standardization and Product Suite Development activity, which covers the development of the first Engineering Model (TRL=6) unit (composed of 3 types of modules, a rack and a backplane) TASI has been selected to be the On-Board Computer module provider. This paper presents the ADHA OBC solution based on the TAS-in-Italy state-of-the-art Platform Computer IPAC (Integrated Processing, data-handling and AOCS Controller) Hi-rel product based on the European quad-core Leon4 System-on-Chip GR740.

Keywords— Advanced Data Handling Architecture, ADHA, OBC, On-board Computers, IPAC, GR740

1. INTRODUCTION

The main objective of the ADHA program is to demonstrate the ADHA industrial concept, the technical concept with the interchangeability and inter-operability of the strategic ADHA modules, and finally performances and functionality of two 6U ADHA Engineering Model units (called 6U-ADHA-U1), which includes three modules: a Power Module, and On-Board Computer (OBC) Module, and a Solid State Mass Memory (SSMM) module, integrated within an ADHA rack.

The OBC module is intended to implement the commanding and control functions for all spacecraft units, communication to and from ground, acquisition, storage and processing of platform data. In addition, it also acts as system controller, commanding and controlling the modules within the same ADHA unit in a fully redundant configuration.

The OBC solution is based on the Core section of IPAC (Integrated Processing Avionics Controller) Hi-rel state-of-the-art TAS product, which has been already selected as Platform Computer, named “SMU-NG”, for the ESA Copernicus ROSE-L / CHIME / CIMR Expansion Missions.

IPAC Hi-Rel version, is fully developed and qualified funded by Italian programmes (TRL-7): the choice of the IPAC concept high performance computer, is an important asset for the future programs development of ADHA, in fact allowing to maintain all the cumulated experiences, tools, FirmWare,

SoftWare, procedures and knowledge and minimize the cost and risks for the ADHA development.

Following chapters focus on the ADHA On-Board Computer Module architecture and main features related to the ADHA OBC specifications and needs.

2. ADHA OBCM ARCHITECTURE

The ADHA OBC module functions are implemented in two boards: the ADHA Processor Module (APM), and the ADHA Telecommand/Telemetry, Reconfiguration and Platform Mass Memory (ATTRM) with its security mezzanine (ASEC). Furthermore an ADHA User backplane is provided to host additional external connectors and to implement the necessary boards signals exchange.

The APM NOM and RED are intended to be hosted in the system slot #5 and #6 of the 6U-ADHA unit while ATTRM on the peripheral slot #3 and #4, as reported below:

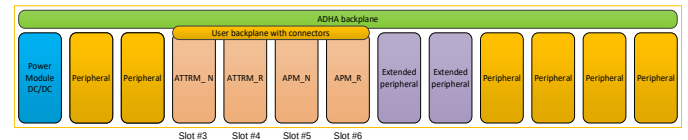


Figure 1: 6U ADHA unit, OBC configuration

The OBCM is able to interface the ADHA standard backplane and to act as **system controller** to configure, control and manage the entire unit. For these purposes it implements:

- The SpaceWire router for the ADHA backplane, effectively acting as the center of the SpaceWire star networks in the ADHA unit.
- The control functions on the backplane, i.e. PS_ON, RST, Health Management System (HMS), distribution of timing and synchronisation signals (SYNC), and bus master on the CAN busses.

The detailed electrical specifications for these signals and interfaces are given in [13], and [14].

Following external interfaces are provided for each of the two branches (nominal and redundant):

- 2 CAN BUS I/F on the rear user backplane side
- 8 SpW links
- 1 MIL-STD-1553B on the rear user backplane side
- 1 Test connector on the user backplane side to the APM (maintenance/test)

- 1 Test connector on the user backplane side to the ATTRM (providing Configuration Upload Manager I/F and Key Injection Manager I/F)
- 1 connector providing TC&TM I/F + 3 PPS IN I/F
- 1 connector providing 16 essential TM input + 6 RM alarm input + 5 PPS OUT + 3 SYNC OUT
- 1 connector providing 16 HPC I/F

In figure below a preliminary mechanical design of the ADHA OBC module (N+R) and its user backplane is depicted:

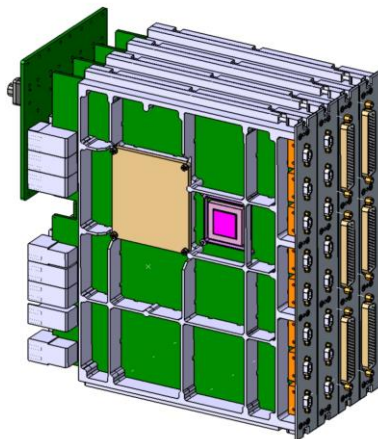
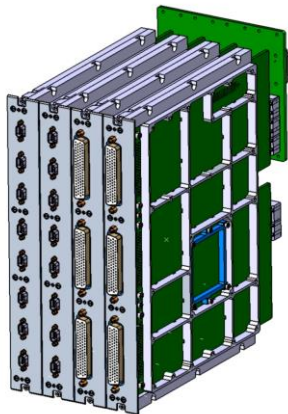
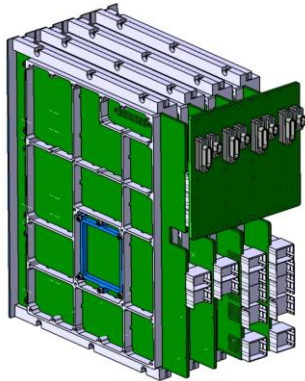


Figure 2: ADHA OBC modules

The APM implements connectors P1, P2, P3, P4 as per ADHA module profile B specifications: (see pictures below):

	Profile (B)	Profile (C)	Profile (D)
P6	Optional: Star Point of SpaceFibre	Optional: Star Point of SpaceFibre	Unused: General Purpose
P5	Unused: General Purpose	Unused: General Purpose	Unused: General Purpose
P4	Optional: SpaceWire / SpaceFibre	Optional: SpaceWire / SpaceFibre	Optional: SpaceWire / SpaceFibre
P3	Optional: Star Point of SpaceWire	Optional: Star Point of SpaceWire	Unused: General Purpose
P2	Source for Control Signal Pins (PSDM, RST, Monitoring)	Unused: General Purpose	Unused: General Purpose
P1	Control Signal Pins	Control Signal Pins	Control Signal Pins
	Power Pins (12V, 5V, 28V)	Power Pins (12V, 5V, 28V)	Power Pins (12V, 5V, 28V)
P0	Optional, unused → removed		

Figure 3: ADHA Slot profiles

The ATTRM board implements P1 only (as per profile D specifications). Refer to [21] for slot profile details.

3. ADHA PM BOARD

The APM is based on the GR740 quad-core processor System-on-Chip and the “Companion” reprogrammable Microchip space qualified RTG4 FPGA, memories, transceivers/drivers/buffers related to various external interfaces and local power distribution devices. The FPGA Companion is intended to:

- support the GR740 in the control of board internal devices
- provide additional interfaces missing in the GR740 SoC
- Implement additional SpW and UART

In order to exploit as much as possible the features offered by the GR740 all functions required by the platform avionics (e.g. MIL-STD-1553B Bus controllers, SpaceWire router links, CAN Bus controllers) are allocated to GR740, while additional functions as internal PCI bus, SpW link, UART, are allocated to the Companion FPGA.

Due to the huge number of SpaceWire links to be managed in the ADHA system and being the links provided by GR740 SoC not enough (8 ports), one additional external FrontGrade Gaisler qualified 18-ports GR718 SpW router is added to expand the number of SpW links and to provide the necessary links on the ADHA backplane: each of the two APM boards provides one SpW link, running up to 200Mbps, towards the peripheral and extended peripheral slots and one link towards the partner APM board.

The GR740 following features are directly accessible by the SW (regardless which processor core is requesting):

- External CAN BUS (A + B links) located on the user backplane
- External MIL-STD-1553B Bus (A + B links) located on the user backplane
- 8 SpaceWire Links (4 pertinent to SpW Router embedded in GR740 and 4 pertinent to the GR718 external router)
- 4 SpaceWire Links to interconnect the external and internal router located on the user backplane.
- 10 SpaceWire Links toward the ADHA standard backplane
- 1 UART that connects (via Core Module backplane) nom. and red. GR740 for SW cross-maintenance purposes (UART 0) on the user backplane
- 1 UART (UART 1) function, routed to local test connector (located on the user backplane) for testing and SW development purposes.

HMS

The health monitoring system implemented in the APM is able to acquire, from each ADHA module, 4 analogue parameters (4+4 parameters for 2FCG module in slot from 1 to 4):

- 1) the current of main power line (+12V);
- 2) a module voltage
- 3) two temperature

The acquiring system hosted in the APM uses address lines Add(0:1) to select (cyclically) the monitored parameters, and two AD128 managed by the SPI I/F to convert the 16 analogue inputs (including its own monitors) into digital. Each APM and ATTRM boards are equipped with an acquisition system (the same used on all the other unit's board) to provide the 4 analogue parameters to the system slot A and system slot B (4+4 lines).

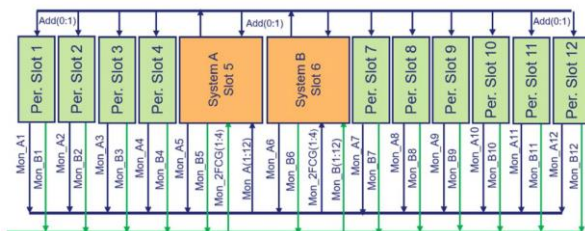


Figure 4: Functional block diagram of the HMS

4. ADHA TTRM BOARD

The ATTRM board integrates, in a single PCB, several functions:

- Ground TC Acquisition and Decoding (TC Decoder compliant with CCSDS protocol) - The decoder is able to receive CLTU packet NOM and RED Transponder
- CPDU unit and HPC generation
- TC MAP routing
- TM Encoder compliant with CCSDS protocol applying several encoding option. The encoder manages up to 8 TM Virtual Channels.
- TM frame generation and VC management
- Internal and external HPTM data collection and TM frame generation
- Real Time TM frame generation

- Downlink of TM frames, previously stored as CCSDS packet into the Local and Partner Platform Mass Memory
- Direct downlink of two external CCSDS TM packet sources
- Cross coupling of TM output streams
- Internal and external alarms surveillance and FDIR reconfiguration management (reconfiguration sequences execution)
- Management of Volatile and Non Volatile SGM
- On Board Time Management
- Synchronization signals generation and synchronization with GNSS PPS
- Interface the partner ATTRM board and two nominal and redundant APM boards
- PSN, Reset and SYNC signals management
- uplink and downlink of files according to CCSDS File Delivery Protocol (CFDP)

A Security Extension Mezzanine, plugged on the ATTRM mainboard, provides the security function:

- TC/TM Authentication
- TC Decryption
- TM Encryption
- Deciphering Key management in NVM

The choice to house the security function on a mezzanine allow either to enhance the function itself guaranteeing the compliance to more demanding standards, or not to include this function (with cost saving) when external encryption/decryption are foreseen.

The ATTRM board hosts the "Streamer" FPGA, based on reprogrammable space qualified RTG-4 which includes the packet Telecommand function devoted to receive, decode and execute (for some type of TC) Ground Telecommands.

The ATTRM (vital module) receives from ground essential telecommands which shall be processed without SW-interaction. These essential telecommands are either AOBC internal handled (e.g. a switch of the OBC-master) or to switch the power status of a module within the same unit, done via PSN signals or to release a high-power-command sent to another unit.

Vital modules needs to be switched-on automatically on as soon as the unit is powered and cannot be switched off , to allow the command and control of the vital function. A set of jumpers are provided on the ADHA backplane to let to configure properly the PSN signals for vital or non-vital modules hosted on slots 3,4,5 and 6 as depicted below:

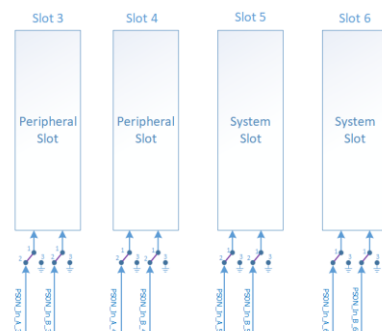


Figure 5: ADHA backplane jumper configuration

The configuration let to implements following cases:

- Modules supplied from rail A (case vital)
- Modules supplied from rail B (case vital)
- Modules switched ON/OFF on power rail A or B

5. POWER DISTRIBUTION

The ADHA boards receive +12 V main power from the backplane connector P1. The OBCM power supply section is implemented basing on the ISL70003ASEH switching regulators to generate all the needed secondary voltages. Special attention was paid to take into account the failure propagation requirements. For this purpose the secondary voltages are not directly converted from the +12V: an intermediate level of conversion with a ISL70001 regulator is provided. Same approach has been used to avoid failure propagation on the +3.3 V power line.

6. USER BACKPLANE

The user backplane allows the specific interconnection among the two APM and the two ATTRM boards. Boards connection on the user backplane are implemented by cPCI connectors Type B.

7. CONCLUSION

The development activities of the ADHA OBCM are ongoing. The Engineering Model, Form Fit and Function representative of Flight Model, is expected to be completed within Q3-25.

The AOBC project provided the context to prove “on the field” the ADHA architecture aspects, facing the challenges implicit in the real implementation; first of all, to accommodate and fit the whole hardware of a complex equipment, like the Spacecraft On-Board Computer, within the ADHA architecture constraints. This has also permitted to refine several aspects of the ADHA standard.

The experience gained during the OBCM design and development has been fruitful and it is fundamental for the consolidation of the ADHA architectural concept.

REFERENCES

- [1] ADHA Document [RD26], Why is ADHA important to Earth Observation?, J. Rosello, ADHA-2 Workshop 2022, Presentation at ADHA 2022 Workshop, 22-23 Nov 2022 ESTEC
- [2] Advanced Data Handling Architecture (ADHA): Status, Current Activities and Industrial Road Map, Olivier Mourra et al, European space Data Handling and Processing Conference - EDHPC 2023, 2-6 Oct 2023, Juan les Pins (FR)
- [3] ADHA Document [RD27], ADHA Objectives, O. Mourra, ADHA-2 Workshop 2022, Presentation at ADHA 2022 Workshop, 22-23 Nov 2022 ESTEC
- [4] ADHA, an Agile Platform Enhancing New Satellite On-Board Data Processing Systems , Olivier Mourra et al, European space Data Handling and Processing Conference - EDHPC 2023, 2-6 Oct 2023, Juan les Pins (FR)
- [5] Copernicus Sentinel Expansion missions, [https://www.esa.int/Applications/Observing the Earth/Copernicus/Copernicus Sentinel Expansion missions](https://www.esa.int/Applications/Observing_the_Earth/Copernicus/Copernicus_Sentinel_Expansion_missions)
- [6] SAVOIR Generic OBC Specification, SAVOIR-GS-001, <https://essr.esa.int/>
- [7] CCSDS Space Data Link Security (SDLS) protocol, CCSDS 355.0-B-2, ccsds.org
- [8] CCSDS Space Data Link Security – Extended Procedures (SDLS-EP) protocol, CCSDS 355.1-B-1, ccsds.org
- [9] ECSS Telemetry and Telecommand Packet Utilization Standard (PUS), ECSS-E-ST-70-41C, ecss.nl
- [10] CCSDS TM Space Data Link Protocol, CCSDS 132.0-B-3, ccsds.org
- [11] CCSDS TM Synchronisation and Channel Coding, CCSDS 131.0-B-4, ccsds.org
- [12] CCSDS File Delivery Protocol (CFDP), CCSDS 727.0-B-5, ccsds.org
- [13] ADHA Document [AD018], ADHA Backplane Electrical Interface Control Document (ADHA-Ux-E-ICD)
- [14] ADHA Document [AD026], ADHA OBC Module Requirement Specification (A-Ux-OBC-M Specification)
- [15] ADHA Document [AD006], ADHA Module Design Interface Requirements (MDIR)
- [16] ADHA Document [AD019], ADHA SpaceWire Specification
- [17] ADHA Document [AD021], ADHA CAN Bus Specification
- [18] ADHA Document [AD014], Generic Design Description for ADHA
- [19] ADHA Document [AD073], Design Description of the Health Monitoring System (HMS) used in ADHA-Ux units
- [20] ADHA Document [AD030], ADHA OBC Low Level Software Specification (A-U1-OBC-M1-SW Specification)
- [21] ADHA Document [AD017], Generic requirements for ADHA modules
- [22] ECSS-E-ST-40C - Software, ecss.nl
- [23] ECSS-E-ST-80C Rev.1 – Software Product Assurance, ecss.nl
- [24] cPCI Serial Space Specification, PICMG CPCI-S.1 R1.0,
- [25] CCSDS TC Synchronisation and Channel Coding, CCSDS 231.0-B-4, ccsds.org
- [26] CCSDS TC Space Data Link Protocol, CCSDS 232.0-B-4, , ccsds.org
- [27] ADHA Document [AD002], ADHA documentation List, reference ESATECEDD-DD-2022-000057
- [28] Advanced Data Handling Architecture (ADHA): On-board Computer (OBC) Module – Olivier Mourra et al, European space Data Handling and Processing Conference - EDHPC 2023, 2-6 Oct 2023, Juan les Pins (FR)
- [29] ADHA On-board Computer Module (OBCM), K. De Mattia, K. Marinis, D. Pascucci, Abstract for DASIA - 30 May 2024