EDHPC 2025 - 2nd European Data Handling & Data Processing Conference

Monday 13 October 2025 - Friday 17 October 2025

Topics

Satellite End-to-end data handling and processing architectures

On-Board data processing architectures

On-board data handling architectures

ADHA - Advanced Data Handling Architecture

Reconfigurable Data System Architectures

Distributed processing architectures

Distributed computing of data and signal processing

Signal processing chain architectures

Lessons learnt

Avionics and data handling systems for platform, launchers, optical & RF payloads

On-Board Computer (OBC) units, Remote Terminal Units (RTU), Mass Memory units, Instrument Control units (ICU)

High Performance Hardware Data and Signal Processing unit/module,

o High throughput electronics for Radar back-ends, Radiometer back-ends, Instrument Front End Electronics
o High throughput electronics for transparent and regenerative processors for Satellite Communication, Intersatellite and TT&C units

Software Defined Radios

Use of digital and mixed-signal components in OBC / OBDP and in data/signal processing systems (Reference Designs)

Multicore processors, GPUs, FPGAs, DSPs, memories, full custom processor ICs,SoC, SiP, DAC, ADC

Use of COTS in OBC / OBDP and signal processing systems

Selection, radiation test results, mitigation technics in designs

Validation & verification, testing, qualification, simulation, modelling of complex systems

Lower-class mission, smallsat and cubesat data handling equipment

Processor simulators/emulators

Software development platforms/toolchains for the new generation of processors (including FPGAs) - compilers, debuggers, etc.

Qualification of low-level software libraries (e.g. OpenMP)

Buses, networks & protocols

Protocol developments of SpaceWire, SpaceFibre, CAN-Bus, Ethernet, other protocols

Software building blocks for higher level protocols

Validation & verification

Simulation suites, Test equipment, approaches, and standards

Components

Embedded interfaces in processors/FPGAs, Switches, routers, SerDes, (optical) transceiver, connectors, harness

Wireless Technologies

OBDP (On-Board Data and Signal Processing)

Device Benchmarks (Multicore processors, GPUs, FPGAs)

Developments in On-Board Data Processing Frameworks, Architectures and Building Blocks

Parallel processing frameworks (OpenMP, OpenCL), Hardware acceleration of processing tasks, Heterogeneous processing systems, FPGA IP and HLS

On-board Data Processing Algorithms and Implementations

On-board processing applications for Multi- and Hyperspectral image processing, Visual navigation, Data reduction

On-board Signal Processing Algorithms for RF applications such as SDR, 5G/6G gNb, AIS, ADS-B, Beamforming, Modems, PNT, Positioning, Synthetic aperture radar (SAR) processing, Radio interferometer processing

Implementations of On-board Signal Processing Algorithms for RF applications (DSP SW, FPGA IP and HLS, etc)

AI and Machine learning for on-board data processing

Data Analysis (classification, segmentation, selection), datasets for training of on-board AI, Efficient Neural Networks, Software tools and FPGA IP for machine learning inference, Fault-tolerance in deep learning algorithms, applications for RF Payloads and Instruments, like signal intelligence, anomaly detection, spectrum allocation, cognitive radar, network orchestration

Validation & verification of hardware and software implementation of On-Board Data & Signal Processing algorithms and functions.