Final Presentation

AAML STUDY

AVIONICS ARCHITECTURE MODELLING LANGUAGE

2014, May 22th

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INTRODUCTION AND OBJECTIVES

GMV INNOVATING SOLUTIONS

INTRODUCTION

- The ESA **AAML (Avionics Architecture Modelling Language)** study aims at advancing the avionics engineering practices towards a model-based approach.
- Consortium led by GMV:

  - **GMV's tasks**: specification of the analyses (algorithms), identification of specialized modelling entities, implementation of the modelling language, graphical editor, modelling environment, analysis tools and use case.
  - **Thales's tasks:** selection of use cases, identification of relevant analyses (input, outputs and tasks in each development phase), identification of modelling entities and design views.
- Project Kick-Off Meeting on February 2013.
- Project Acceptance Review on April 2014.

SCOPE AND BACKGROUND (1 / 2)

- Defining an avionic architecture for a given project means making several key architecture choices and sizing several performance parameters.
- The selection is usually based on:
  - The architect's expertise and background.
  - Avionics-specific analyses (to perform trade-offs).

Traditional process:

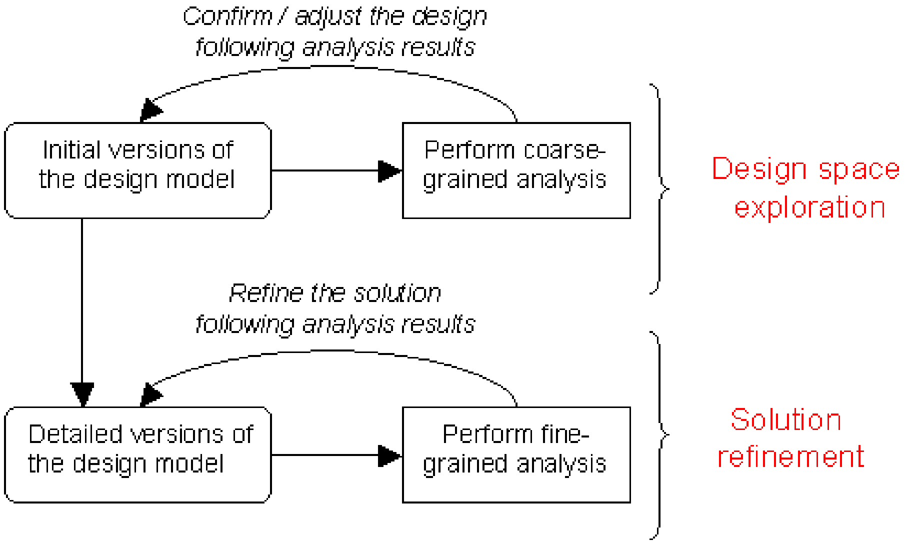
- Each type of analysis is based on a dedicated model (sometimes ad-hoc to solve a particular problem).
- Some training is required to be used effectively.

AAML model-based approach:

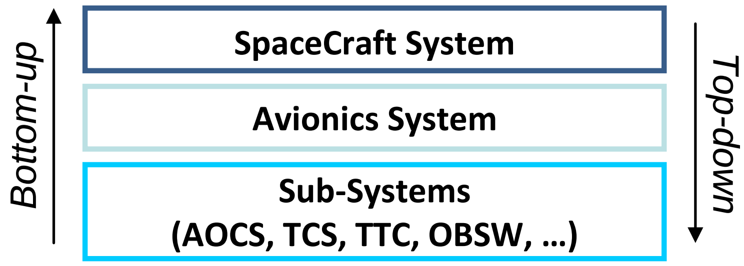
- Usage of a single architectural model.
- The same input (i.e., single source model) is used to perform different avionics analyses.
- The analyses cover most of the phases of the life-cycle.

SCOPE AND BACKGROUND (2 / 2)

- **Advantages**:
  - Improves the consistency.
  - It allows architects to trace their decisions during the model refinement iterations.
  - Facilitates the reuse (e.g., instantiation off-the-shelf components).



- Contribution to the objectives of the **SAVOIR** initiative:
  - Opportunity to bridge (or make closer) the S/C, avionics and SW paradigms.
  - It provides further results to be considered in the definition of the On-Board Software Reference Architecture (OSRA).



STUDY OBJECTIVES

- The objectives of this study are threefold:

1. **Specification of avionics-relevant analyses.**

   The identification and detailed specification of the analyses relevant to support the avionics architectural design.

   It includes the prioritization of the various analyses with respect to their added value to the architects.

2. **Specification of modelling language features.**

   The specification of the modelling language features necessary to support the identified avionics-relevant analyses.

3. **Demonstration and prototyping.**

   The prototyping of software tooling to demonstrate the automation of the selected analyses based on a modelling language that complies to the specification defined within this study.

STUDY ACTIVITIES

INNOVATING SOLUTIONS

STUDY ACTIVITIES

- Three main activities:
  - Activity 1. Specification of the avionics-relevant analyses.
  - Activity 2. Specification of the modelling language features.
  - Activity 3. Demonstration and prototyping.

ACTIVITY 1 – EVALUATION OF AVIONICS-RELEVANT ANALYSES

- Several **Use Cases** were selected from real missions:
  - Goal: Identify the relevant avionics analyses and their priorities.
  - Missions: Sentinel 3, GöKTürk, Herschel/Planck, MTG and ExoMars.
- **Result**: A catalogue and a complete description of all the analyses of interest for the avionics design in the different phases of development, including their inputs and expected results.

Analysis	Priority	Complexity	Weight on Design
Satellite mode definition, RAMS, FDIR and autonomy concept	HIGH	HIGH	HIGH
Design consistency and correctness checks	HIGH	LOW	HIGH
Commandability and observability	MEDIUM → HIGH	MEDIUM	LOW
Bus load and data latency	LOW → HIGH	LOW → HIGH	MEDIUM
Space/ground communication	LOW→ HIGH	HIGH	LOW → MEDIUM
Avionics resources	MEDIUM	LOW	MEDIUM
On-board functions and performance	MEDIUM	MEDIUM	MEDIUM
Power and mass	MEDIUM	LOW	MEDIUM

ACTIVITY 1 – SELECTION OF AVIONICS-RELEVANT ANALYSES

- **Selection of 3 analyses**:

Inputs

- Analysis of the priority, impact on the design and criticality of the analyses in different missions.
- Detailed description of each analysis (including the inputs, outputs and tasks along the different phases of the development).

Criteria

- Relevance for the Space Domain.
- Complexity of the implementation.
- The connection among them.

Result

- Commandability and observability.
- Bus load and data latency.
- On-board functions and performance.

- **Selection of the use case**: Sentinel 3 mission.

ACTIVITY 1 – COMMANDABILITY AND OBSERVABILITY ANALYSIS

- **Goal**: Size the RF communication system.

- **Metrics**: Data throughput [bps], link occupation [%], link occupation margin.

  - Coarse-grained analysis (Phases: 0 to B). Few information on the equipment needs in terms of TM/TC is available. Estimations are made based on the information defined and on the knowledge of similar missions.

  - Fine-grained analysis (Phases: C to F). It is based on accurate real data at equipment level.

ACTIVITY 1 – BUS LOAD AND DATA LATENCY ANALYSIS (1/2)

- **Bus load and data latency: RS-422/RS-232/RS-485**.
  - Goal: Size the RS-422/RS-232/RS-485 serial links.
  - Metrics: Data latency [ms], message transmission time [ms], bus load [%], bus margin, bus utilization.
    - Coarse-grained analysis (Phases: 0 to B). The message size is based on estimations.
    - Fine-grained analysis (Phases: C to D). Accurate real inputs are used.

ACTIVITY 1 – BUS LOAD AND DATA LATENCY ANALYSIS (2/2)

- **Bus load and data latency: MIL-STD-1553**.
  - Goal: Size the MIL-STD-1553 bus.

    Note. Only BC-RT and RT-BC patterns are considered.
  - MIL-STD-1553 schedulability analysis.
  - Coarse-grained analysis (Phases: 0 to B). Message size is based on estimations and the bus occupation profile is not defined.
    - Metrics: Data latency [ms], message transmission time [ms], bus load per minor frame [%], bus load per major frame [%].
  - Fine-grained analysis (Phases: C to D). All the inputs required at equipment level are available.
    - Metrics: Data latency [ms], message transmission time [ms], bus load [%], bus margin [%], bus utilization [%].

ACTIVITY 1 – ON-BOARD FUNCTIONS AND PERFORMANCE ANALYSIS

- **Goal**: Analyse the CPU load and memory sizing.
  - **CPU Metrics**: CPU usage [%], CPU throughput [MIPS], CPU usage margin [%].
    - Coarse-grained analysis (Phases: 0 to B). WCET cannot be measured. It is computed based on estimations on the size of the code.
    - Fine-grained analysis (Phases: C to F) based on the WCET already available.
  - **Memory Metrics**: Non-volatile/volatile memory size [MB], non-volatile/volatile memory margins[%].
    - Coarse-grained analysis (Phases: 0 to B). A default stack size is assigned.
    - Fine-grained analysis (Phases: C to F). The stack size of each function is computed.

STUDY ACTIVITIES

- Three main activities:
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ACTIVITY 2 – AAML MODELLING PROCESS

Avionics Functional Definition

- Used to design the avionics system as a set of high-level functions.
- It answers directly to what the avionics is supposed to do.

Logical Architecture Definition

- Representation of how the system will work so as to fulfil the requirements and expectations of the users.

Physical Architecture Definition

- It represents how the system will be concretely developed and built using real components.

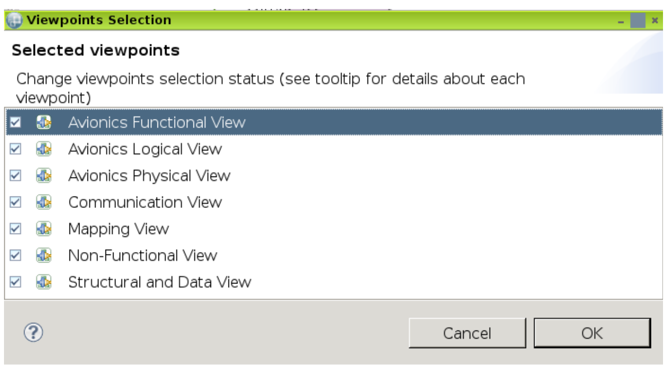
Non-Functional Properties Definition

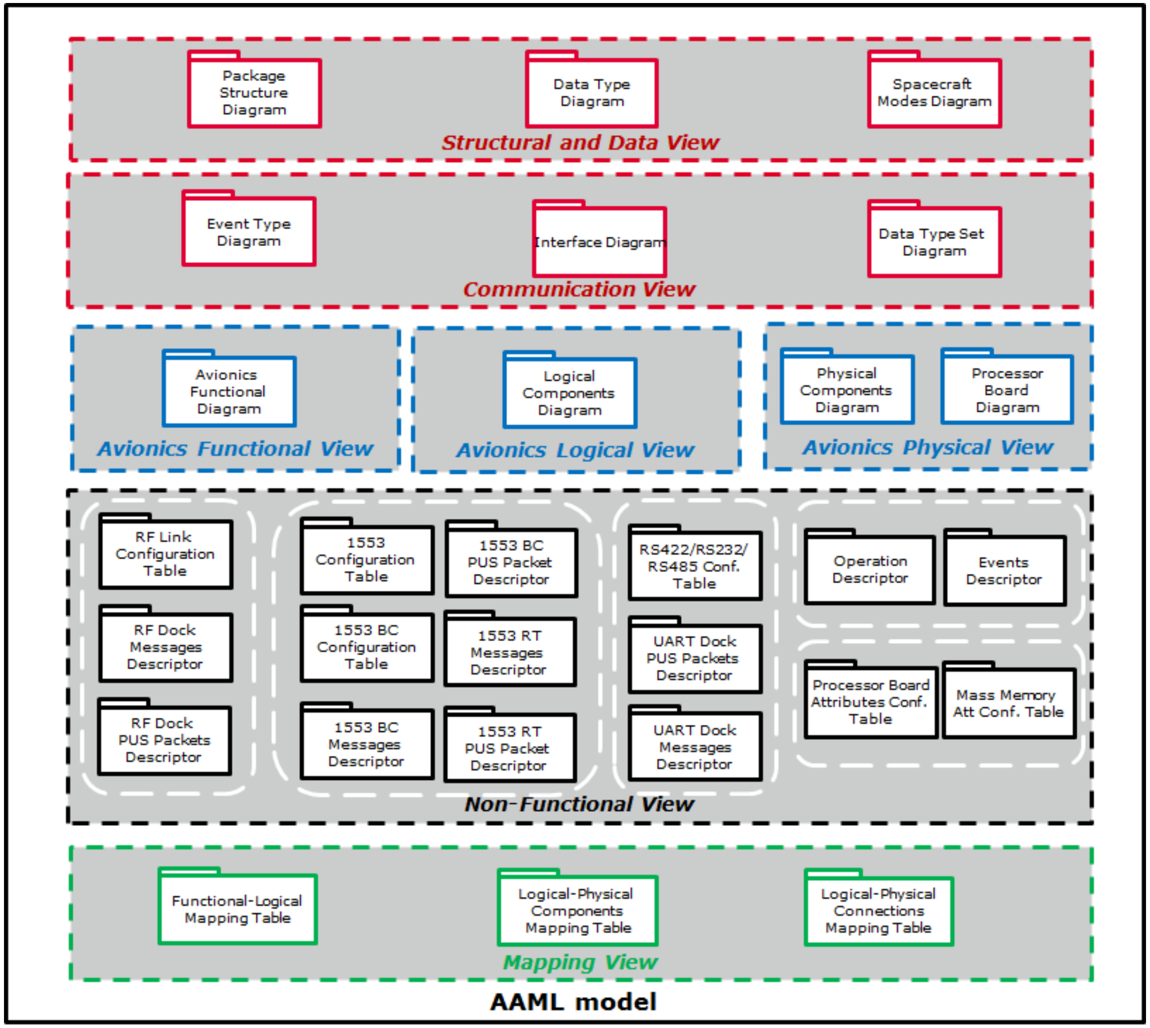
ACTIVITY 2 – AAML MODELLING LANGUAGE

- Definition of the **AAML Modelling Language**.
  - Entities: general entities, data model, avionic entities (e.g., avionic function, logical component, physical components), communication entities (e.g., operation), interaction entities (e.g., interface port), state modelling.
  - Non-functional properties to describe the entities in the various non-functional dimensions of interest.
- Elaboration of **Language Extension Mechanisms**.
  - AAML is a domain specific language (DSL).
  - Evaluation:
    - Approaches: (i) Usage of profiles or (ii) the implementation of a new meta-model based on some metamodel language.
    - Modelling languages: AADL, UML, SysML, MARTE, CHESS-ML (CHESS project) and Space Component Model (adopted and extended in COrDeT activities for OSRA).
  - Selection:
    - SCM was selected as the inspiration for the definition of the AAML implementation.
  - Implementation:
    - AAML modelling language is split into two parts: *AAML_Core* and *AAML_Extension*.

ACTIVITY 2 – AAML DESIGN VIEWS

- Definition of the **AAML Design Views**.
  - Representation of a the whole system from the perspective of a related set of concerns.
  - In AAML, there are specialized representations of the system according to the avionics design phase (Avionics Functional, Logical and Physical Views).





STUDY ACTIVITIES

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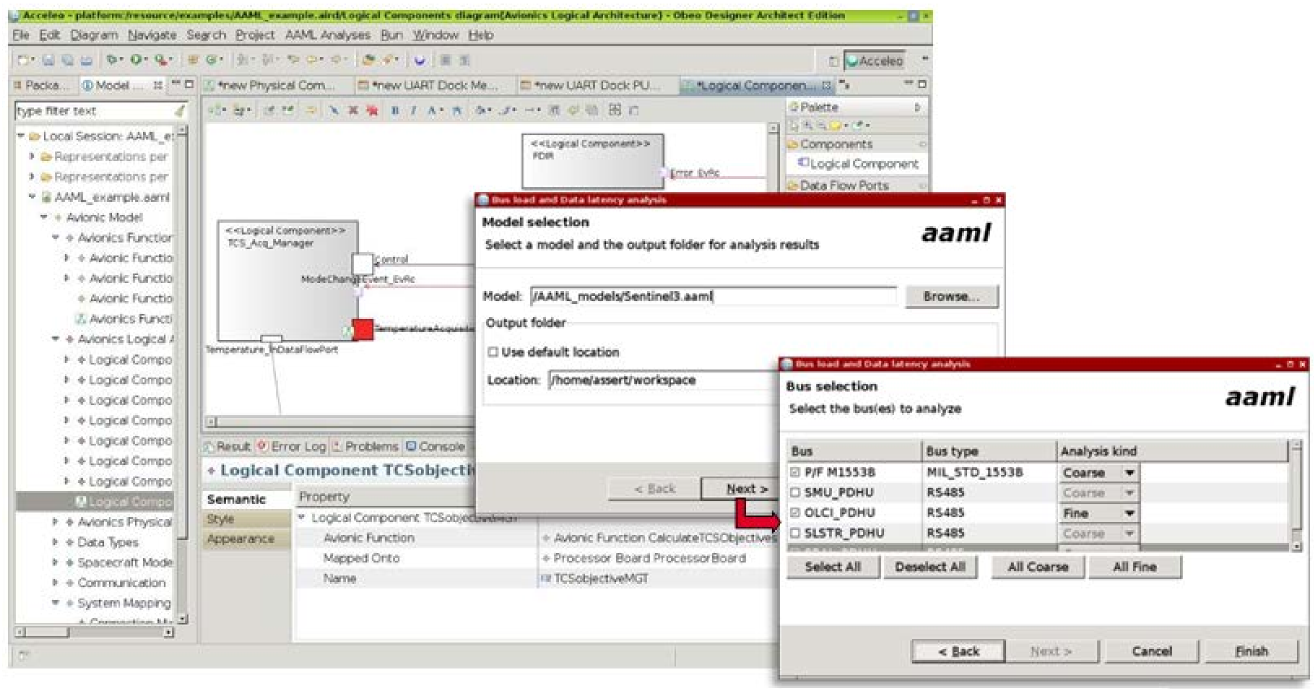
ACTIVITY 3 – DEMONSTRATION AND PROTOTYPING (1/2)

- Goal:
  - Implementation of a prototype demonstrator for a graphical editor (design views) and analyses tools.
- Technology:
  - Developed as a set of Eclipse plug-ins that configure a design and analysis environment integrated into the Eclipse platform.
  - Obeo Designer is used for the graphical editor.
- Capabilities:
  - Creation/modification of an AAML model through the graphical editor.
    - Usage of different Design Views.
    - Edition by means of different kinds of diagrams/tables.
  - Configuration of the avionics analyses from a GUI based on Eclipse wizards.
  - Execution of the avionics analyses.
  - Identification of model inconsistences.

ACTIVITY 3 – DEMONSTRATION AND PROTOTYPING (2/2)

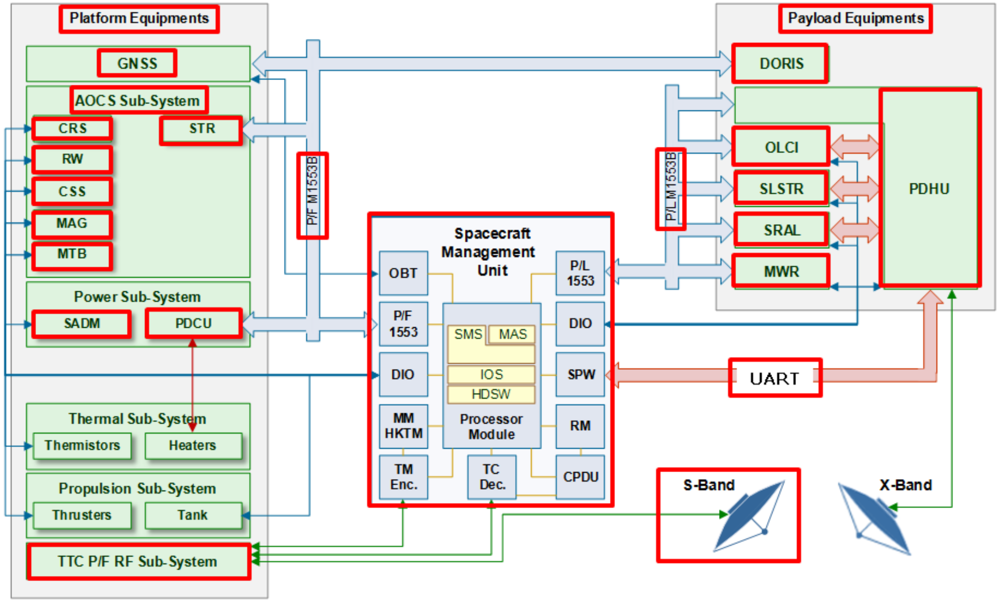
- Analysis outputs:
  - A file containing the analysis results.
  - A file containing debug information, where the user may examine which model elements/properties were used for computing the analysis results.
  - A set of error/warning messages when issues are detected during the analysis.
- Demonstration:
  - Sentinel-3 Use Case.



PROTOTYPE DEMONSTRATION– USE CASE

PROTOTYPE DEMONSTRATION – USE CASE

- Use Case:
  - It was intended to demonstrate at full extend all the capabilities of the AMML modelling methodology, meta-model and toolset as well as its corresponding avionics analyses.
  - It was based on the **Sentinel-3 mission**.
  - It allowed:
    - Exercising various analyses at avionics level based on a real case with a classical complexity level.
    - Ensuring that the approach proposed in the study was compatible with the vision on the On-Board Software Reference Architecture.
    - The use case aimed at being rich enough to evaluate all the aspects of the approach.



PROTOTYPE DEMONSTRATION – STEPS

- Steps:
  - Functional Architecture Definition.
  - Logical Architecture Definition.
  - Physical Architecture Definition.
- Execution of the analysis.

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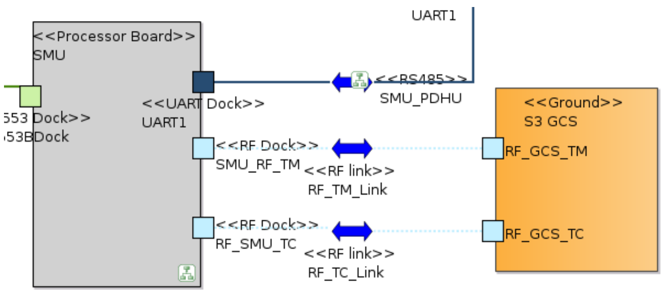
PROTOTYPE DEMONSTRATION – C&O AND 1553B RESULTS



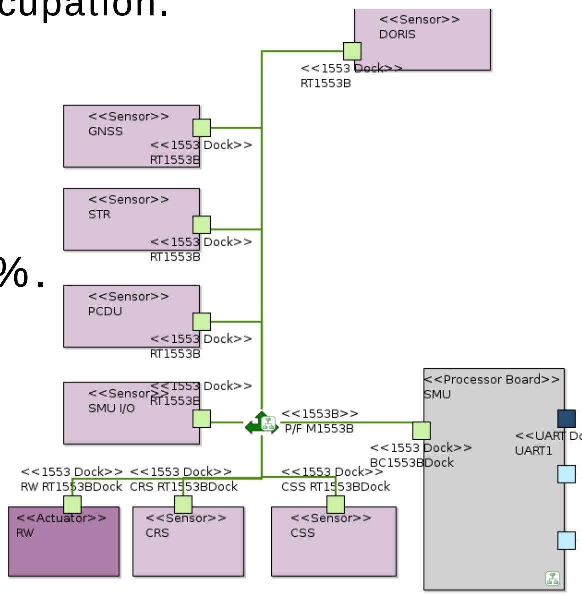
❑ Commandability and observability.

- TM link at very low level of occupation (1.3-2.6%).
- TC links:
  - o Assumption of visibility window of 10 min.
  - o TC upload of SRAL binary: 7974 bps, 55.1% of occupation.
  - o TC upload of CSW binary: 20796 bps, 143.7% of occupation.

❑ Bus load: 1553B.

- Scheduling: Major frame of 1000 ms and a minor frame of 125 ms.
- Fine-grained analysis computes a bus load of 14%.

Coarse-grained Analysis
Bus 'P/F M1553B' Mode 'Normal':
Bus load: 35.839993 %
Bus system load: 36.82166 %
Data throughput: 358400 bps
Major frame load: 36.821655 %
Minor frame load: 91.52813 %
Fine-grained Analysis
Bus load: 13.938399 %
Bus system load: 11.956026 %
Data throughput: 139384 bps

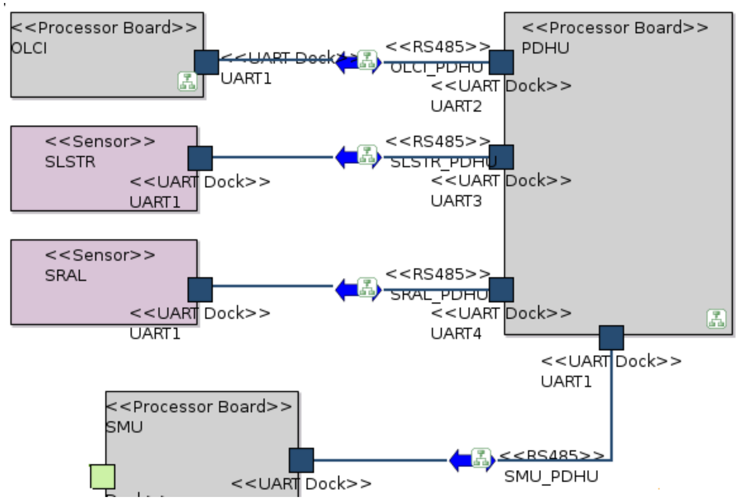


PROTOTYPE DEMONSTRATION – UART RESULTS

❑ Bus load: UART.

- Fine-grained analysis detects that SRAL-PDHU data exchange exceeds bus capability (due to calibration messages).

Bus 'OLCI_PDHU'
Mode 'Normal':
Bus load: 47.5573 %
Bus system load: 48.770016 %
Data throughput: 95114608 bps
Bus 'SLSTR_PDHU'
Mode 'Normal':
Bus load: 26.623524 %
Bus system load: 26.793247 %
Data throughput: 13311762 bps
Bus 'SRAL_PDHU'
Mode 'Normal':
Bus load: ***118.250046 %***
Bus system load: 119.00389 %
Data throughput: 59125020 bps
Bus 'SMU_PDHU'
Mode 'Normal':
Bus load: 0.63666666 %
Bus system load: 1.4159467 %
Data throughput: 61120 bps

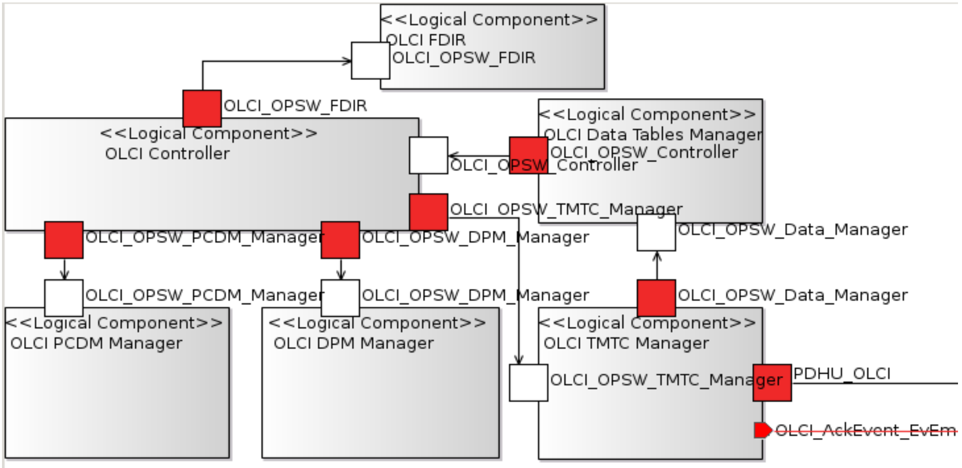


- After introduction of calibration mode the bus load is reduced to 55.4% (normal) and 62.8% (calibration).

PROTOTYPE DEMONSTRATION – ON-BOARD FUNCTIONS AND PERFORMANCE RESULTS

On-board functions and performance.

- Firstly, only one EEPROM is used.
- The fined-grained analysis detects:
  - Computation of CPU load of OLCI OPSW: **51.6%**.
  - SRAM occupation of **35.7%** (below 50%).
  - High EEPROM1 occupation: **124.4%**.
- Reallocation of DPM, PCDM, FDIR, PDHU PL and SMU logical components over EEPROM2:
  - EEPROM1 occupation: **67.3%**.
  - EEPROM2 occupation: **56.9%**.



CONCLUSIONS AND FUTURE WORK

CONCLUSIONS

- AAML study has provided:
  - **Identification and evaluation of the avionics analyses**.
  - **AAML modelling language**:
    - The set of entities and non-functional properties included in the language are **precise and practical** enough for capturing the avionics architecture and to be used as input for specialized avionics analysis.
    - The language suitably supports the possibility of both **coarse- and fine-grained specification** by means of the non-functional properties defined.
    - The three levels of definition (functional, logical and physical) supported by the language provide all the necessary means to manage the **different phases** of conception and implementation of the avionics system.
  - **AAML toolset**:
    - **Design and analysis** of the avionics system.
      - The execution of the avionics analysis process is fast and easy to follow.
      - The analysis outputs are useful to confirm or modify the system design and to detect model inconsistencies or missing information.

FUTURE WORK

- Some future work activities have been identified during this study.
- They represent **improvements in the modelling language and the toolset**.
- The future work activities have been prioritized: High, Medium, Low.
- Some **examples**:

Future Work	Priority
Extend the meta-model and toolset to support additional avionic analyses	MEDIUM
Improve the analysis reports output format	MEDIUM
Develop and independent model consistency validator	HIGH
Include hierarchy levels	MEDIUM
Modelling errors	LOW

Thank you

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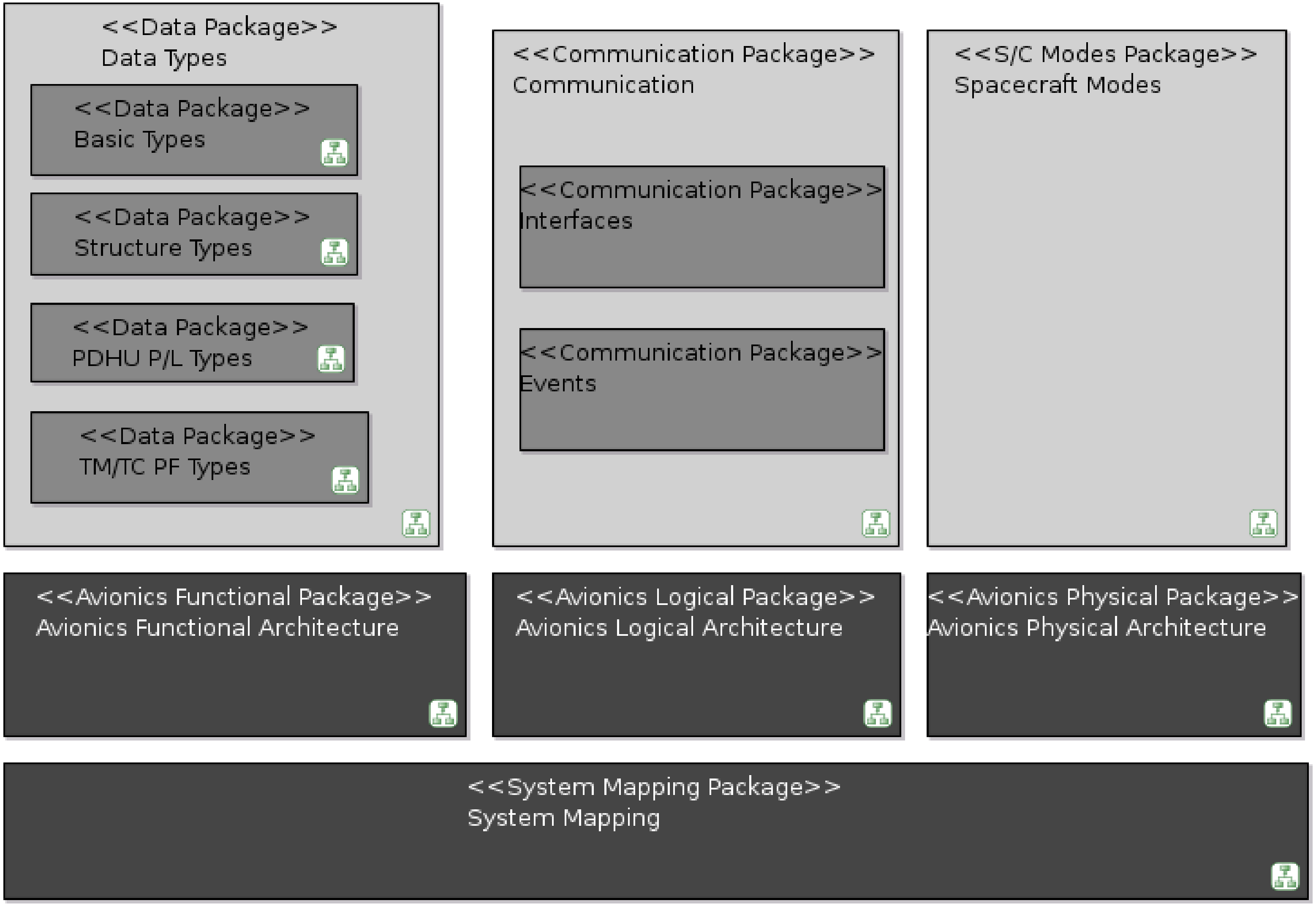
Space Systems Business Unit
Avionics & On-Board SW Division

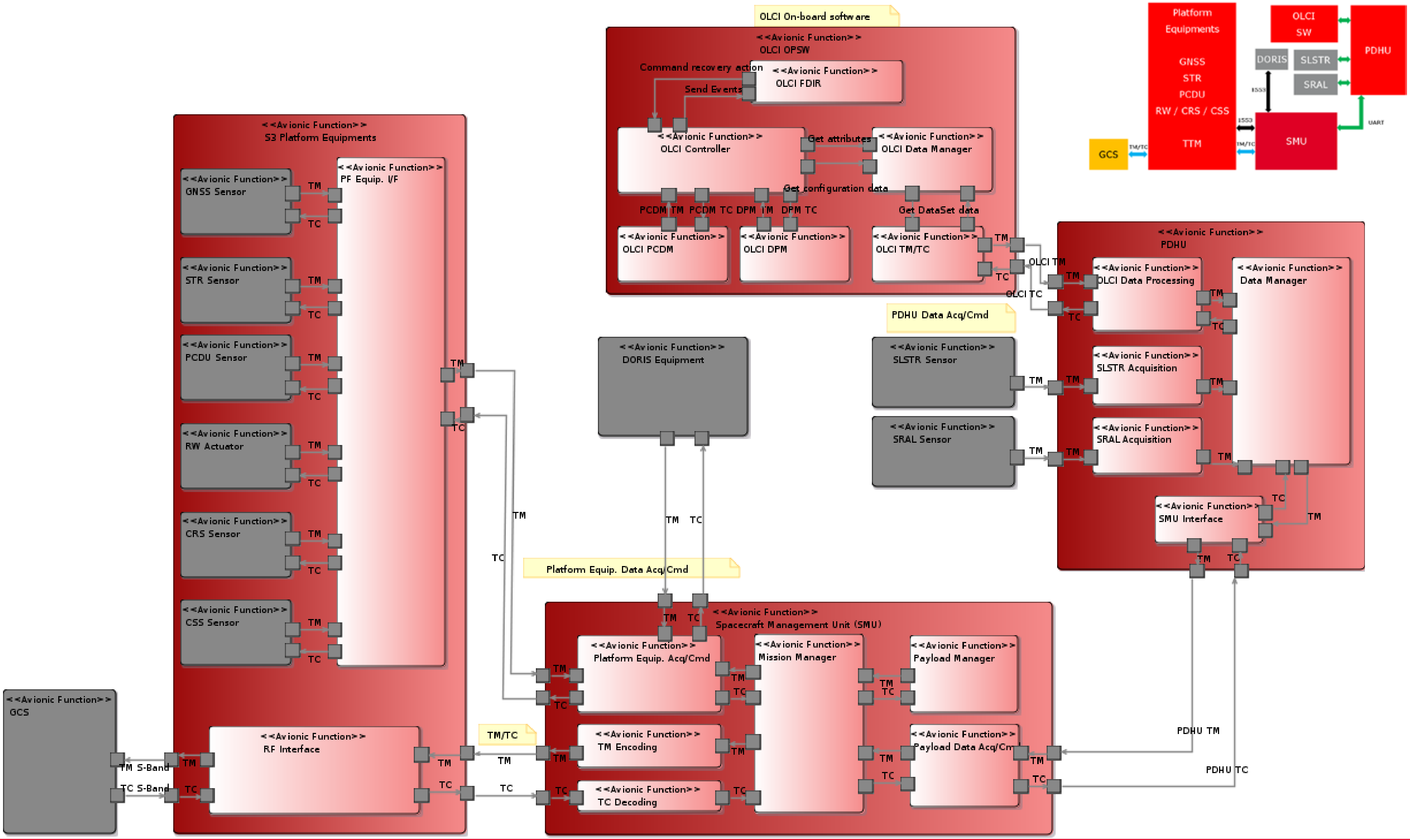
INNOVATING SOLUTIONS

USE CASE IMAGES

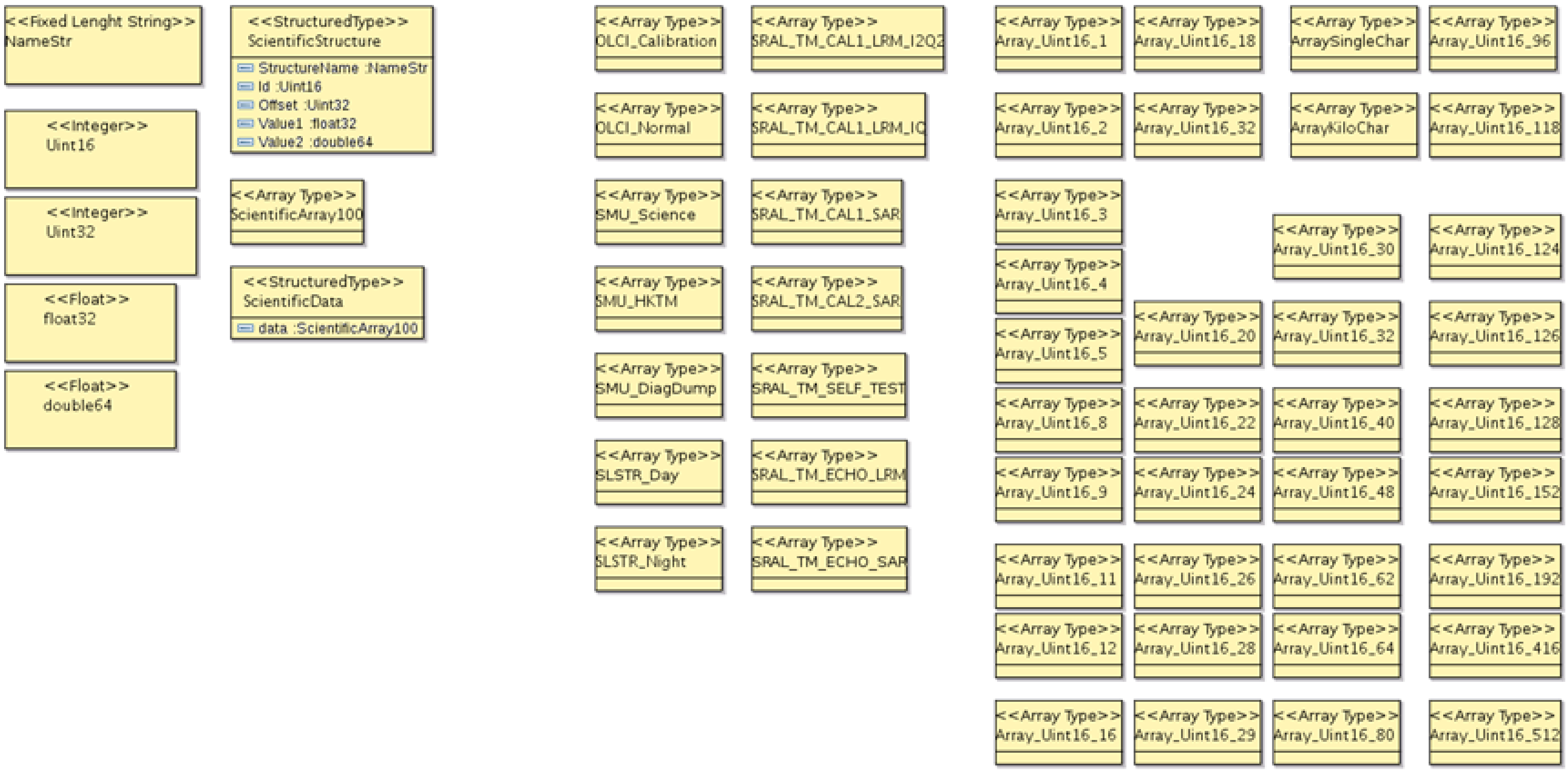
SENTINEL 3: PACKAGE STRUCTURE



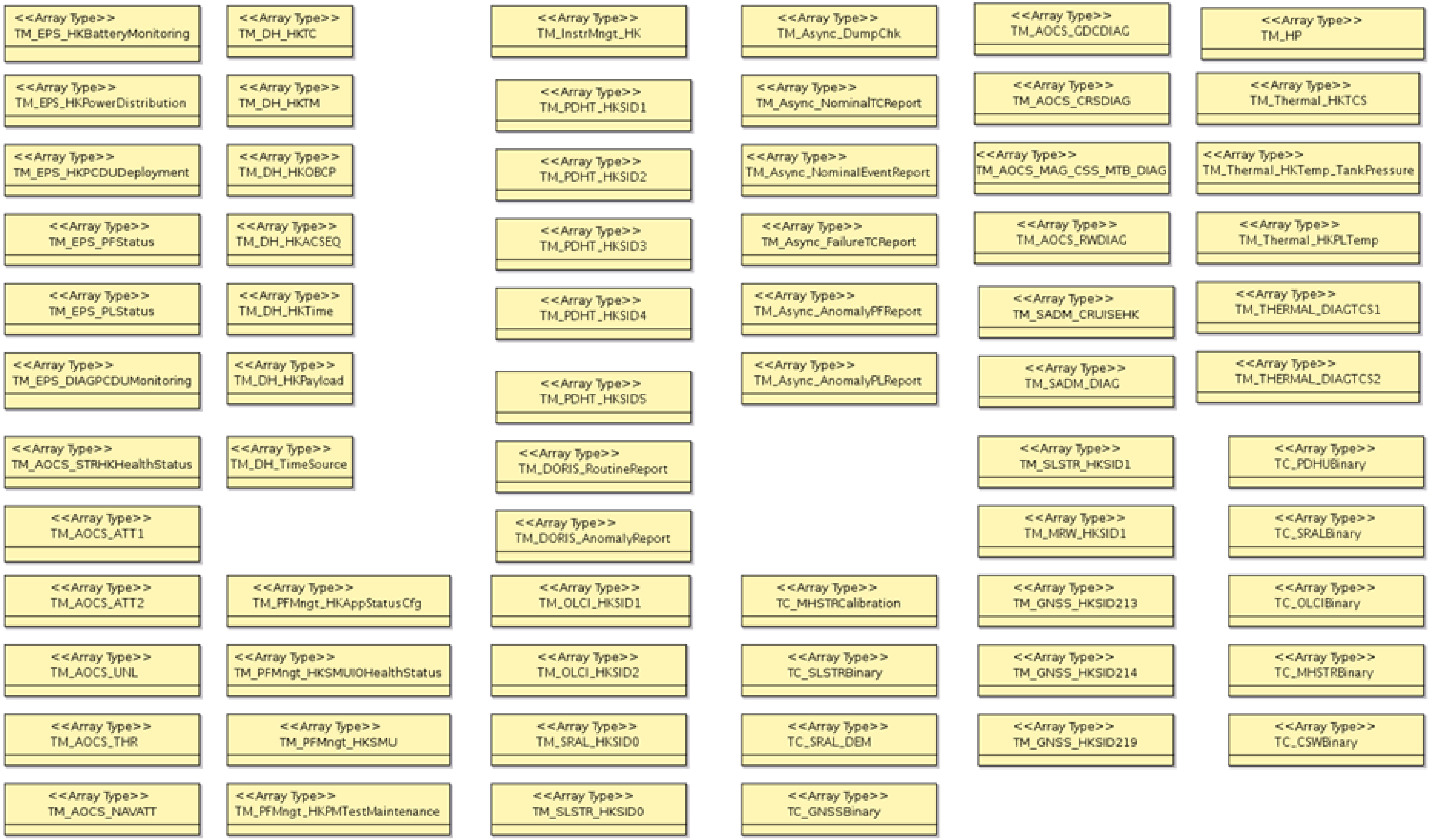
SENTINEL 3: AVIONICS FUNCTIONAL DIAGRAM



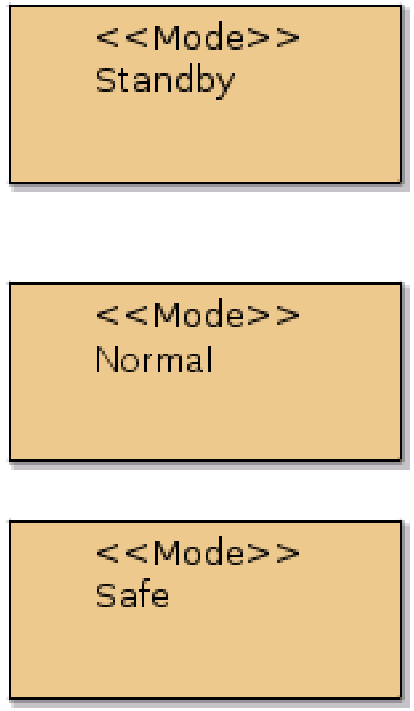
SENTINEL 3: DATA TYPES (I)



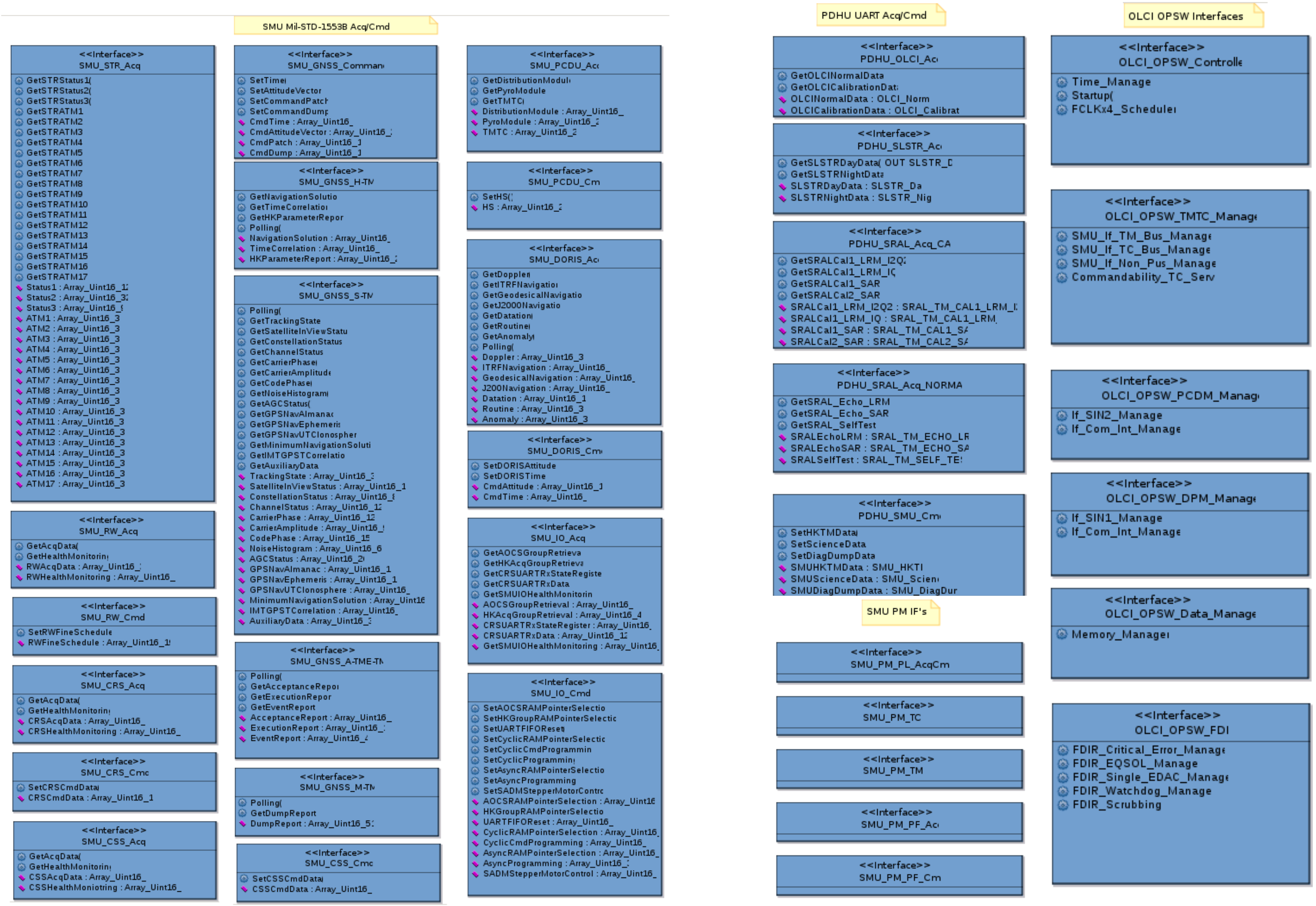
SENTINEL 3: DATA TYPES (II)



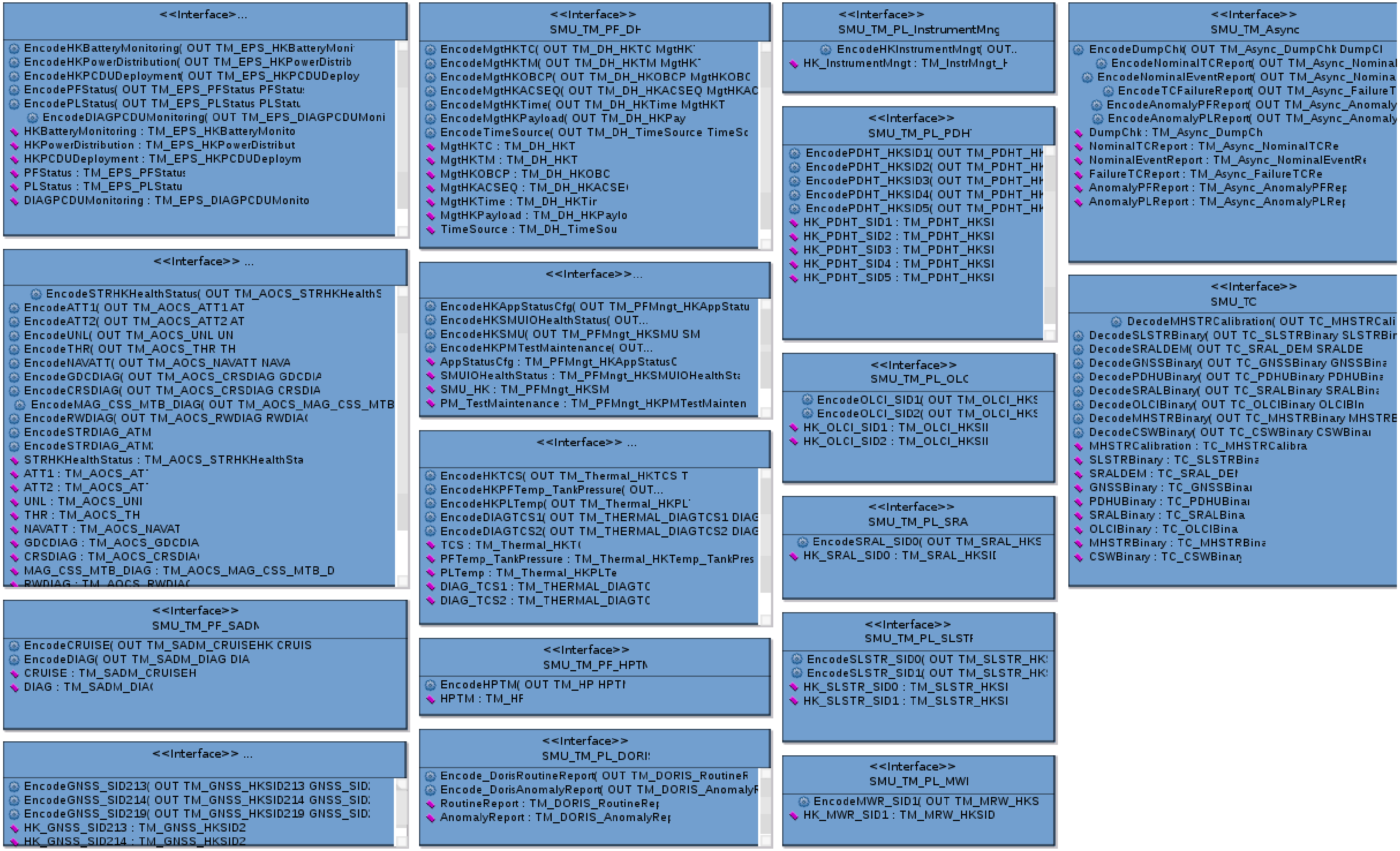
SENTINEL 3: SPACECRAFT MODES



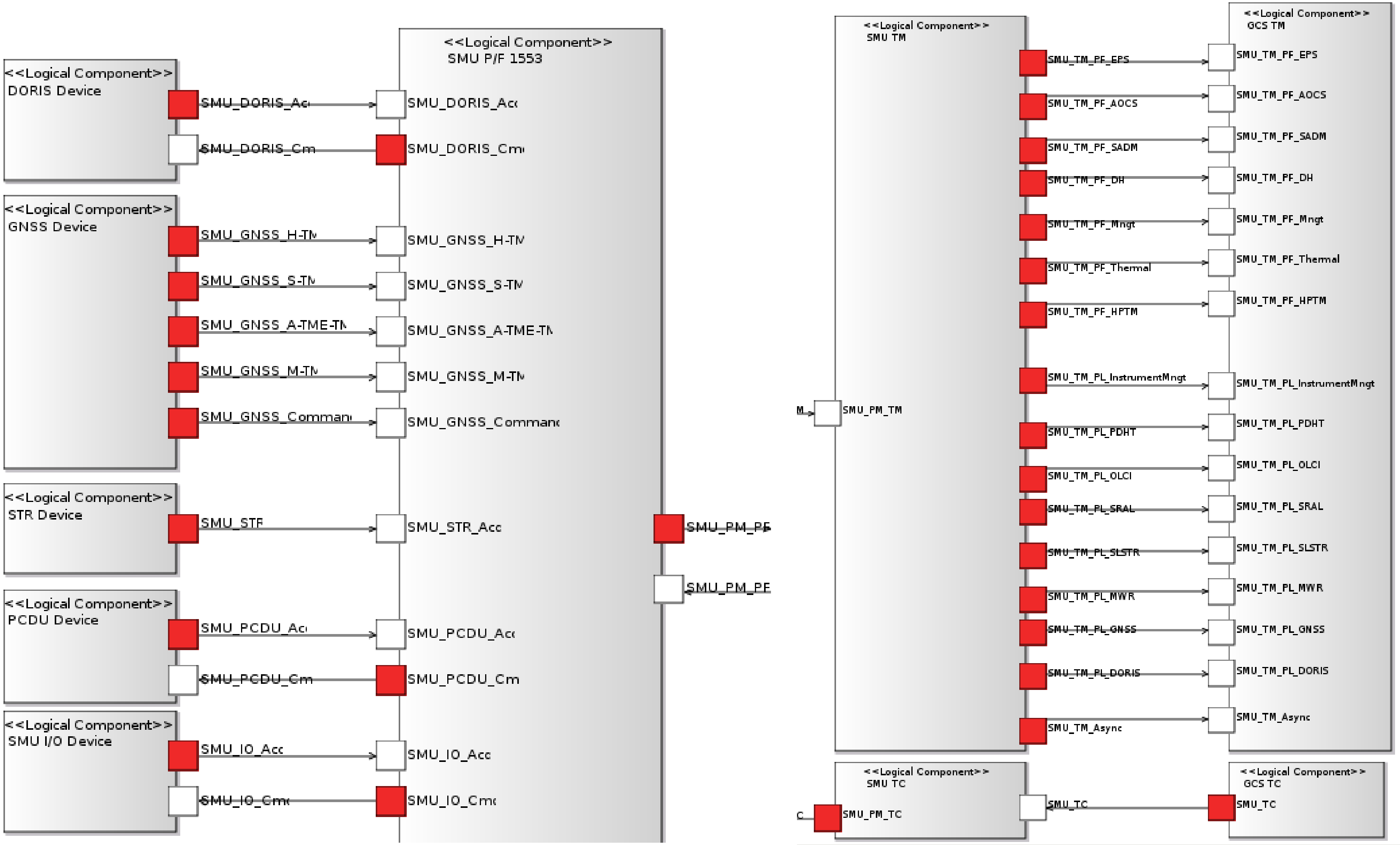
SENTINEL 3: COMMUNICATION ENTITIES (I)



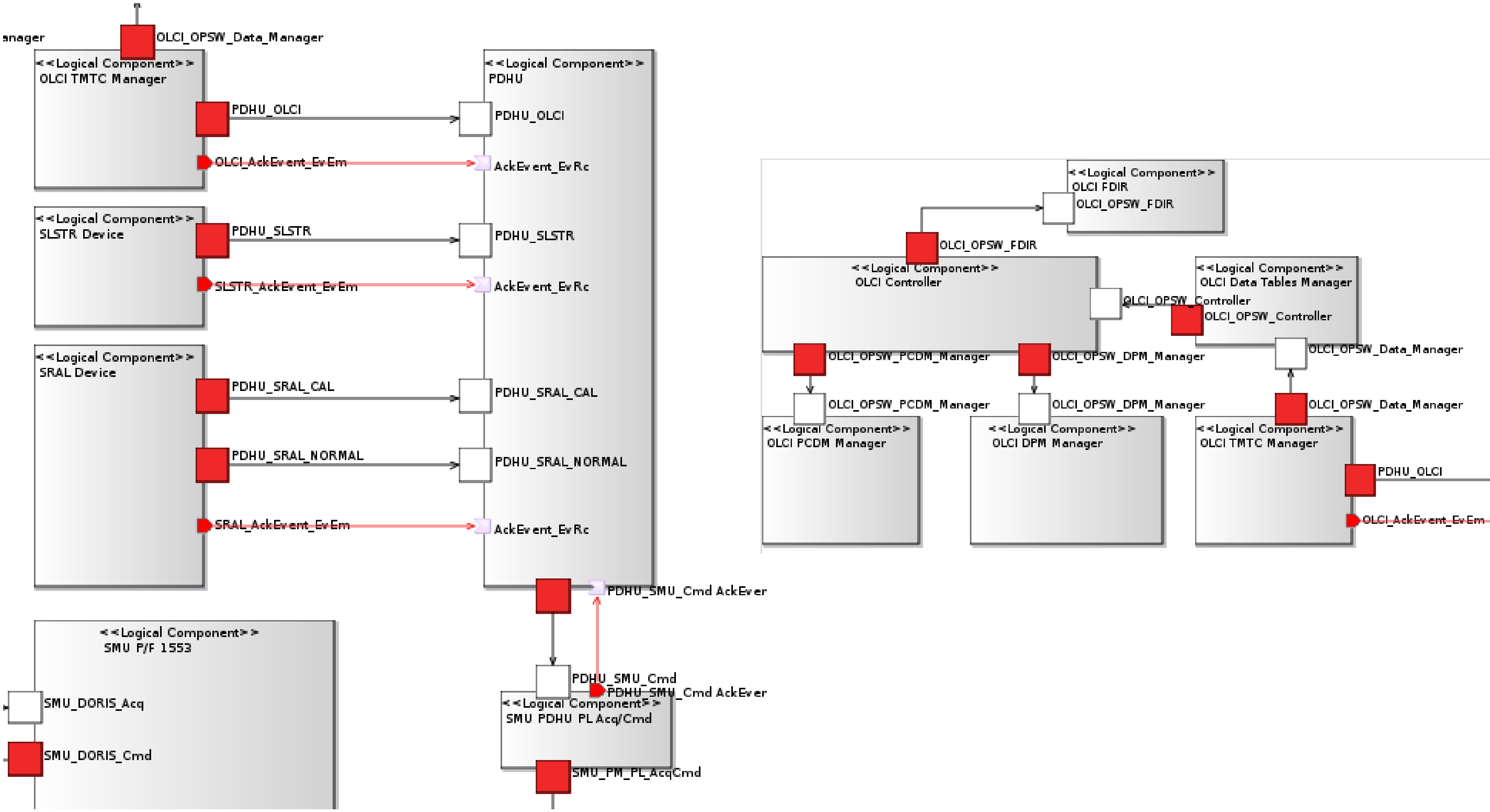
SENTINEL 3: COMMUNICATION ENTITIES (II)



SENTINEL 3: AVIONICS LOGICAL DIAGRAM (I)



SENTINEL 3: AVIONICS LOGICAL DIAGRAM (II)



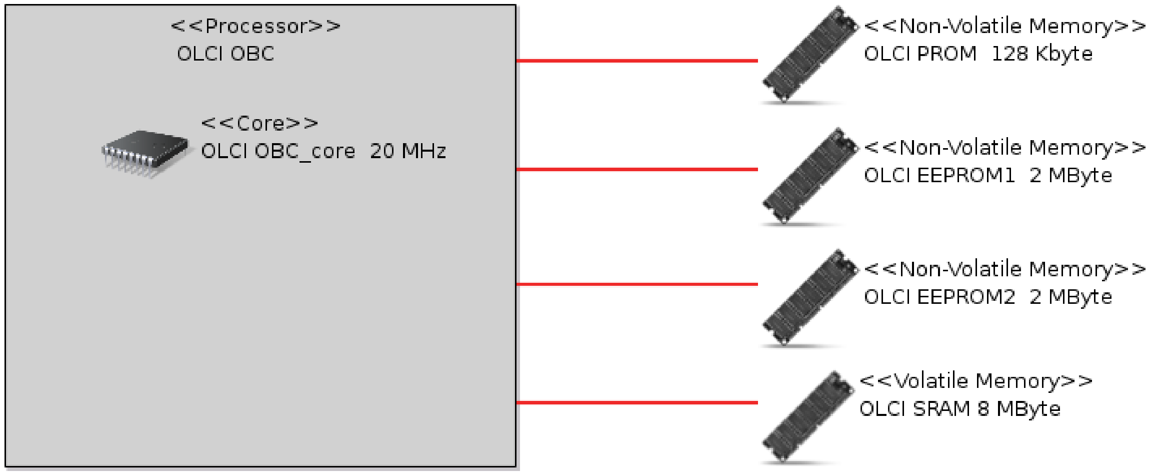
SENTINEL 3: MAPPING FROM AVIONICS FUNCTIONS TO LOGICAL COMPONENTS (I)

Avionic Function OLCI OPSW	Logical Component OLCI Controller
Avionic Function OLCI FDIR	Logical Component OLCI FDIR
Avionic Function OLCI Controller	Logical Component OLCI Controller
Avionic Function OLCI Data Tables	Logical Component OLCI Data Tables Manager
Avionic Function OLCI TM/TC	Logical Component OLCI TMTC Manager
Avionic Function OLCI PCDM	Logical Component OLCI PCDM Manager
Avionic Function OLCI DPM	Logical Component OLCI DPM Manager
Avionic Function PDHU	Logical Component PDHU
Avionic Function PDHU OLCI Acq/Cmd	Logical Component PDHU
Avionic Function PDHU Data Manager	Logical Component PDHU
Avionic Function PDHU SLSTR Acq	Logical Component PDHU
Avionic Function PDHU SMU IF	Logical Component PDHU, Logical Component SMU I/O Device
Avionic Function PDHU SRAL Acq	Logical Component PDHU
Avionic Function Spacecraft Management Ur	Logical Component SMU Processor Module
Avionic Function SMU PDHU PL Acq/Cmd	Logical Component SMU PDHU PL Acq/Cmd, Logical Component PDHU
Avionic Function SMU Processor Module	Logical Component SMU Processor Module
Avionic Function SMU TM Encoder	Logical Component SMU TM
Avionic Function SMU P/F 1553	Logical Component SMU P/F 1553
Avionic Function SMU P/L 1553	
Avionic Function SMU TC Decoder	Logical Component SMU TC
Avionic Function SLSTR Sensor	Logical Component SLSTR Device
Avionic Function SRAL Sensor	Logical Component SRAL Device

SENTINEL 3: MAPPING FROM AVIONICS FUNCTIONS TO LOGICAL COMPONENTS (II)

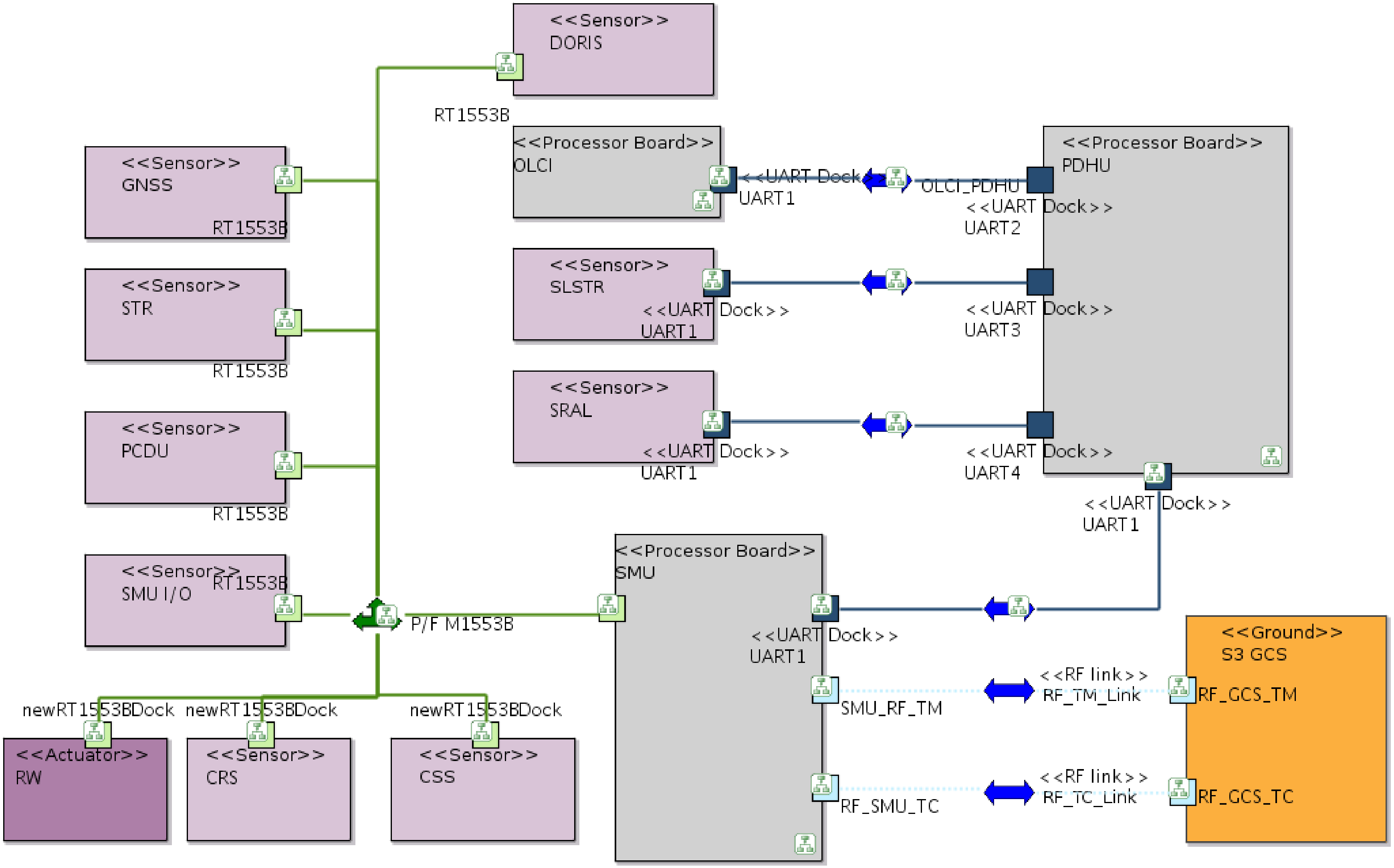
Avionic Function S3 Platform Equipments	Logical Component SMU Processor Module
Avionic Function PF TTC RF	
Avionic Function PF 1553 I/F	Logical Component SMU P/F 1553
Avionic Function GNSS Sensor	Logical Component GNSS Device
Avionic Function STR Sensor	Logical Component STR Device, Logical Component SLSTR Device
Avionic Function PCDU Sensor	Logical Component PCDU Device
Avionic Function RW Actuator	Logical Component RW Device
Avionic Function CRS Sensor	Logical Component CRS Device
Avionic Function CSS Sensor	Logical Component CSS Device
Avionic Function GCS	Logical Component GCS TM, Logical Component GCS TC
Avionic Function DORIS Equipment	Logical Component DORIS Device

SENTINEL 3: PROCESSOR BOARDS



- Processor OLCI OBC
  - Processor Core OLCI OBC_core
    - Frequency: 20 MHz
    - Typical Throughput: 16 MIPS
    - Instructions Per Line Of Code (only required for FINE analysis): 5
- Volatile Memory OLCI SRAM
  - Data Size: 8 MByte
- Non Volatile Memory OLCI PROM
  - Data Size: 128 Kbyte
- Non Volatile Memory OLCI EEPROM1
  - Data Size: 2 MByte
- Non Volatile Memory OLCI EEPROM2
  - Data Size: 2 MByte

SENTINEL 3: PHYSICAL ARCHITECTURE



SENTINEL 3: MAPPING FROM LOGICAL TO PHYSICAL COMPONENTS

	Physical Component	Processor Core (Only for	Non Volatile Memory Use	Volatile Memory Used (Only for Proc
Logical Component PDHU	Processor Board PDHU			
Processor Board Mapping Descriptor		Processor Core PDHU_Proc_core	Non Volatile Memory PDHU Non\	Volatile Memory PDHU VolatileMemory
Logical Component SRAL Device	Sensor SRAL			
Logical Component OLCI TMTC Manager	Processor Board OLCI			
Processor Board Mapping Descriptor		Processor Core OLCI OBC_core	Non Volatile Memory OLCI EEPR	Volatile Memory OLCI SRAM
Processor Board Mapping Descriptor		Processor Core OLCI OBC_core	Non Volatile Memory OLCI EEPR	Volatile Memory OLCI SRAM
Logical Component SLSTR Device	Sensor SLSTR			
Logical Component SMU P/F 1553	Processor Board SMU			
Processor Board Mapping Descriptor		Processor Core SMU_Proc_core	Non Volatile Memory SMU NonVo	Volatile Memory SMU VolatileMemory
Logical Component STR Device	Sensor STR			
Logical Component GNSS Device	Sensor GNSS			
Logical Component PCDU Device	Sensor PCDU			
Logical Component DORIS Device	Sensor DORIS			
Logical Component GCS TM	Ground S3 GCS			
Logical Component SMU TM	Processor Board SMU			
Processor Board Mapping Descriptor		Processor Core SMU_Proc_core	Non Volatile Memory SMU NonVo	Volatile Memory SMU VolatileMemory
Logical Component SMU TC	Processor Board SMU			
Processor Board Mapping Descriptor		Processor Core SMU_Proc_core	Non Volatile Memory SMU NonVo	Volatile Memory SMU VolatileMemory
Logical Component GCS TC	Ground S3 GCS			
Logical Component SMU I/O Device	Sensor SMU I/O			
Logical Component RW Device	Actuator RW			
Logical Component CSS Device	Sensor CSS			
Logical Component OLCI Data Tables Ma	Processor Board OLCI			
Processor Board Mapping Descriptor		Processor Core SMU_Proc_core	Non Volatile Memory OLCI EEPR	Volatile Memory OLCI SRAM
Logical Component OLCI Controller	Processor Board OLCI			
Processor Board Mapping Descriptor		Processor Core OLCI OBC_core	Non Volatile Memory OLCI PROM	Volatile Memory OLCI SRAM
Processor Board Mapping Descriptor		Processor Core SMU_Proc_core	Non Volatile Memory OLCI PROM	Volatile Memory OLCI SRAM
Logical Component OLCI DPM Manager	Processor Board OLCI			
Processor Board Mapping Descriptor		Processor Core SMU_Proc_core	Non Volatile Memory OLCI PROM	Volatile Memory OLCI SRAM
Logical Component OLCI PCDM Manager	Processor Board OLCI			
Processor Board Mapping Descriptor		Processor Core SMU_Proc_core	Non Volatile Memory OLCI PROM	Volatile Memory OLCI SRAM
Logical Component OLCI FDIR	Processor Board OLCI			
Processor Board Mapping Descriptor		Processor Core SMU_Proc_core	Non Volatile Memory OLCI PROM	Volatile Memory OLCI SRAM
Logical Component SMU PDHU PL Acq/(	Processor Board SMU			
Processor Board Mapping Descriptor		Processor Core SMU_Proc_core	Non Volatile Memory OLCI PROM	Volatile Memory OLCI SRAM
Logical Component SMU Processor Moc	Processor Board SMU			
Processor Board Mapping Descriptor		Processor Core SMU_Proc_core	Non Volatile Memory OLCI PROM	Volatile Memory OLCI SRAM

SENTINEL 3: MAPPING FROM LOGICAL TO PHYSICAL CONNECTIONS

S3 Logical Connections - Physical Connections Mapping Table

	Connection	HW Communication Media	TC/TM Standard
Mapping: RF-TM_PF_EPS Connection	Interface Connection communicationSMU_TM_PF_EPSSMU_TM_PF_EPS	RFlink RF_TM_Link	PUS
Mapping: RF-TC Connection	Interface Connection communicationSMU_TCSMU_TC	RFlink RF_TC_Link	PUS
Mapping: RF-TM_PF_AOCS Connection	Interface Connection communicationSMU_TM_PF_AOCS	RFlink RF_TM_Link	PUS
Mapping: RF-TM_PF_SADM Connection	Interface Connection communicationSMU_TM_PF_SADMSMU_TM_PF_SADM	RFlink RF_TM_Link	PUS
Mapping: RF-TM_PF_DH Connection	Interface Connection communicationSMU_TM_PF_DHSMU_TM_PF_DH	RFlink RF_TM_Link	PUS
Mapping: RF-TM_PF_Mngt Connection	Interface Connection communicationSMU_TM_PF_MngtSMU_TM_PF_Mngt	RFlink RF_TM_Link	PUS
Mapping: RF-TM_PF_Thermal Connectic	Interface Connection communicationSMU_TM_PF_ThermalSMU_TM_PF_Thermal	RFlink RF_TM_Link	PUS
Mapping: RF-TM_PF_HPTM Connection	Interface Connection communicationSMU_TM_PF_HPTMSMU_TM_PF_HPTM	RFlink RF_TM_Link	PUS
Mapping: RF-TM_PL_InstrMngt Connect	Interface Connection communicationSMU_TM_PL_InstrumentMngtSMU_TM_PL_Ir	RFlink RF_TM_Link	PUS
Mapping: RF-TM_PL_PDHT Connection	Interface Connection communicationSMU_TM_PL_PDHTSMU_TM_PL_PDHT	RFlink RF_TM_Link	PUS
Mapping: RF-TM_PL_OLCI Connection	Interface Connection communicationSMU_TM_PL_OLCISMU_TM_PL_OLCI	RFlink RF_TM_Link	PUS
Mapping: RF-TM_PL_SRAL Connection	Interface Connection communicationSMU_TM_PL_SRALSMU_TM_PL_SRAL	RFlink RF_TM_Link	PUS
Mapping: RF-TM_PL_SLSTR Connection	Interface Connection communicationSMU_TM_PL_SLSTRSMU_TM_PL_SLSTR	RFlink RF_TM_Link	PUS
Mapping: RF-TM_PL_MWR Connection	Interface Connection communicationSMU_TM_PL_MWRSMU_TM_PL_MWR	RFlink RF_TM_Link	PUS
Mapping: RF-TM_PL_GNSS Connection	Interface Connection communicationSMU_TM_PL_GNSSSMU_TM_PL_GNSS	RFlink RF_TM_Link	PUS
Mapping: RF-TM_PL_DORIS Connection	Interface Connection communicationSMU_TM_PL_DORISSMU_TM_PL_DORIS	RFlink RF_TM_Link	PUS
Mapping: 1553-SMU_GNSS_A-TME-TM (	Interface Connection communicationSMU_GNSS_A-TME-TM	MIL STD 1553B P/F M1553B	PUS
Mapping: RF-TM_Async Connection	Interface Connection communicationSMU_TM_AsyncSMU_TM_Async	RFlink RF_TM_Link	PUS
Mapping: 1553-SMU_DORIS_Acq Conn	Interface Connection communicationSMU_DORIS_AcqSMU_DORIS_Acq	MIL STD 1553B P/F M1553B	PUS
Mapping: 1553-SMU_GNSS_H-TM Conn	Interface Connection communicationSMU_GNSS_H-TM	MIL STD 1553B P/F M1553B	PUS
Mapping: 1553-SMU_STR_Acq Connect	Interface Connection communicationSMU_STR	MIL STD 1553B P/F M1553B	PUS

SENTINEL 3: OPERATION DESCRIPTORS (TM/TC)

	S/C Mode	Type [S/A]	Freq./MIAT [Hz]	Packet
RF Dock: SMU_RF_TM				
Operation: EncodeHKBatteryMonitoring	Mode Normal	SYNCHRONOUS	0.03125	
Packet Standard				PUS
Operation: EncodeHKPowerDistribution	Mode Normal	SYNCHRONOUS	0.125	
Packet Standard				PUS
Operation: EncodeHKPCDUDeployment	Mode Normal	SYNCHRONOUS	1.0E-9	
Packet Standard				PUS

SMU_TM RF Dock PUS Packets Descriptor

	Service Type	Sub-Service Type	Data Field [Byte]	Overhead [Byte]	Nº Packets (Optional)
RF Dock: SMU_RF_TM					
Operation: EncodeHKBatteryMonitorir					
PUS Descriptor	128	128	45.0	20.0	
Number Packets					1
Operation: EncodeHKPowerDistributic					
PUS Descriptor	128	128	130.0	20.0	
Number Packets					1
Operation: EncodeHKPCDUDeploymer					
PUS Descriptor	128	128	48.0	20.0	
Number Packets					1
Operation: EncodePFStatus					
PUS Descriptor	3	25	234.0	20.0	
Number Packets					1
Operation: EncodePLStatus					
PUS Descriptor	3	25	61.0	20.0	
Number Packets					1
Operation: EncodeDIAGPCDUMonitori					
PUS Descriptor	128	128	42.0	20.0	
Number Packets					1
Operation: EncodeSTRHKHealthStatus					
PUS Descriptor	3	25	140.0	20.0	
Number Packets					1

*SMU_TC RF Link Configuration Table

- RF link
  - RF link descriptor
    - Upload Occupation: 87.5%
    - Download Occupation: 100%
    - Total Upload Rate: 64,000 bps
    - Total Download Rate: 64,000 bps

SMU_TM RF Link Configuration Table

- RF link
  - RF link descriptor
    - Upload Occupation: 100%
    - Download Occupation: 85%
    - Total Upload Rate: 1,000,000 bps
    - Total Download Rate: 1,000,000 bps

SENTINEL 3: OPERATION DESCRIPTORS (1553)

	S/C Mode	Type [S/A]	Freq./MIAT [Hz]	Packet Standa	Minor Frame	Slot	RT Sub-Address
MIL STD 1553 BC Dock: BC1553BDo							
Operation: SetDORISAttitude	Mode Normal	SYNCHRONOUS	1.0				
Packet Standard				PUS			
1553 Communication Profile							
Minor Frame/Slot					1	1	10
Minor Frame/Slot					2	1	10
Operation: SetDORISTime	Mode Normal	SYNCHRONOUS	1.0				
Packet Standard				PUS			
1553 Communication Profile							
Minor Frame/Slot					1	2	14

SMU 1553 Bus Controller Configura

- MIL_STD_1553B BC Dock
  - MIL STD 1553B BC Descriptor
    - BC Start Time: 21 us
    - BC Stop Time: 19 us
    - BC Schedule List Time: 55 us

*STR 1553 Remote Terminal PUS Packets Descriptor

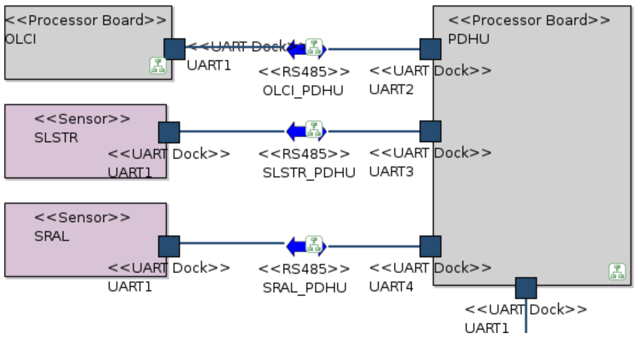
	Service Type	Sub-Service Type	Data Field [Byte]	Overhead [Byte]	Nº Packets (Optional)
MIL STD 1553 RT Dock: RT1553					
Operation: GetSTRStatus1					
PUS Descriptor	1	1	24.0	20.0	
Number Packets					1
Operation: GetSTRStatus2					
PUS Descriptor	1	1	64.0	20.0	
Number Packets					1
Operation: GetSTRStatus3					
PUS Descriptor	1	1	18.0	20.0	
Number Packets					1
Operation: GetSTRATM1					
PUS Descriptor	1	1	64.0	20.0	
Number Packets					1
Operation: GetSTRATM2					
PUS Descriptor	1	1	64.0	20.0	
Number Packets					1
Operation: GetSTRATM3					
PUS Descriptor	1	1	64.0	20.0	
Number Packets					1
Operation: GetSTRATM4					
PUS Descriptor	1	1	64.0	20.0	
Number Packets					1

SMU Bus 1553 Configuration Table

- MIL STD 1553B Bus
  - MIL STD 1553B descriptor
    - Response Time (RT): 12 us
    - Inter-Message Gap Time (IMG): 4 us
    - Command Word Transmission Time (CWT): 20 us
    - Status Word Transmission Time (SWT): 20 us
    - Data Word Transmission Time (DWT): 16 us
    - Maximum Throughput: 1,000,000 bps
    - Bus Maximum Margin: 50%
    - Major Frame (only needed for fine-grained bus analysis):
    - Minor Frame (only needed for fine-grained bus analysis):

SENTINEL 3: OPERATION DESCRIPTORS (UART)

	S/C Mode	Type [S/A]	Freq./MIAT [Hz]	Packet Standard
UART Dock: UART1				
Operation: GetOLCINormalData	Mode Normal	SYNCHRONOUS	22.7272	
Packet Standard				PUS
Operation: GetOLCICalibrationData	Mode Normal	SYNCHRONOUS	22.7272	
Packet Standard				PUS
Event: AckEvent	Mode Normal	ASYNCHRONOUS	22.727274	
Packet Standard				PUS



	Service Type	Sub-Service Type	Data Field [Byte]	Overhead [Byte]	Nº Packets
UART Dock: UART1					
Operation: GetOLCINormalData					
PUS Descriptor	1	1	33582.0	20.0	
Number Packets					5
Operation: GetOLCICalibrationData					
PUS Descriptor	1	1	35490.0	20.0	
Number Packets					10
Event: AckEvent					
PUS Descriptor	1	1	2.0	20.0	
Number Packets					1

PDHU-SRAL RS232/RS422/RS485 Config

- RS-485
  - RS-485 Descriptor
    - Data Latency: 1.02 ns
    - Maximum Throughput: 50 Mbps
    - Maximum Load Margin: 50%