Final Presentation

Single Board Computer Core Phase 1

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RUAG Space at a Glance

- Leading European space product supplier to the industry
- Acquisition of Saab Space and Austrian Aerospace (2008), Oerlikon Space (2009)
- Seven sites in three countries (Switzerland, Sweden, Austria)
- US office in Denver, Colorado
- 1150 employees (2013)
- Total revenues (2013): 243 M€
- Headquarters: Zurich (CH)
- This activity carried out by RUAG Space AB in Gothenburg, Sweden

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RUAG Space AB, Sweden - RSE

Headquarters and center for Computer systems, Antennas and Microwave Electronics: Göteborg, Sweden

Mechanical systems
Linköping operations, Sweden

2013:	
Sales:	750 MSEK, 87 MEuro, 115 MUSD
No of employees:	377

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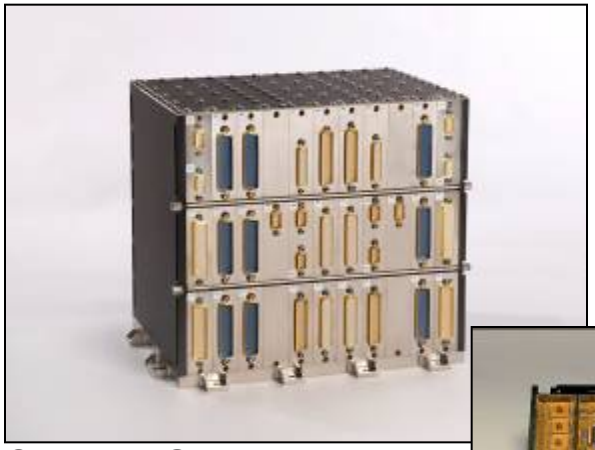
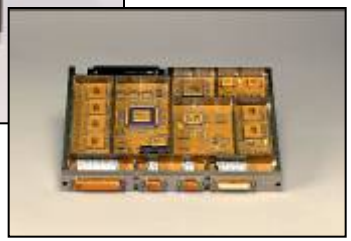
RSE Product Areas





Computer Systems

Adapters and separation systems

Satellite Structures

Antennas

Frequency Converters & Receivers

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Why Single Board Computer Core?

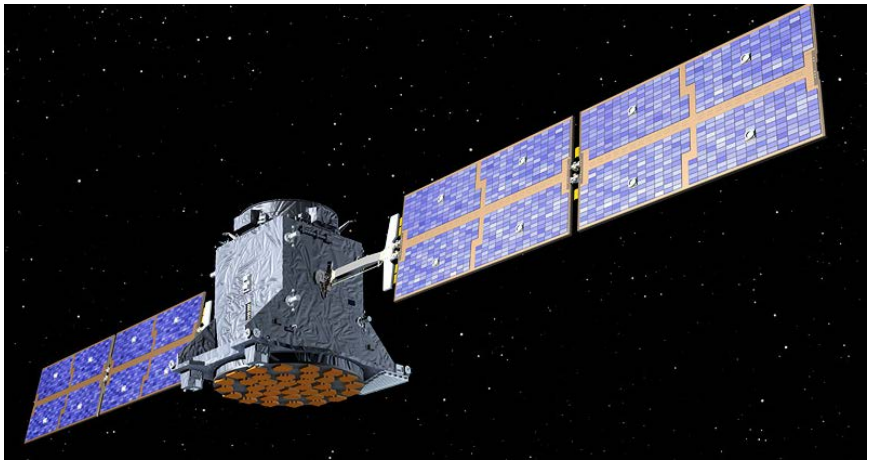
- RUAG is a major supplier of On-Board Computers (OBCs) and Spacecraft Management units (SMUs)
- The next generation OBC needs to have
  - Reduced Cost
  - Reduced Weight & Volume
  - Reduced Power Consumption
  - New Functionality

Why Single Board Computer Core?

- SBCC (Single Board Computer Core) is a major stepping stone for the evolution of the OBC and SMU products
- The SBCC will integrate all functions and interfaces needed for an OBC or SMU core on a single board
- Large Instrument Control Units will also benefit from SBCC
- SMU is an OBC + I/O boards. SBCC is focused on improving the OBC, and SMU core

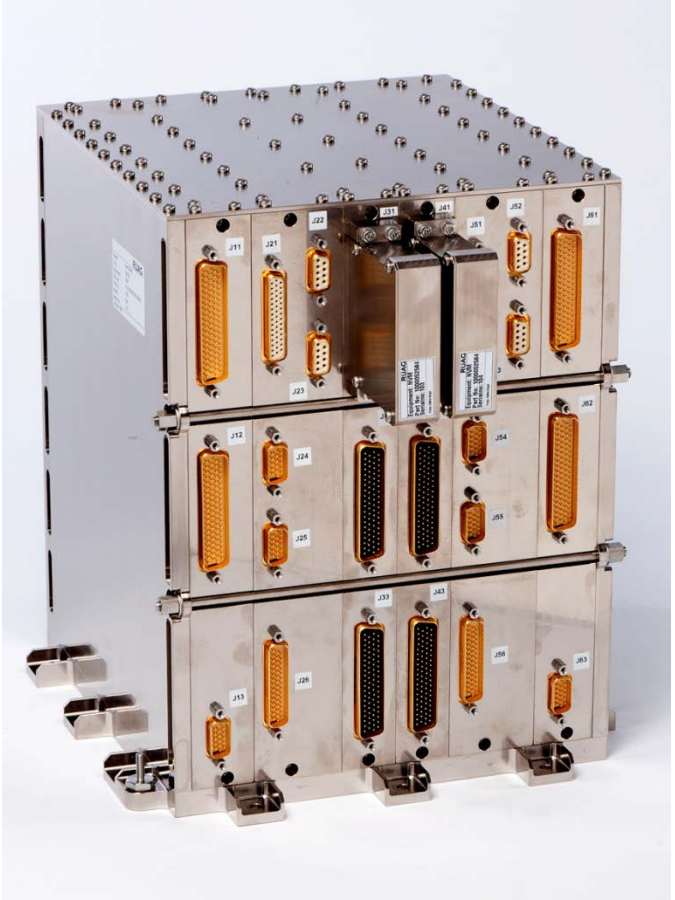
SBCC Target Missions

- Future ESA constellation, earth observation & science missions
  - Juice, Plato, L2, EO8, Mars Explorer missions, next generation Galileo…
- Future commercial satellites
- Emerging markets
  - Non-European Programmes
- Synergies with next generation launcher computers



Current OBC Concept

- Two digital boards per redundant OBC half
- One TTRM Board
  - Telemetry (TM), Telecommand (TC)
  - Reconfiguration
  - Mass Memory (Small)
  - Two ASICs: CROME and HAMSTER
- One PM (Processing Module) Board
  - Processing
  - Control interfaces: MIL-STD-1553, SpaceWire, UART…
  - One ASIC: COLE (LEON 2 with I/O controllers)



SBCC OBC Concept

- One digital board per redundant half
- Combines the functionality of the TTRM and PM boards
  - A single System-on-a-Chip ASIC: CREOLE, including the functionality of the existing ASICs
- The move to a single board, with a new ASIC, has several advantages
  - Reduced Cost, due to fewer components to handle and reduced manufacturing cost
  - Reduced Weight & Volume, due to smaller chassis
  - Reduced Power Consumption, due to better ASIC process and increased integration
- Architecturally similar to the current OBC concept
- Software interface has been kept as intact and compatible as possible
- Possible to increase performance significantly by using an additional add-on processor.

SBCC Phase 1 Result

- The development of SBCC is divided into three phases
- Final result will be a validated CREOLE ASIC
- Result of SBCC Phase 1:
  - A CREOLE baseline design that contains vital functionality of the current generation OBC, targeted for flight
  - Low-Level Driver Software for the CREOLE with an interface similar to the current generation OBC & Boot Software for the CREOLE allowing autonomous start of an SBCC unit
  - A hardware prototype with all standard OBC interfaces and the CREOLE baseline design implemented in an FPGA
  - Basic functionality of the hardware prototype verified
  - A processor mezzanine board, providing an add-on optional high-speed processing function connected to the CREOLE

SBCC Phase 1 Functionality

- SBCC is based on the SAVOIR ASRA (Avionics System Reference Architecture) generic OBC specification
- Standard Interfaces:
  - MIL-STD-1553, SpaceWire, CAN, UART
  - CCSDS packet Telemetry and Telecommand
- Core functionality
  - LEON Processing
  - Reconfiguration & Essential Telecommand
  - Synchronization
  - Essential Telemetry
  - AES (Advanced Enryption Standard) Authentication Unit
  - Mass Memory
- Scalability
  - Add-on powerful processor or FPGA

Support for Powerful Add-on Processor, for those projects needing it

- Processor performance requirements expected to increase during the CREOLE lifetime
- Solution: An external processor connected to the integrated processor on the CREOLE to share the workload
- SBCC Phase 1 uses a Next Generation Microprocessor (NGMP) functional prototype as an additional processor
- Future high-end missions could potentially use future higher performance processors without replacing the CREOLE

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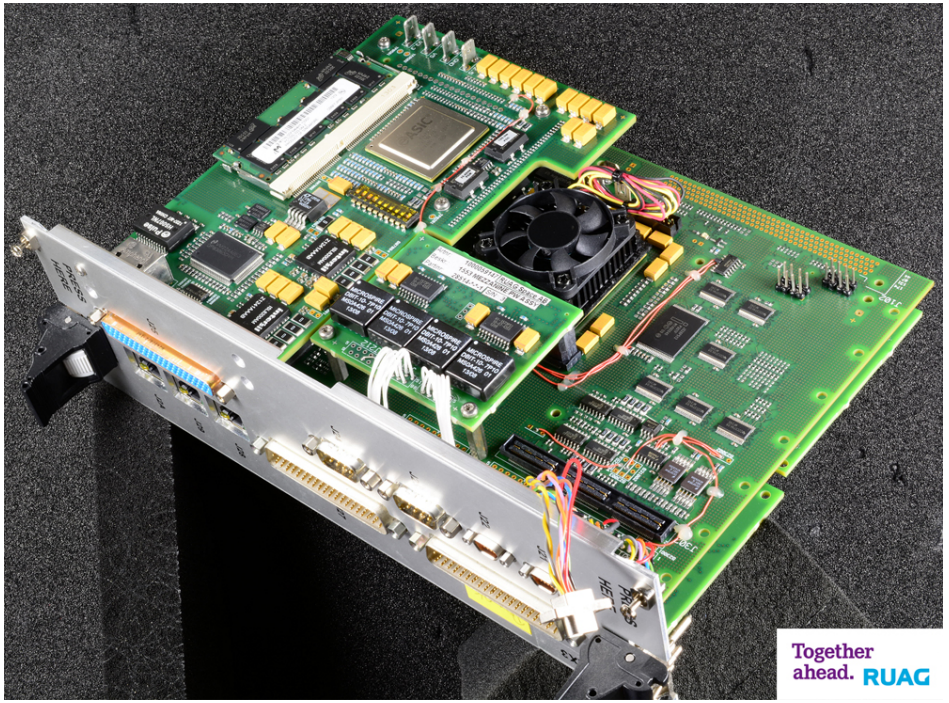
CREOLE Architecture

- A single System-on-a-Chip that contains blocks from
  - COLE – LEON2 with interfaces (UART, M1553, CAN, SpaceWire etc..)
  - CROME & HAMSTER – TTR functionality (Telemetry, Telecommand, Reconfiguration, Synchronization etc…)
  - Contains all vital functionality from the current generation OBC

- Changes compared to previous generation
  - Merge of memory buses, oscillators & reset management reduces external component requirement
- Driving architectural goal: SW compatibility
  - Maintaining SW as compatible as possible reduces cost for software redevelopment, both for RSE and customers

Multi Functional Core (MFC) Breadboard

- Prototype & Development board used for basic SBCC verification
- Standard OBC interfaces
  - MIL-STD-1553, CAN
  - SpaceWire, UART
  - TM, TC, Alarms
- NGFP Processor Mezzanine to verify high performance option
- Growth provisions
  - Ethernet – allows advanced debug support unit to be added
  - Mezzanine connectors - allows future functional growth without need for MFC breadboard redesign



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Multi Functional Core (MFC) Breadboard

- The MFC board contains all standard interfaces of an OBC
- Can be used as breadboard for current and next generation OBC, SMU and Instrument Control Unit computers, as well as for development activities
- Expansion possibilities allows it to be used for further development activities, and for customer specific tailorisations, without expensive hardware redesign
- The large FPGA makes it easy to develop new functionality but still maintain feature compatibility with the entire future ASIC
- Will be used for final validation of the CREOLE prior to ASIC tapeout

Summary

- RUAG Space has created a single digital board with the functionality of the current generation OBC
- Maintaining the software interface reduces cost for software adaptation
- SBCC Phase 1 provides a good base for the coming phases and the adaptable hardware development platform and CREOLE architecture is prepared for the addition of new functionality

- All development for SBCC Phase 1 was completed on schedule

- Waiting for Phase 2 to be started

Thank you for your attention!