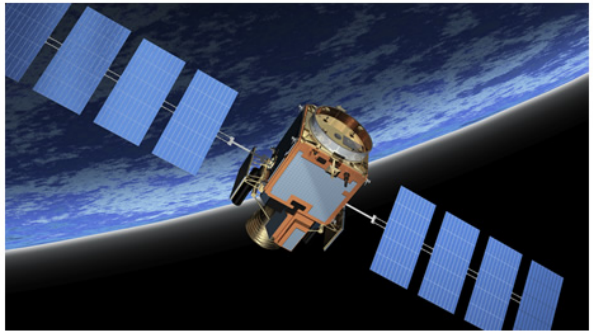
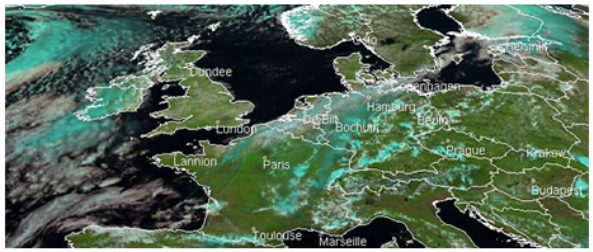
Dynamic Translation Based On-Board Processor Emulator QERx

Final Presentation

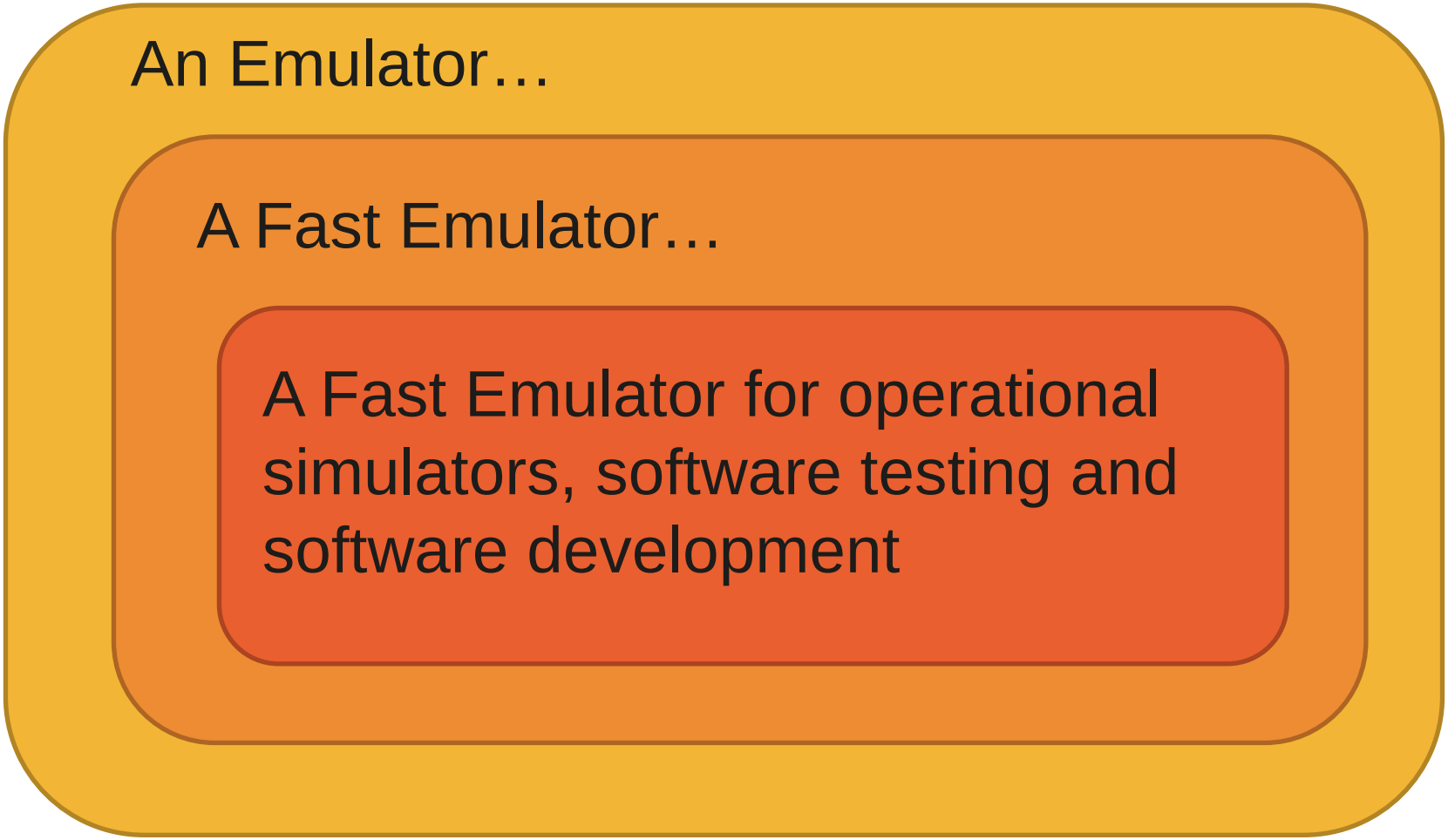
Daniel Townson

Wednesday, 21 May 2014





What is QERx



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Why Use QERx

- Performance
- Extensibility
- Practicality
- Validation

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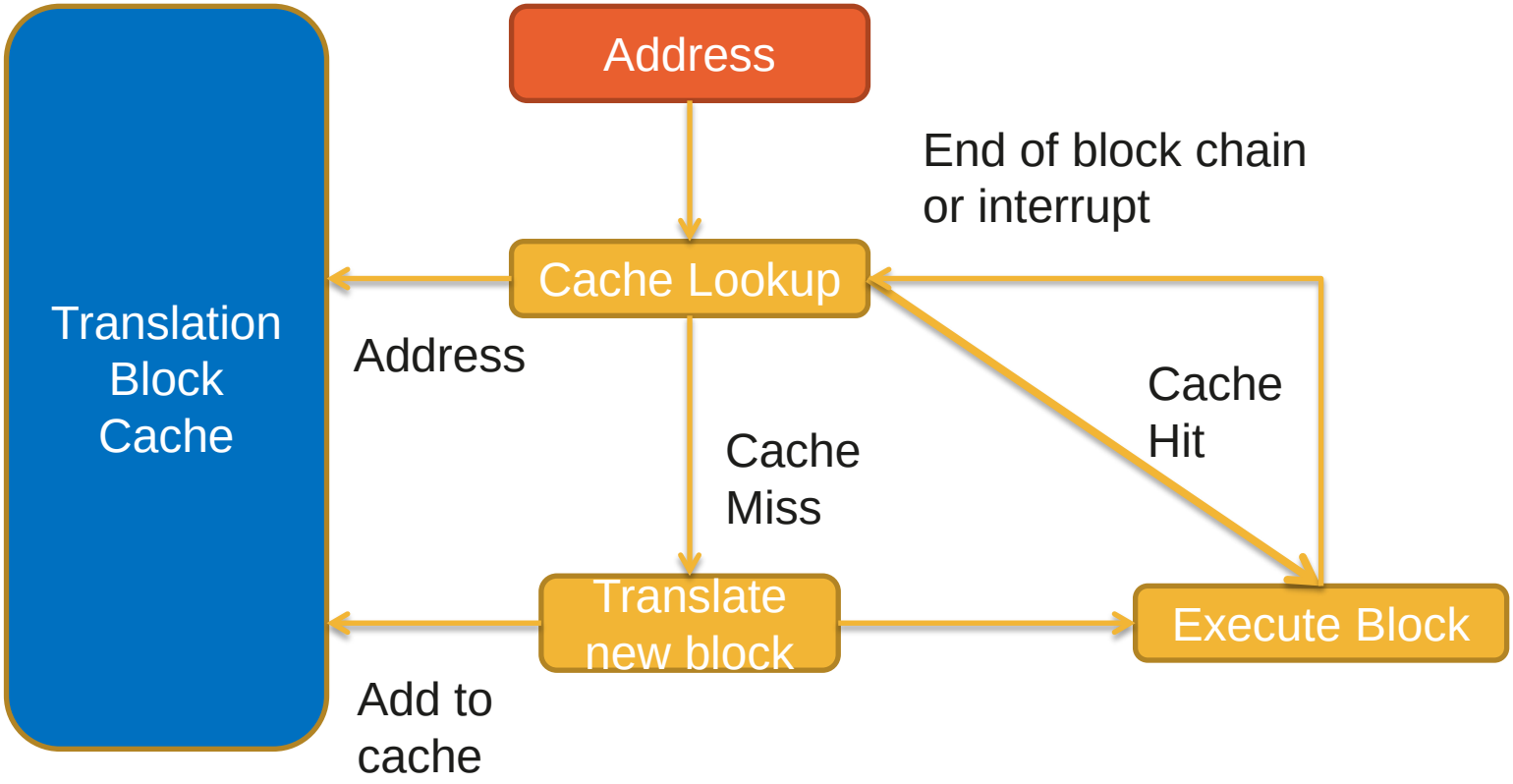
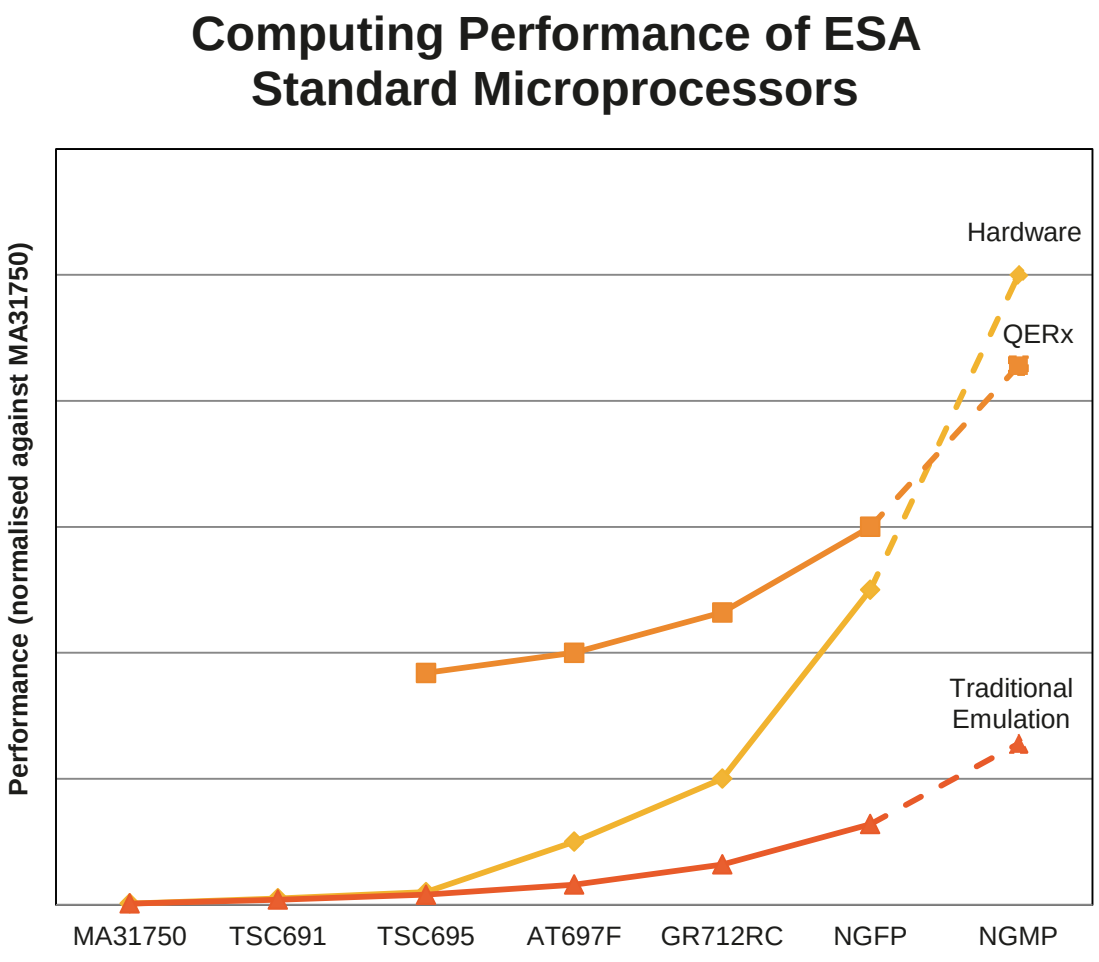
Performance



Performance



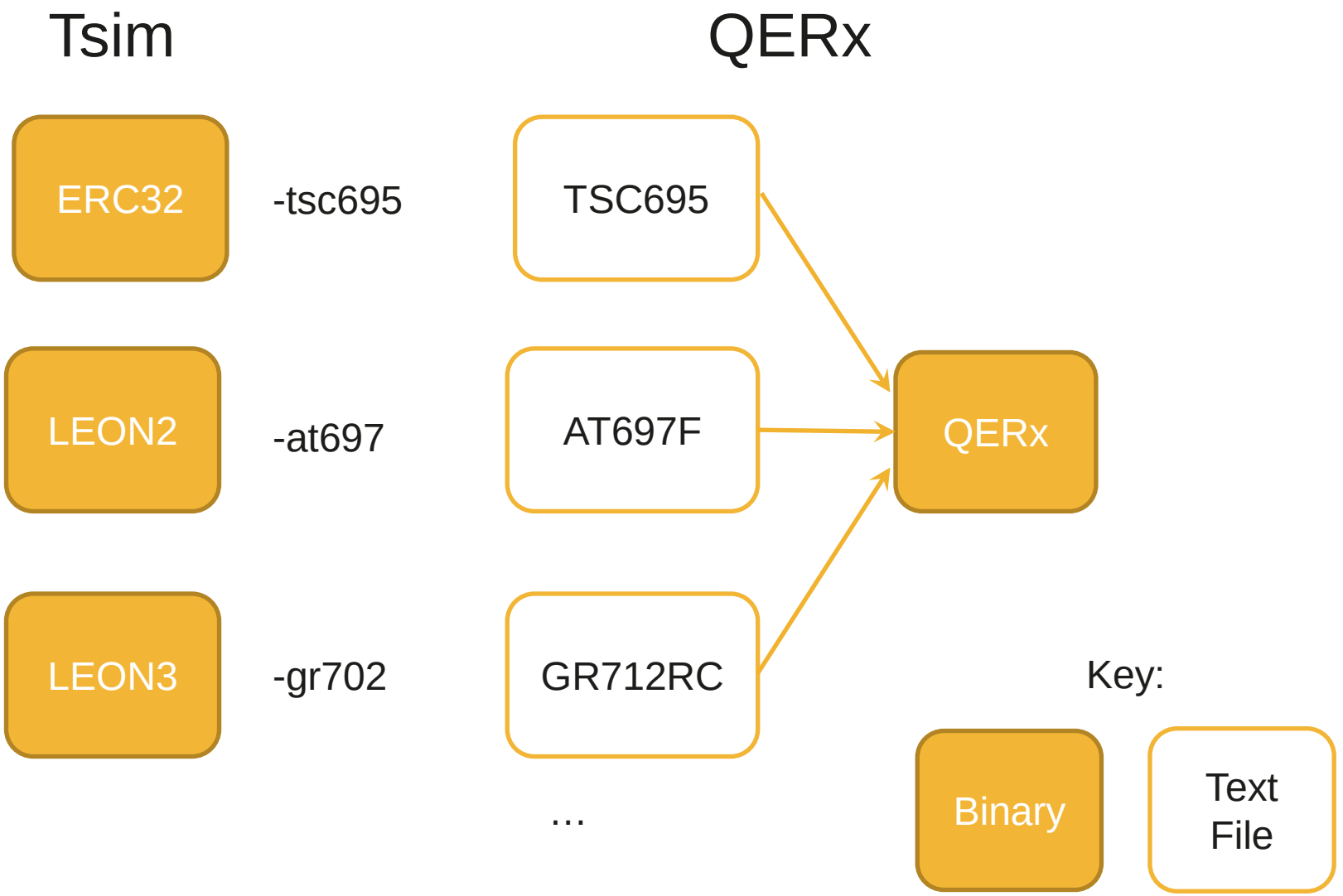
Past (ERC32)
Slow processors, emulation speed not a problem

Current (LEON2)
A gap starting to show between processor speed and traditional emulation

Near Future (LEON3)
Traditional emulation frustratingly slow

Medium Future (LEON4)
Traditional emulation unfeasible, architecture change required

Extensibility



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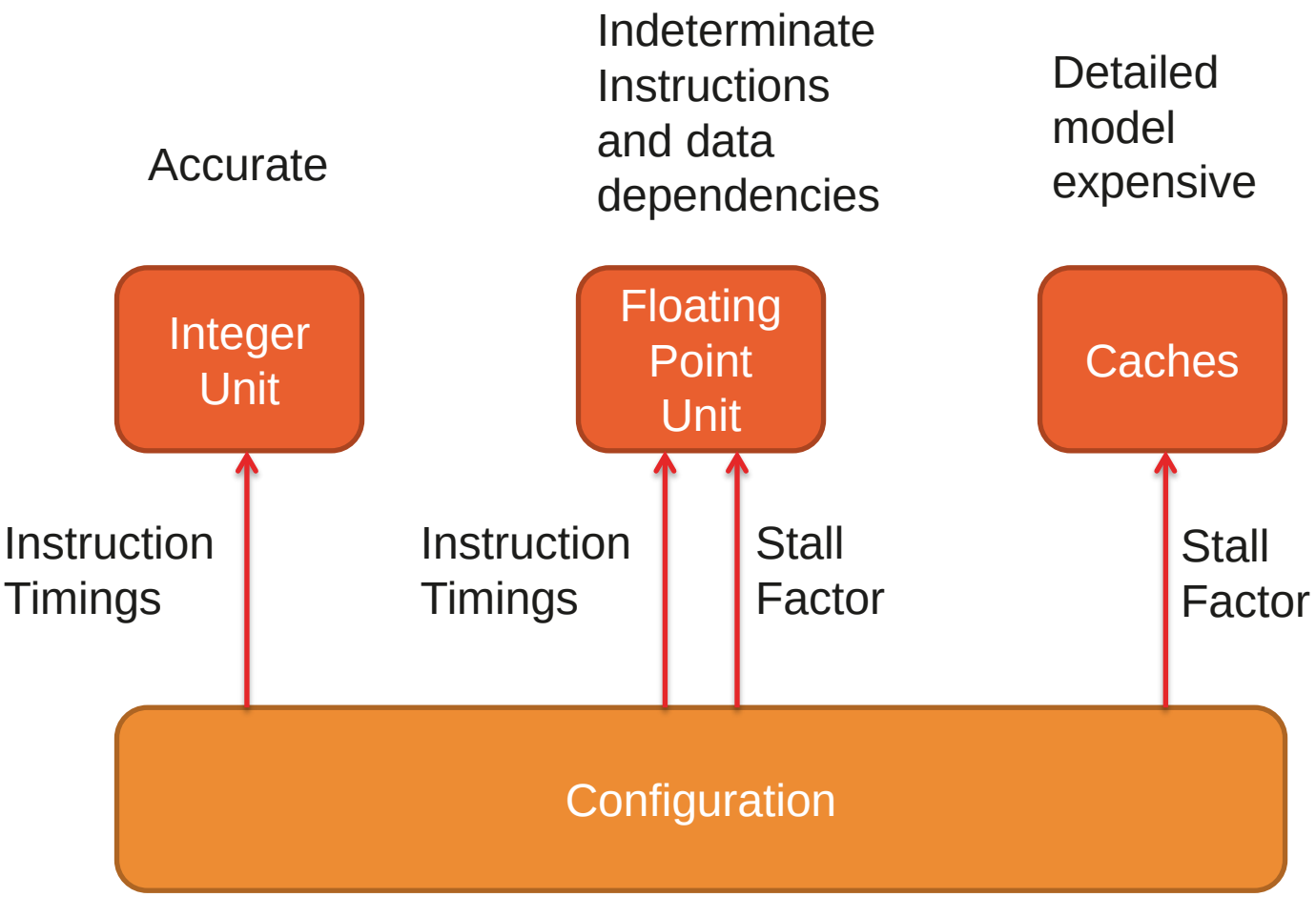
Accuracy



Configuration provides other details: clock speeds, cache details…

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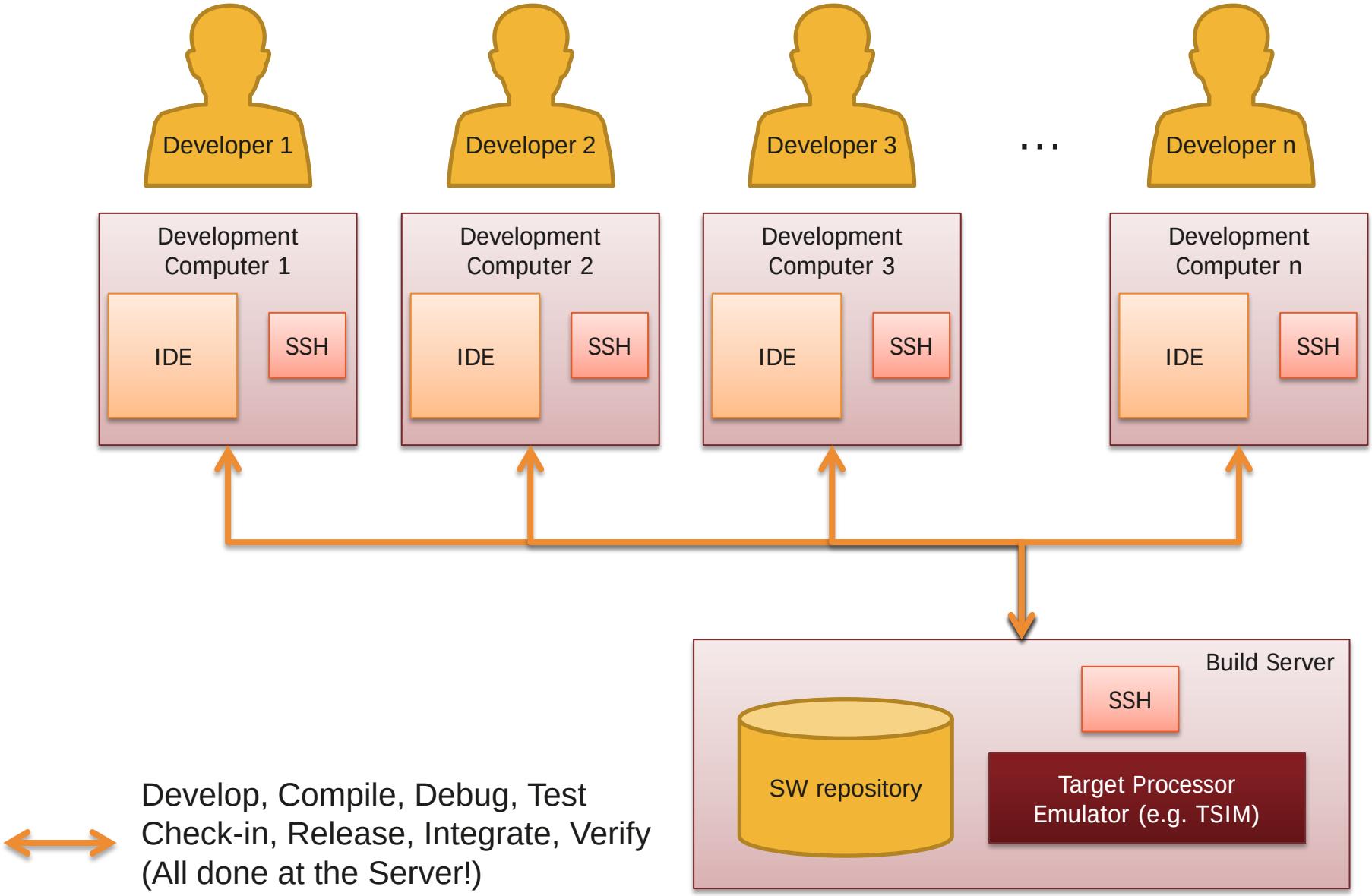
Practicality



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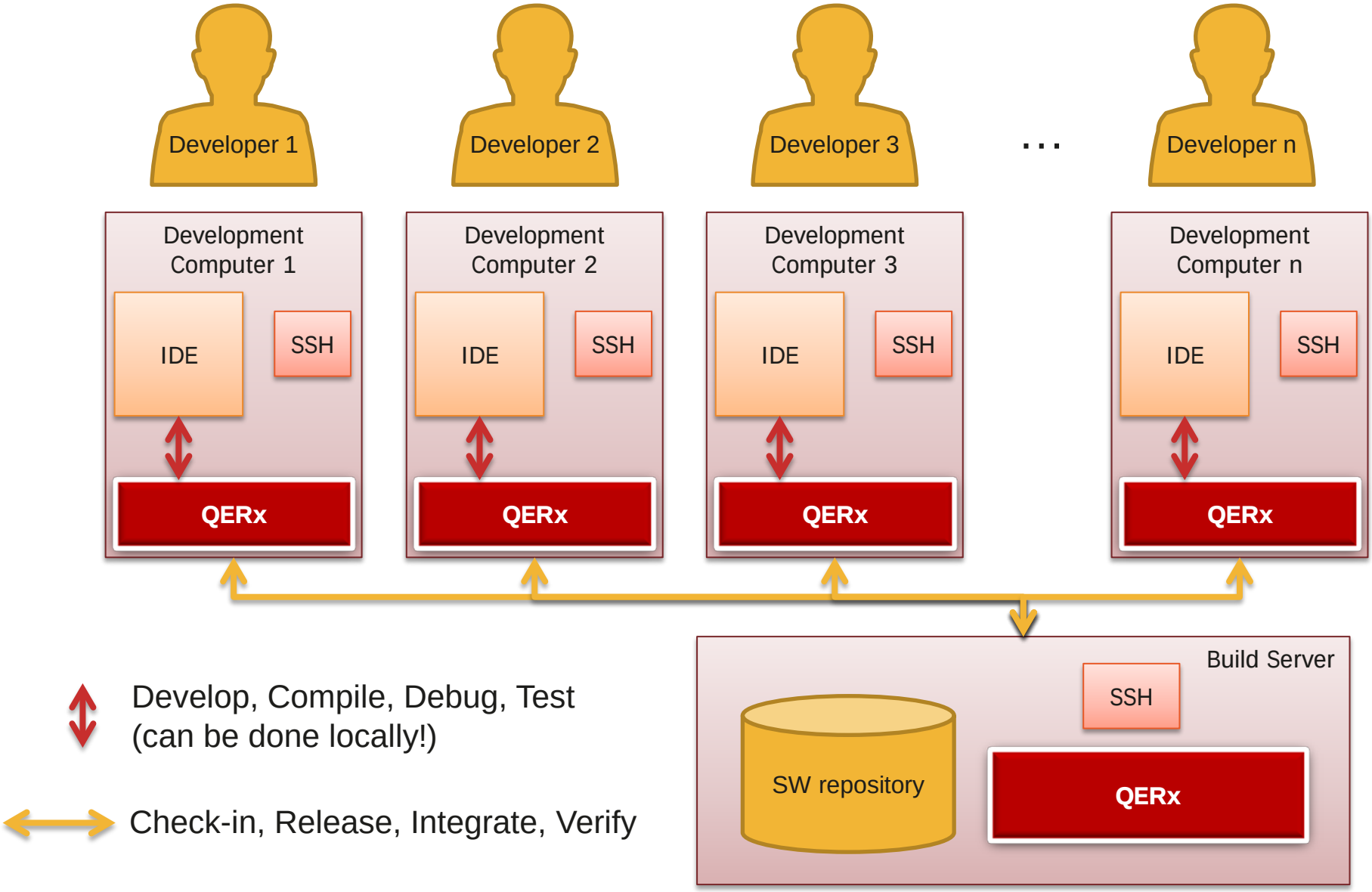
Practicality



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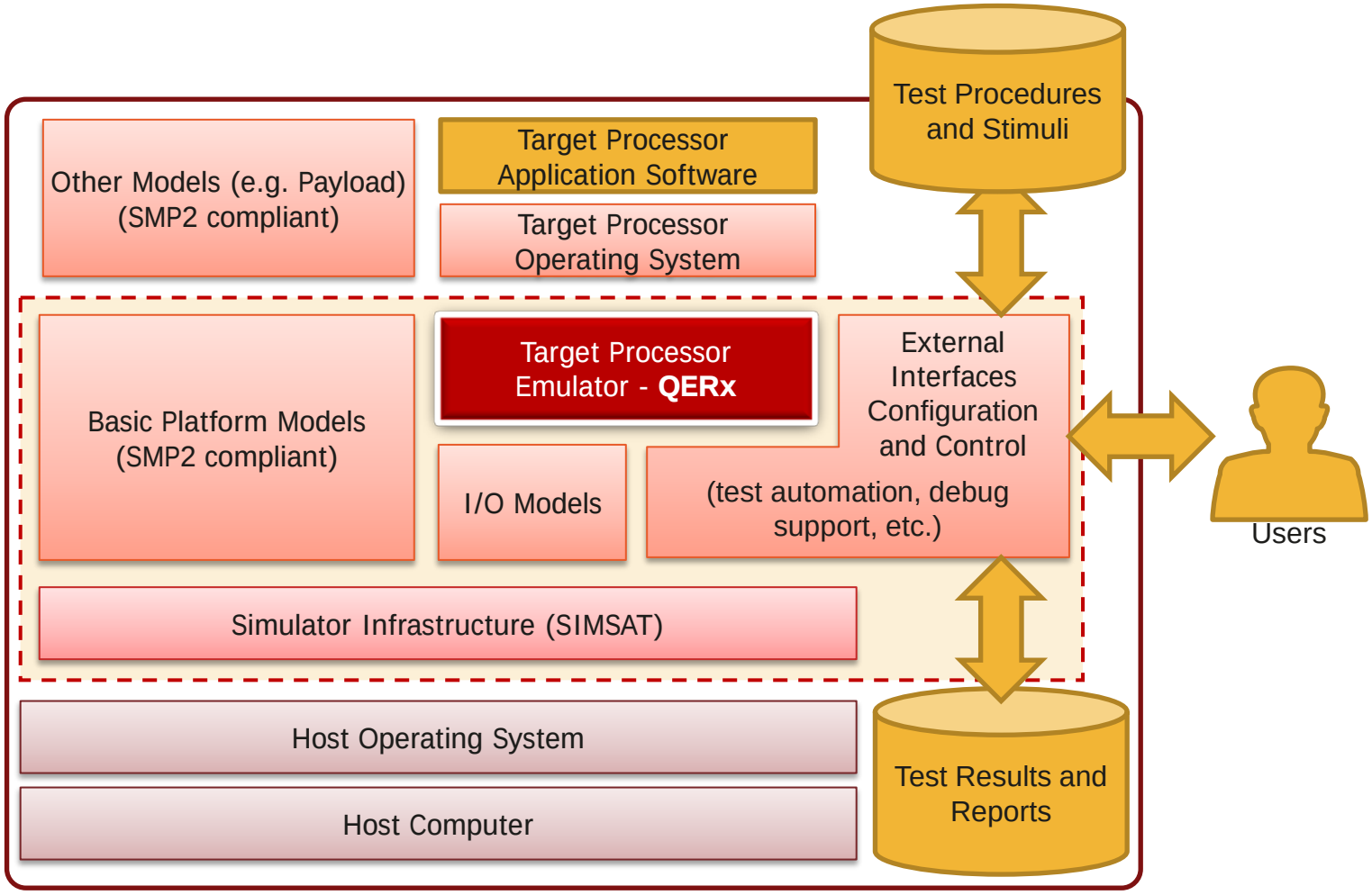
Software Validation Facilities – SVF



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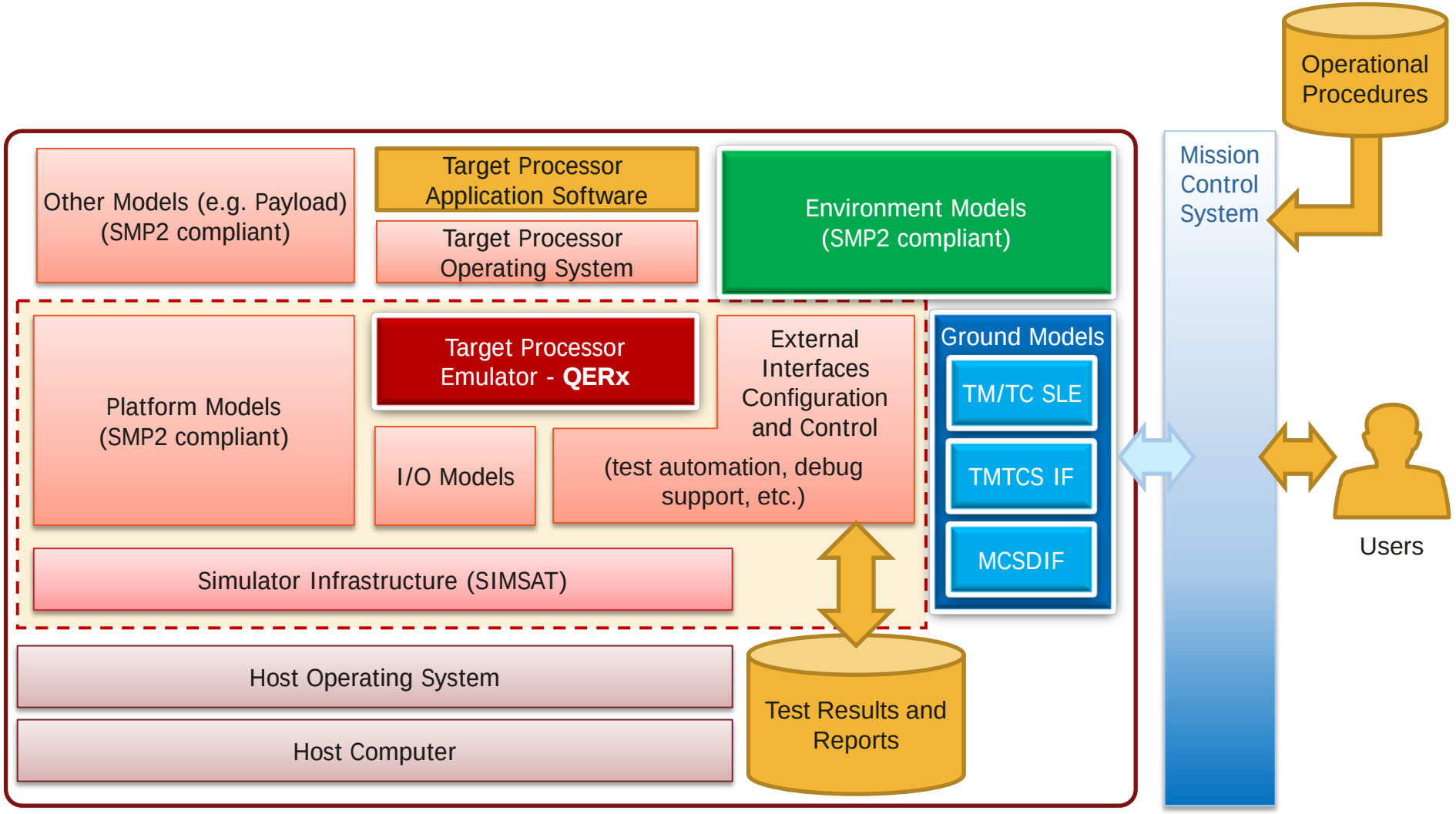
Operational Simulators



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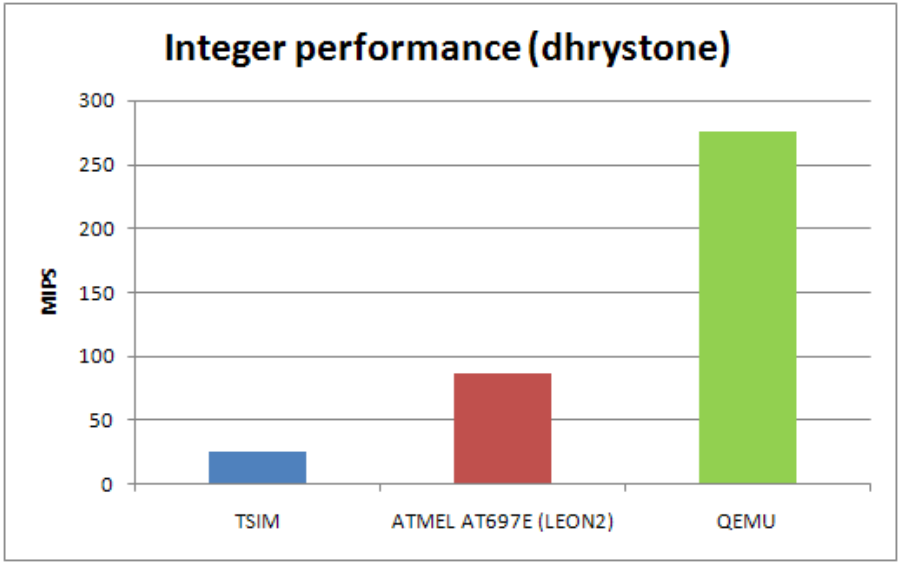
Background of QERx

- QEMU Dynamic Translation Emulator
  - » Open Source
  - » Supports many target processors including SPARC
  - » FAST
- But, why can't you just use QEMU:
  - » Complete machine emulation (not just a processor)
  - » Doesn't support ERC32
  - » Doesn't support LEON
  - » Virtual timers rely on host clock – no link to instructions executed
  - » Not available as a shared library
  - » No command driven interface



Intel Pentium 4 EM64T @ 3.6 GHz

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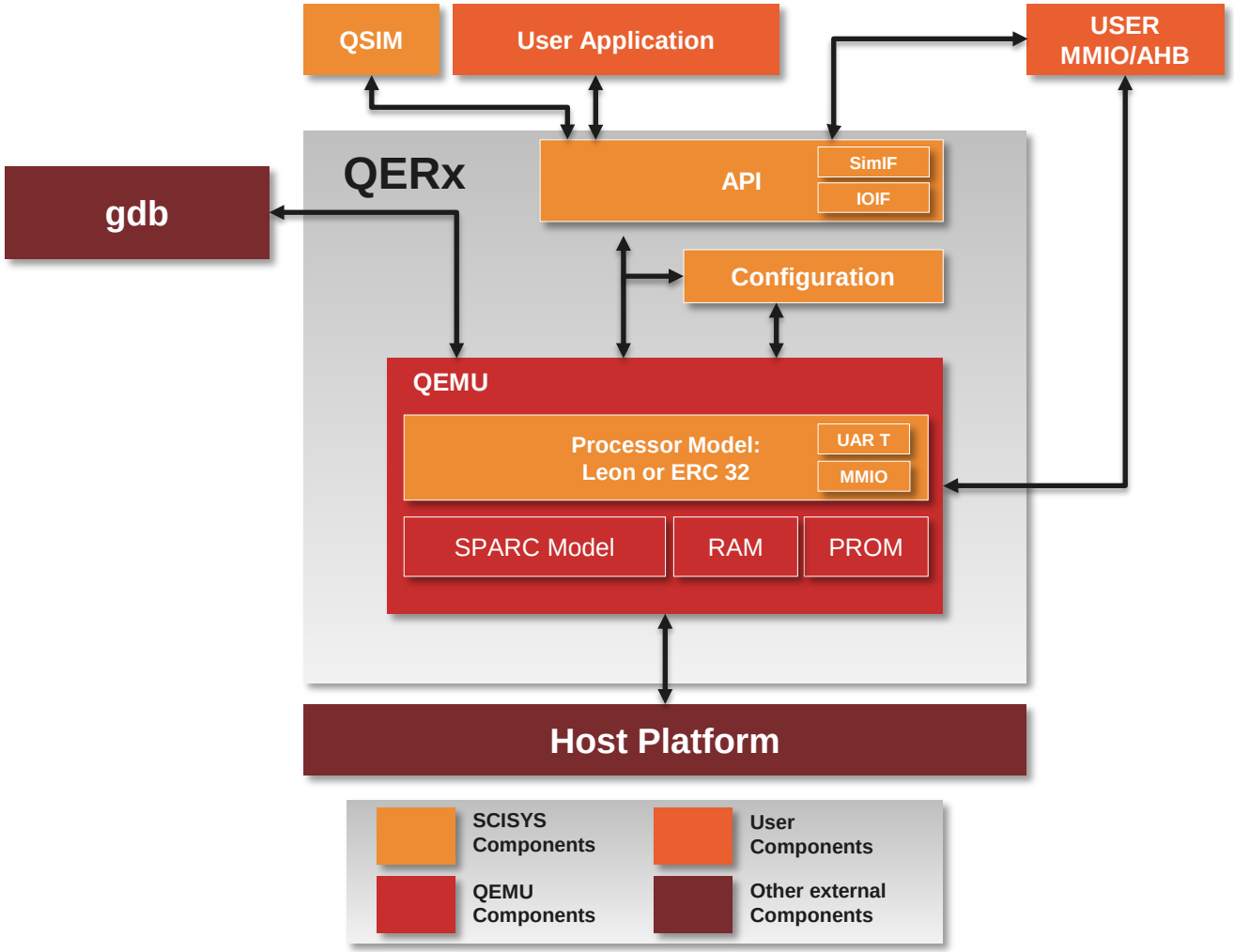
What is QERx

Overview of the QERx Architecture



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Current Status

Processor	SPARC	FPU	UARTs	AHB	Cores	MMU	Memory Protection
ERC32 (TSC695F)	v7	Soft or hard	2 Tx/Rx	N/A	1	N/A	2 units
LEON2 (AT697F)	v8	Soft or hard	2 Tx/Rx	✔	1	N/A	4 units
LEON3 (GR712RC)	v8e	Soft or hard	6 Tx/Rx	✔	2	✔	MMU

Key added features:

- LEON3 validation
- Multicore support
- Memory management unit and memory protection support
- Bidirectional UARTs
- Hard and soft FPU implementation
- An extensive set of commands and tools

Validation

QERx Functional Tests

SPARC v8 Compliance test

Gaia Operational Simulator (ERC32)

EarthCARE STF (LEON2)

LEON3 Study Software

Hardware Comparison (GR712RC)

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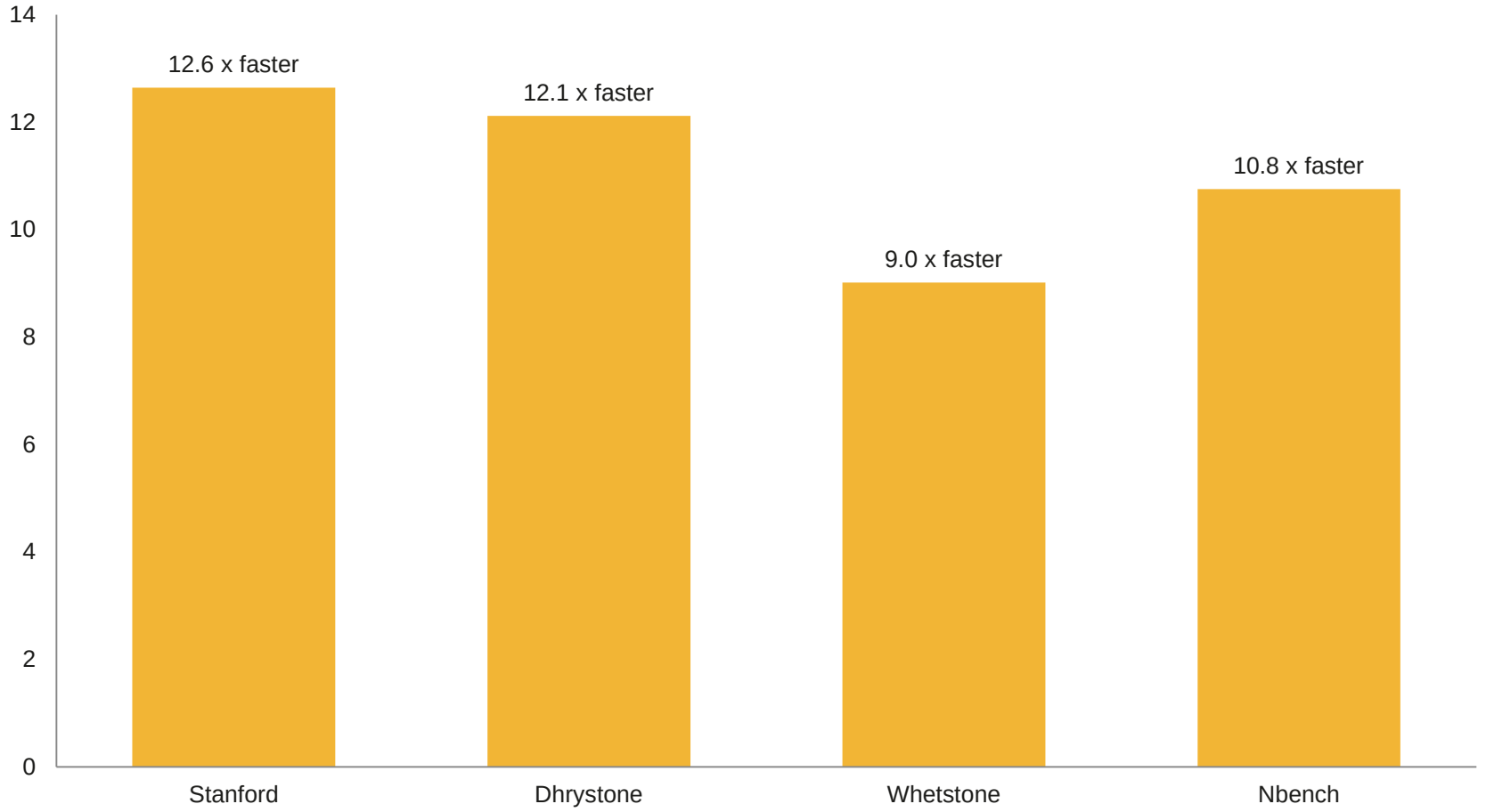
Performance

Benchmark	Iterations	Execution Time on Tsim (ms)	Execution Time on QERx (ms)
Stanford	1	2,445	225
Stanford	25	75,824	5,998
NBench	1	667,113	62,035
Dhrystone	400k	28,924	2,975
Dhrystone	1M	70,326	5,805
Whetstone	1	13,813	1,532

Both on 64-bit Intel Xeon E5507 @ 2.26 GHz

Performance

Performance improvement over Tsim



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Performance

Performance of Gaia Operational Simulator

	ESOC			QERx				% Improvement		
Breakpoint	Min *	Mean *	Max *	Min *	Mean *	Max *		Min	Mean	Max
IGM	2.86	3.16	3.36	3.2	3.56	3.71		12	13	10
TSM	2.46	2.67	2.88	2.68	2.88	3.09		9	8	7
NM	2.54	2.71	2.9	2.69	2.96	3.14		6	9	8

* Figures shows speed against real time

Intel Xeon E31245 @ 3.3 GHz
Launch Ready Gaia Operational Simulator

Highest AOCS modes:

IGM	Inertial Guidance Mode
TSM	Transition Mode
NM	Normal/Nominal Mode

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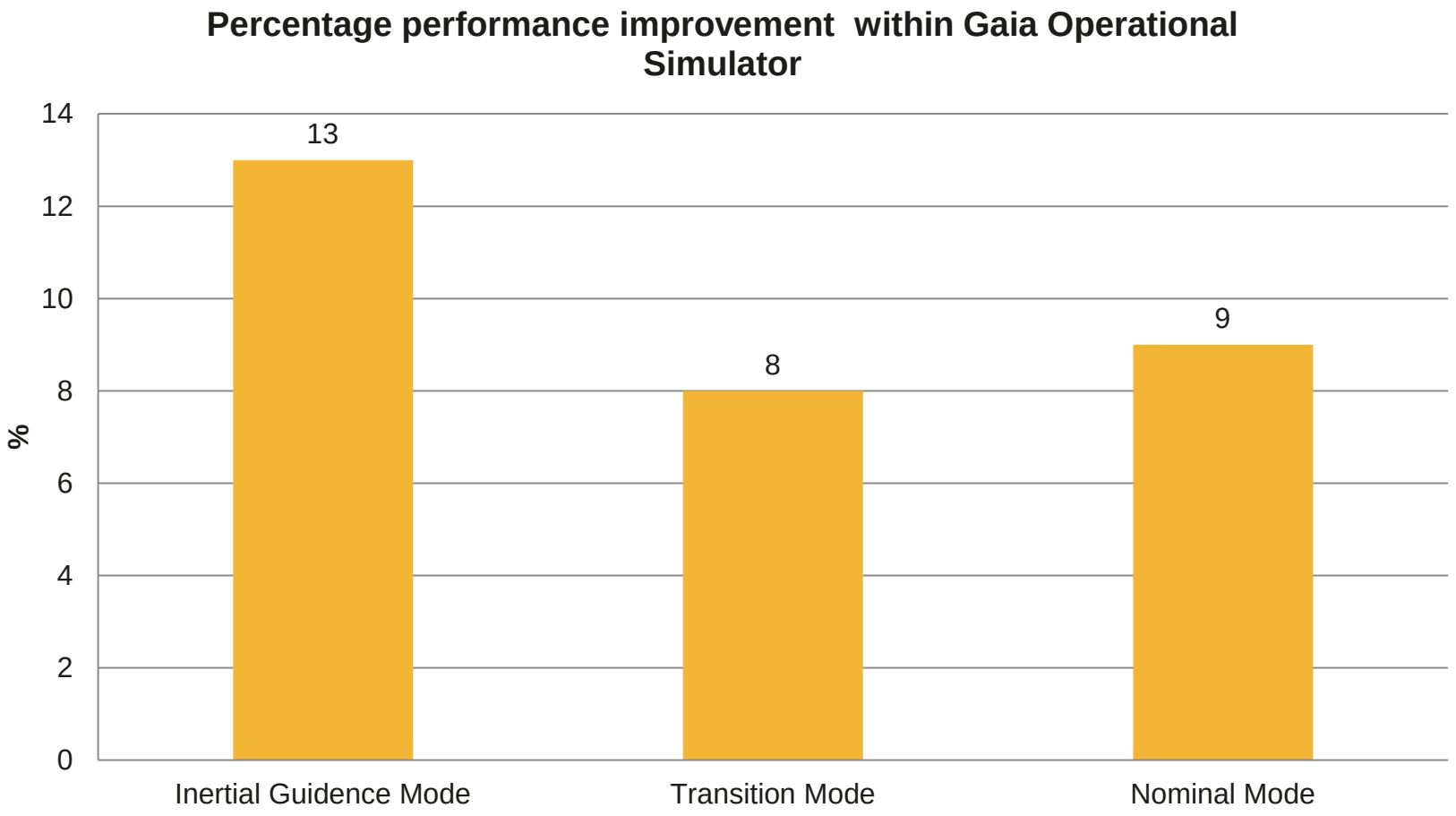
Performance



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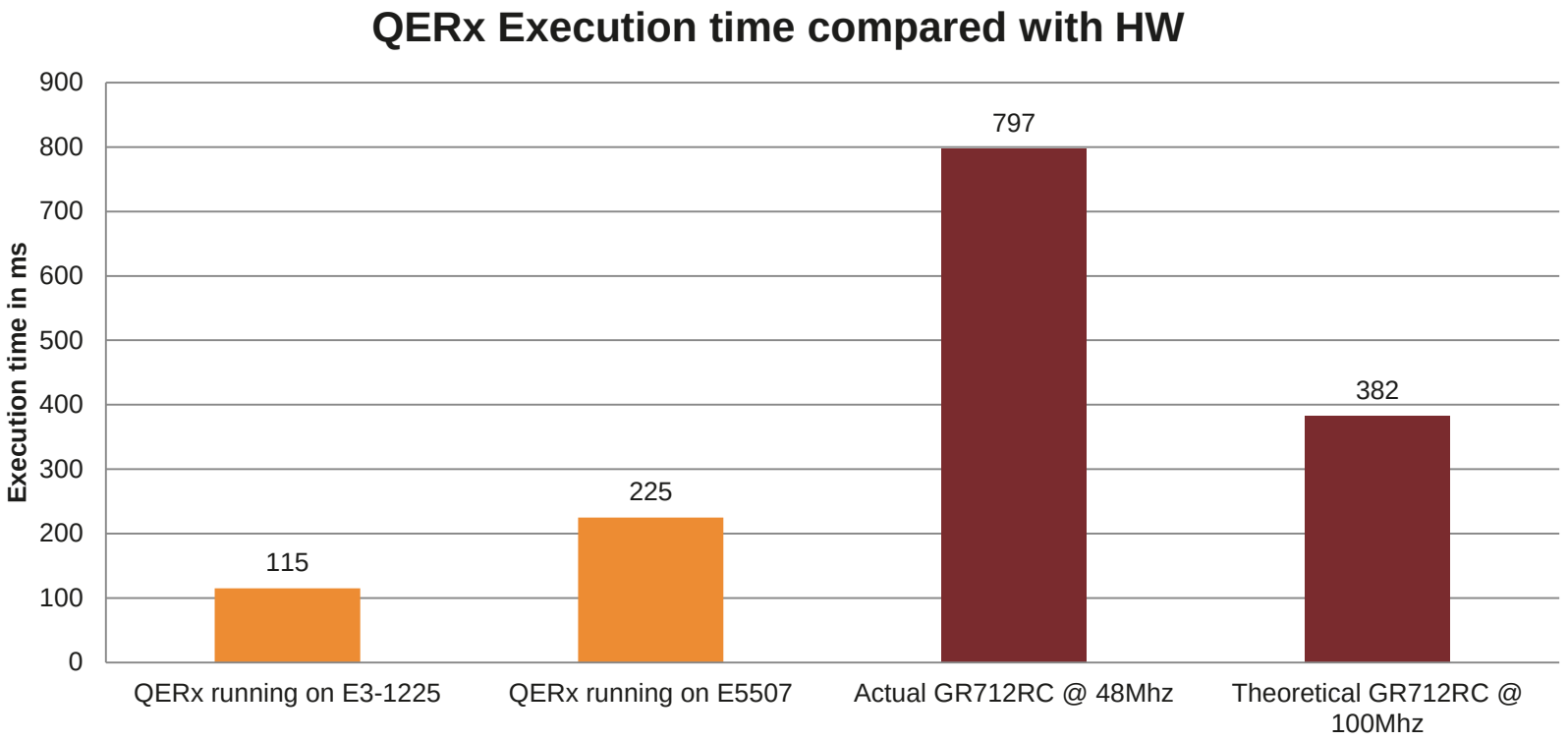
Performance



QERx running on E3-1225 (ms)	QERx running on E5507 (ms)	Actual GR712RC @ 48Mhz (ms)	Theoretical GR712RC @ 100Mhz (ms)
115	225	797	382

Up to 8 times faster than the hardware

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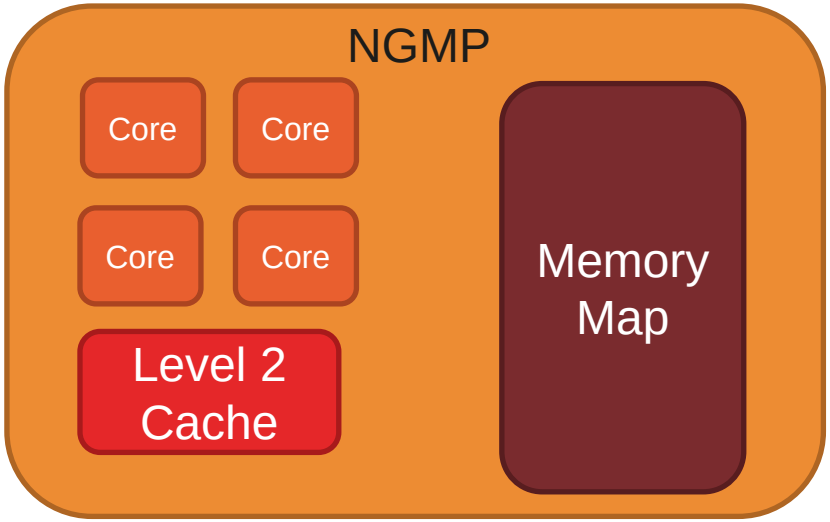
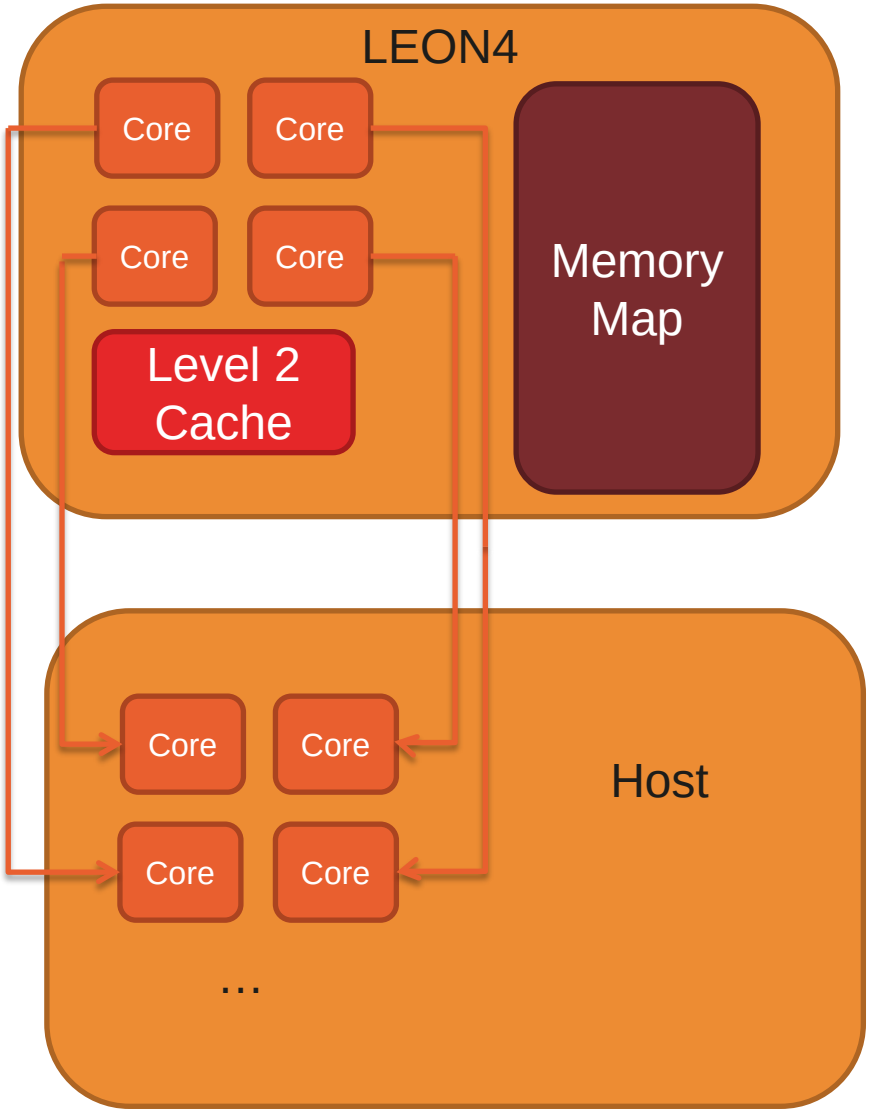
Future

LEON4



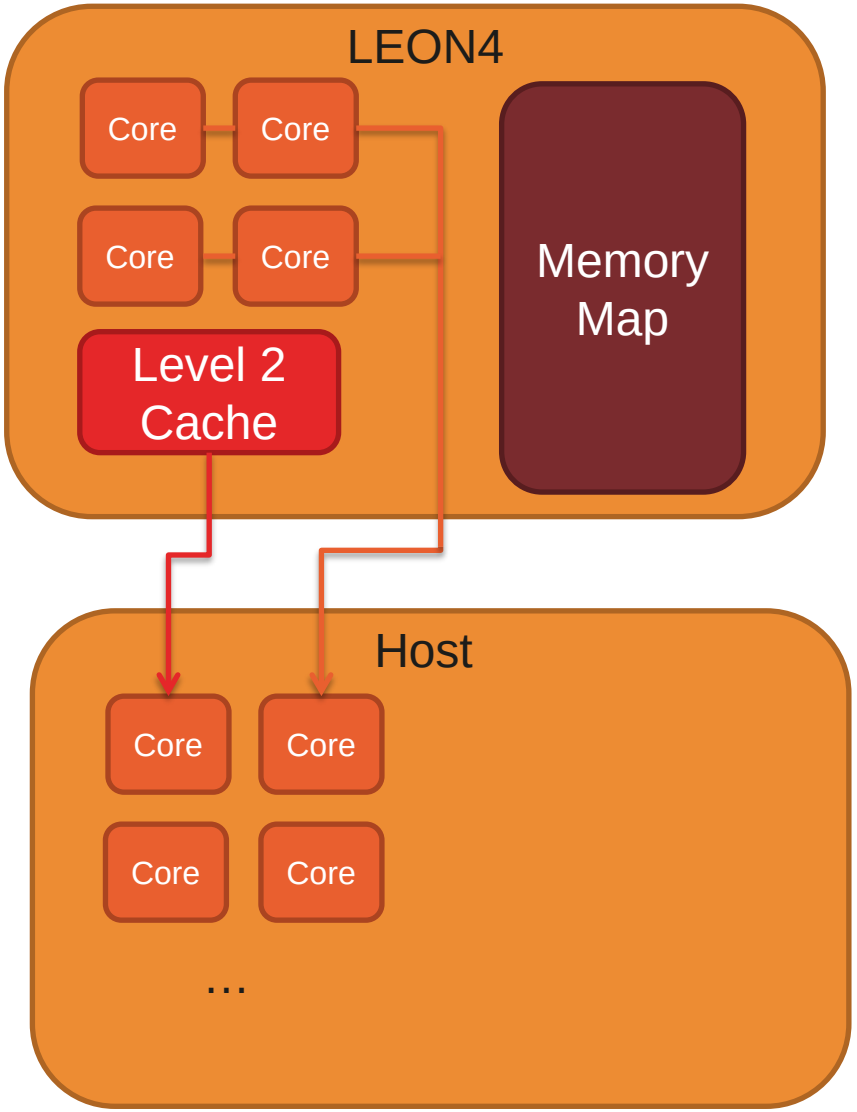
Future

Target cores
to host cores



Future

Functions onto individual cores



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Summary

- Performance
  - » Faster than real-time, up to 8 times (LEON3)
  - » 10 times faster than Tsim
  - » Significant performance improvement over the ESOC emulator within an Operational Simulator
- Extensibility
  - » Next Generation Processors
  - » Configurable to different chipsets
  - » Tuneable
- Practicality
  - » Large range of tools
  - » Simple and familiar interface
  - » Flexible and configurable
- Validation
  - » Validated against independent test suite
  - » Used in realistic environments
  - » Validated against hardware up to LEON3

Questions?

Product information sheet available

Bruno Carvalho
Business Development Manager
Space Division

SCISYS UK Ltd
Clothier Road, Bristol
BS4 5SS, UK

Direct: +44 1249 466 337
Mobile: +44 7584 349174

bruno.carvalho@scisys.co.uk
www.scisys.co.uk