OBC Simulator Architectures and Interfaces to System Test Benches (LeonSVF)

GSTP + StrIn + Lab investment activity progress presentation

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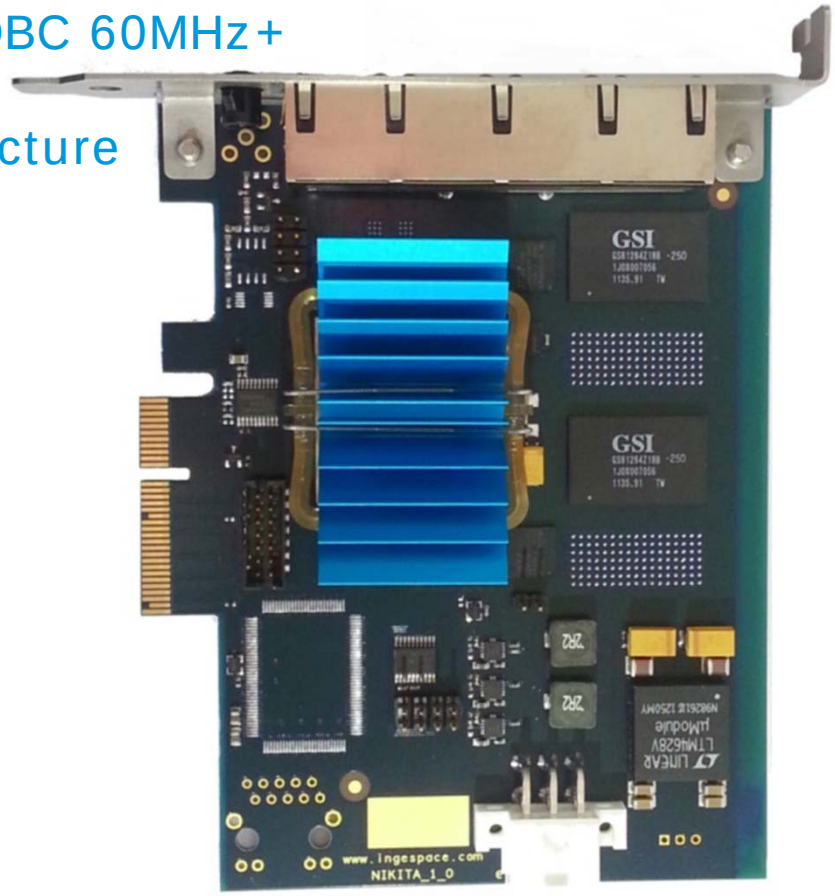
Prime: Astrium SAS Toulouse / Airbus
Consultant: Ingespace SARL (Toulouse)
Subco: Terma AS (Copenhagen)

Skipping to conclusions: Leon Emulation Board (LEB)

Do you need a Leon System on Chip emulator?

- 100% representative
- simulate in real time a S/C with OBC 60MHz+
- works in Eurosim, SimTG
- easy to integrate in your infrastructure
- easy to operate
- ...



Leon Emulation Board !

Skipping to conclusions: Leon Emulation Board (LEB)

Easy to tailor to another SoC

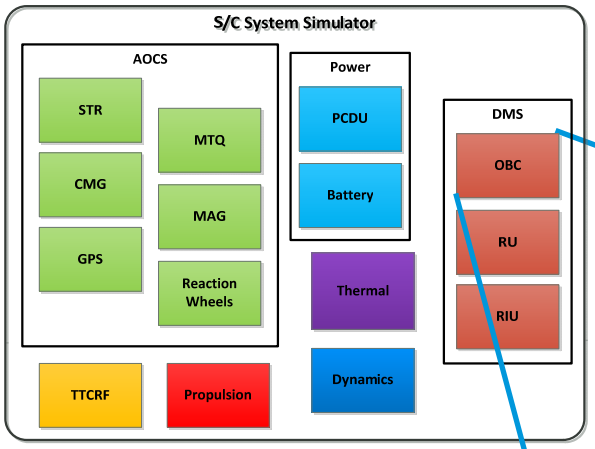
LEON2 configuration →	LEON3 configuration →	SCOC3-inspired configuration (extension of LEON3 config) →	Another SoC ????
- Leon2FT@100Mhz - GRFPU	- Leon3@100Mhz - GRFPU	- Leon3@100Mhz - GRFPU - SpW packets: Leon ←→ Sim SW - 2 Amba buses	Leon2FT? Leon3? ...
- 4+4MB Leon PROM/EEPROM - 16 MB Leon SRAM at 0 wait states - 64 MB SDRAM - 4+4 MB for fast simulation of I/O mapped memories - SW Simulation on I/O and AMBA bus (APB and AHB) - UART characters Leon ←→ Simulation SW - Monitor and control of PIO, reset and watchdog pins			
- Scheduler and Timed Events - GDB Server - Save and Restore of simulation contexts - API TSIM compliant (partly) plus extensions - Runs in Eurosim (Dutch Space) and in SimTG (Airbus DS)			

Agenda

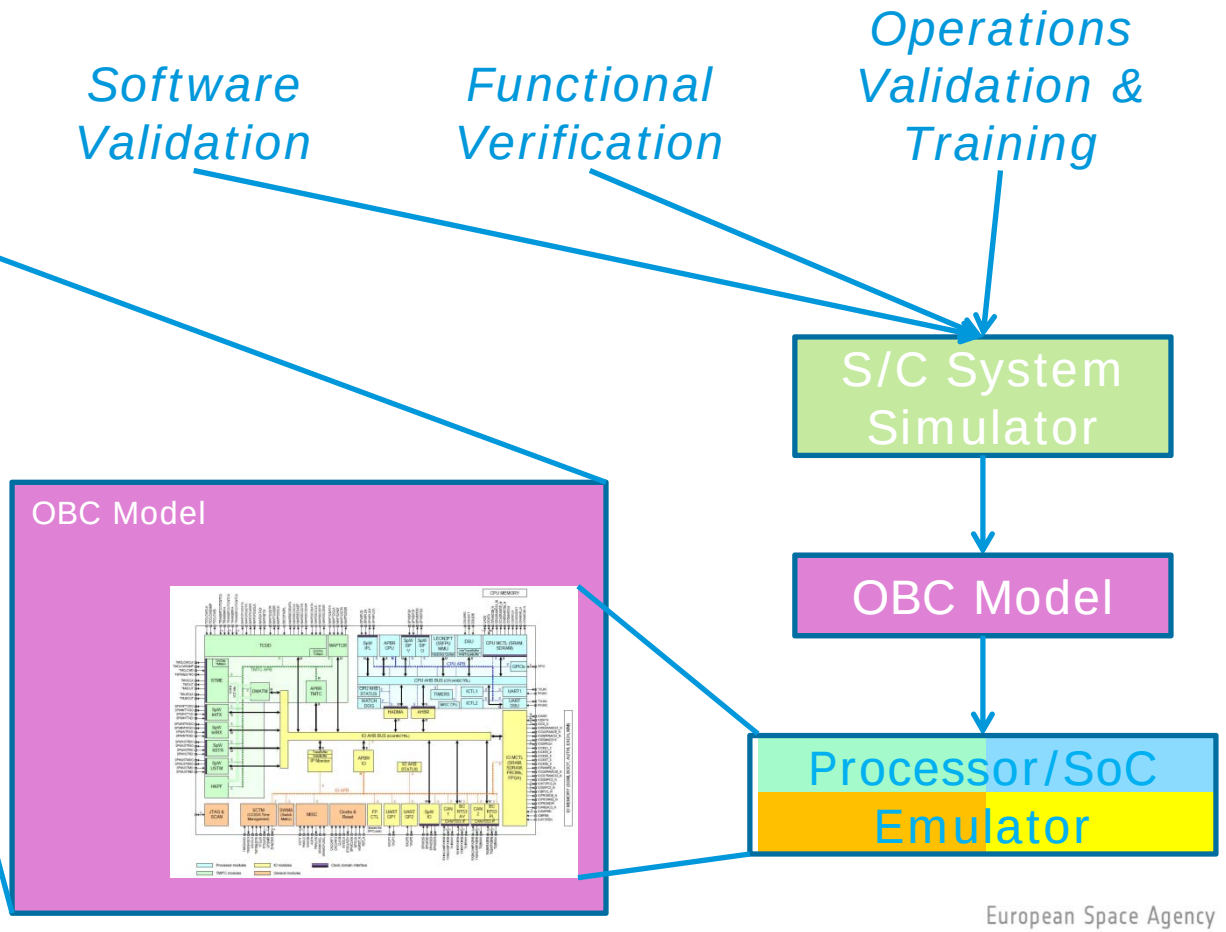
1. Context and goals of the project
    a. from CPU to SoC emulation with HW-in-the-loop
2. Work logic and status
3. Leon Emulation Board (LEB)
    a. Functions, Leon2FT/Leon3, Performance
    b. Future: multicore? DSU4?
4. HW/SW Co-engineering and the SysC/TLM SpW model
5. SOIS in system simulation
6. Conclusions

Context

When actual OBSW flight image and/or CPU instruction set are required



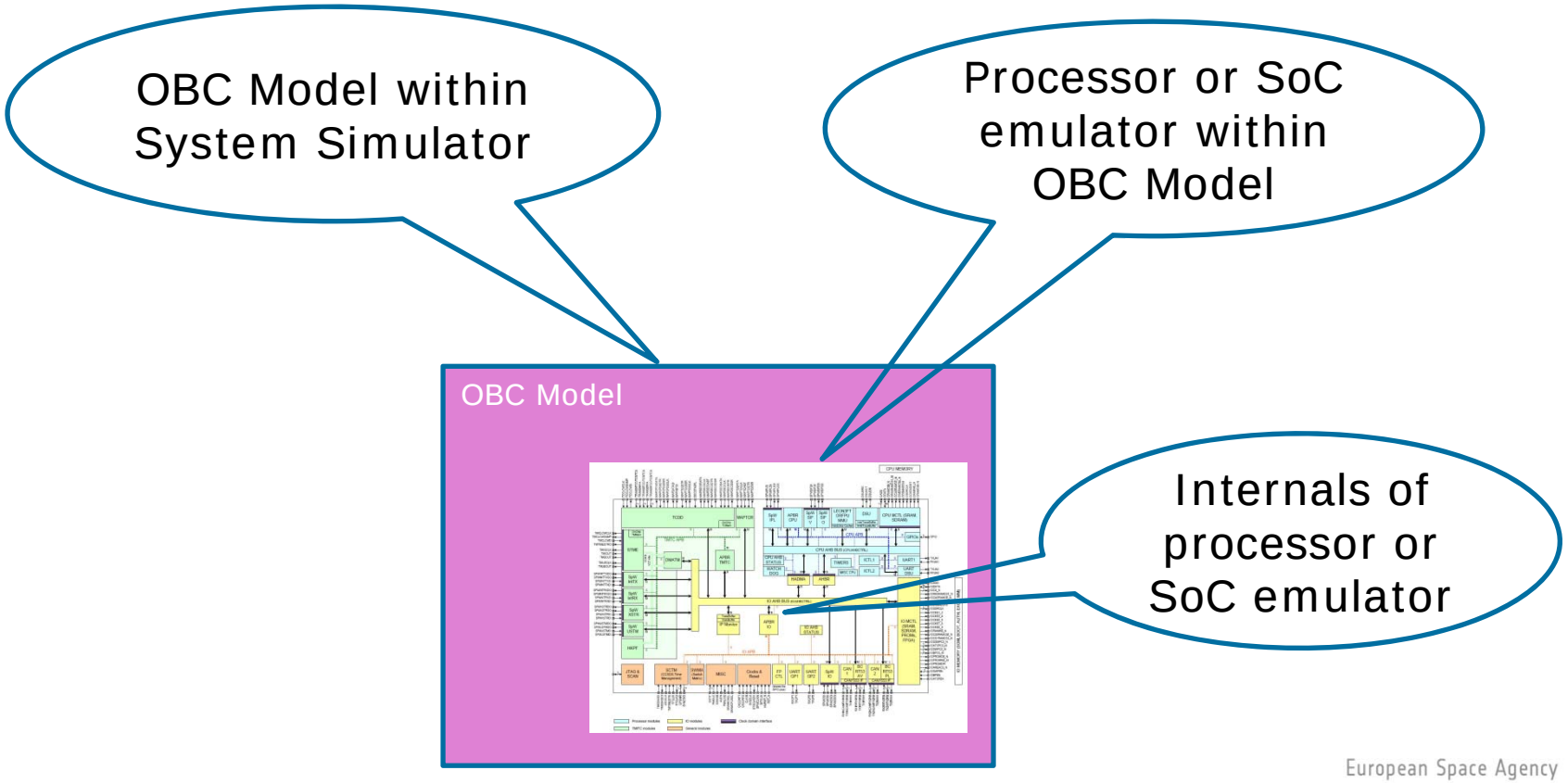
eg SPOT6 by Airbus DS



Context: the project

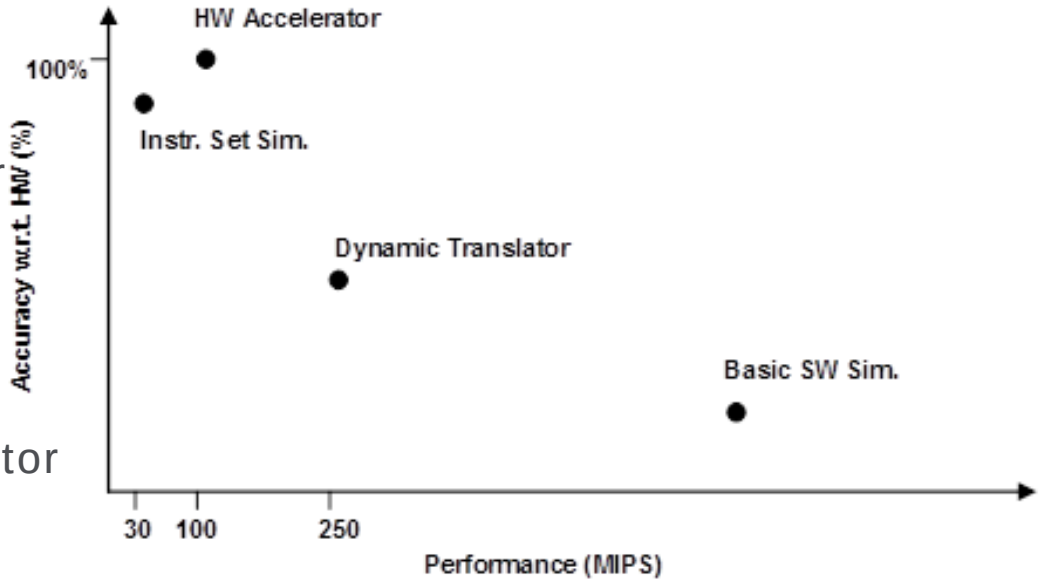
“OBC Simulator Architectures and Interfaces to System Test Benches”

Motive: Moving from processor emulators to System On Chip emulators

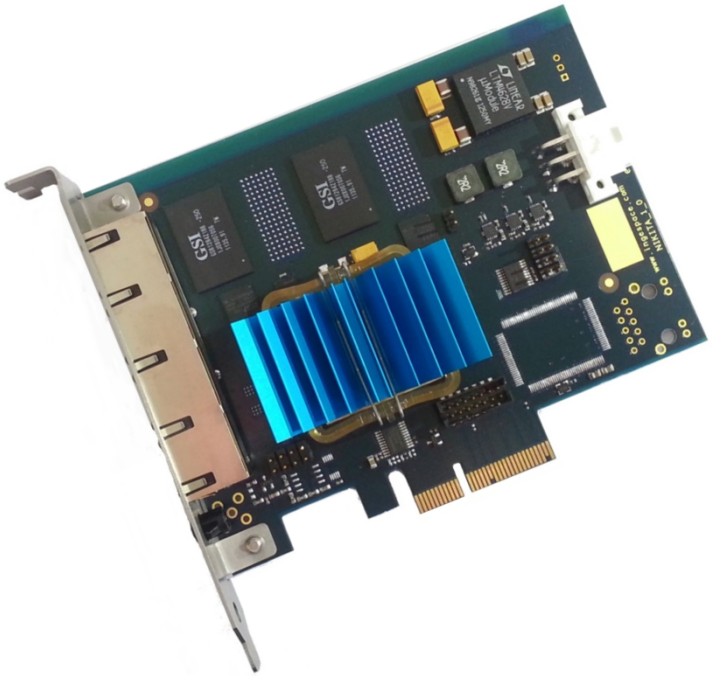


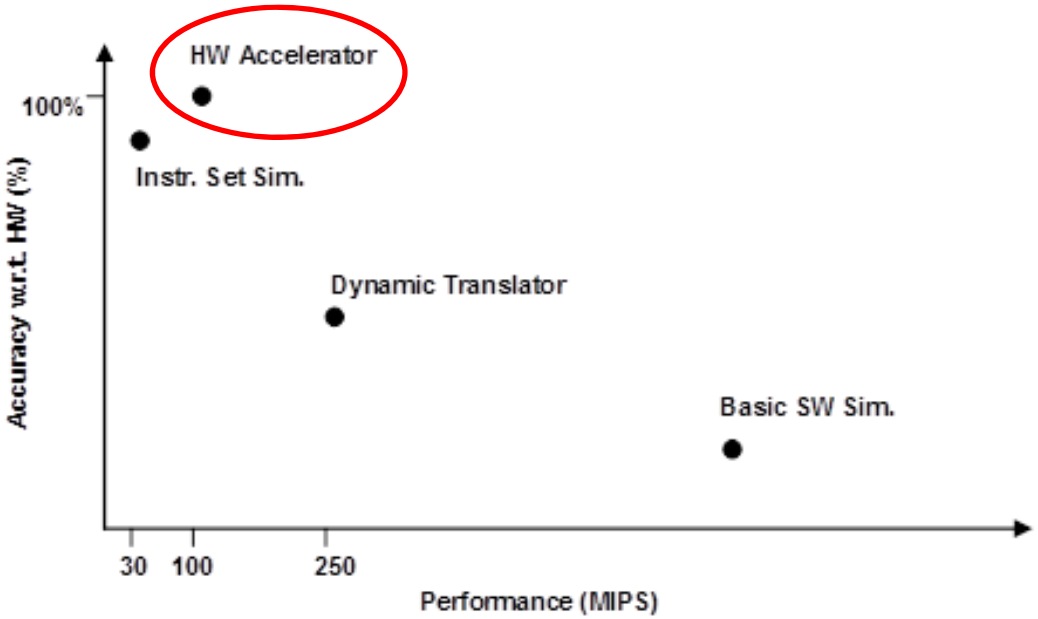
Context: processor emulation techniques

1. Instruction Set Simulation
    a. TSIM: Aeroflex-Gaisler
    b. SimLeon: Airbus
    c. TS: Spacebel
    d. “ESOC simulator”
2. Just-in-time / Dynamic Translator
    a. QERx: SciSys
    b. SimLeon: Airbus
3. Hybrid (HW and SW in the loop)
    a. LeonSVF/Leon Emulator Board: ESA, Airbus, Ingespace & Terma
    b. TSIM-HW: Aeroflex-Gaisler
    c. EPICA-next: TAS, Ingespace
    d. MAS281, DSP21020 … ERC32: SHaM architecture by ESA & Chess



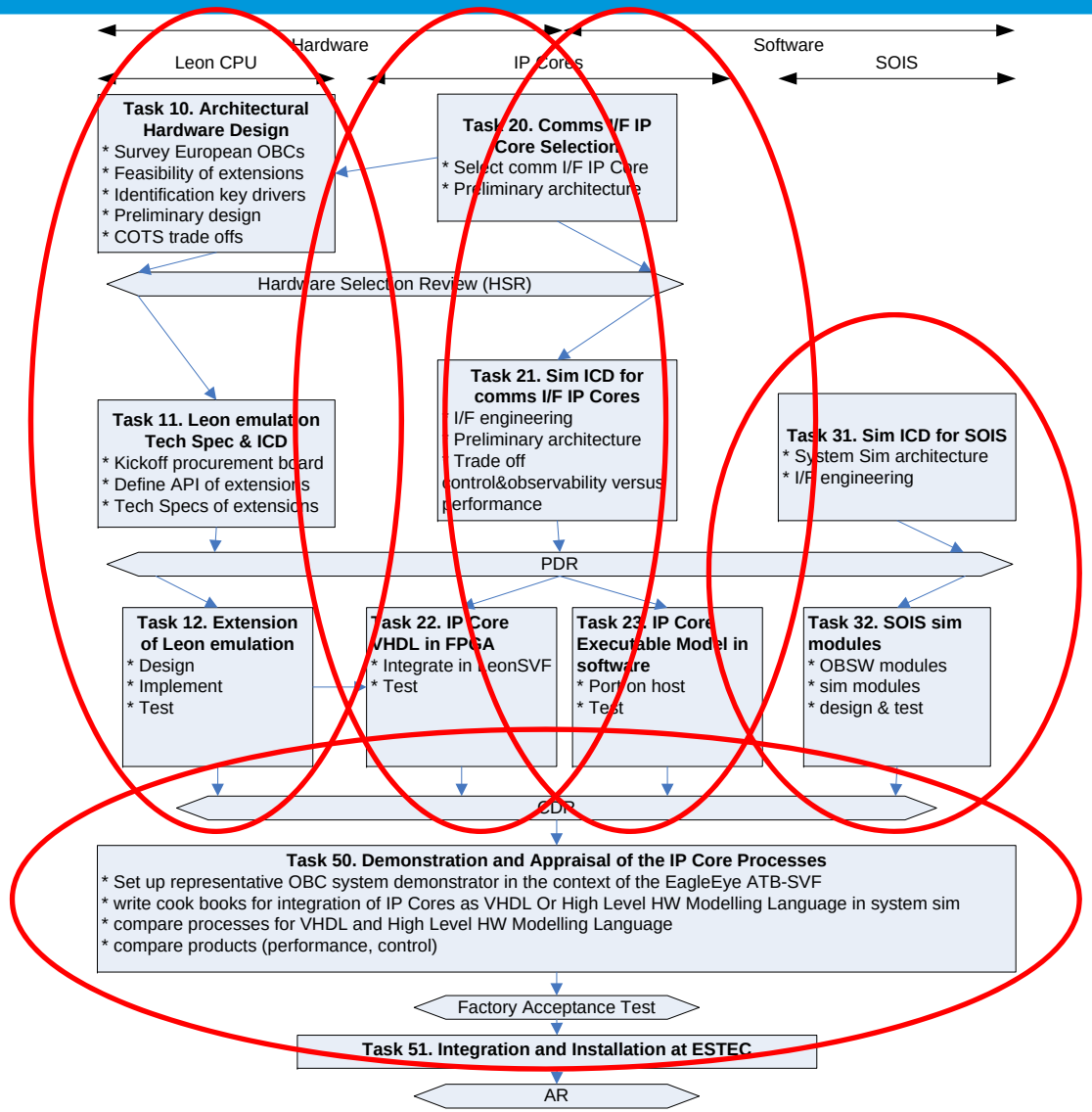
Context: Leon Emulation Board (LEB)





3. **Hybrid (HW and SW in the loop)**
   a. LeonSVF/**Leon Emulator Board**: ESA, Airbus, Ingespace, Terma
      - Leon Processor IP Core (HIL): actual VHDL runs in the FPGA
      - Other IP Cores (HIL/SIL): in FPGA and in workstation
      - I/O peripherals (SIL): simulated in workstation

Project work logic



Hybrid Processor Emulation

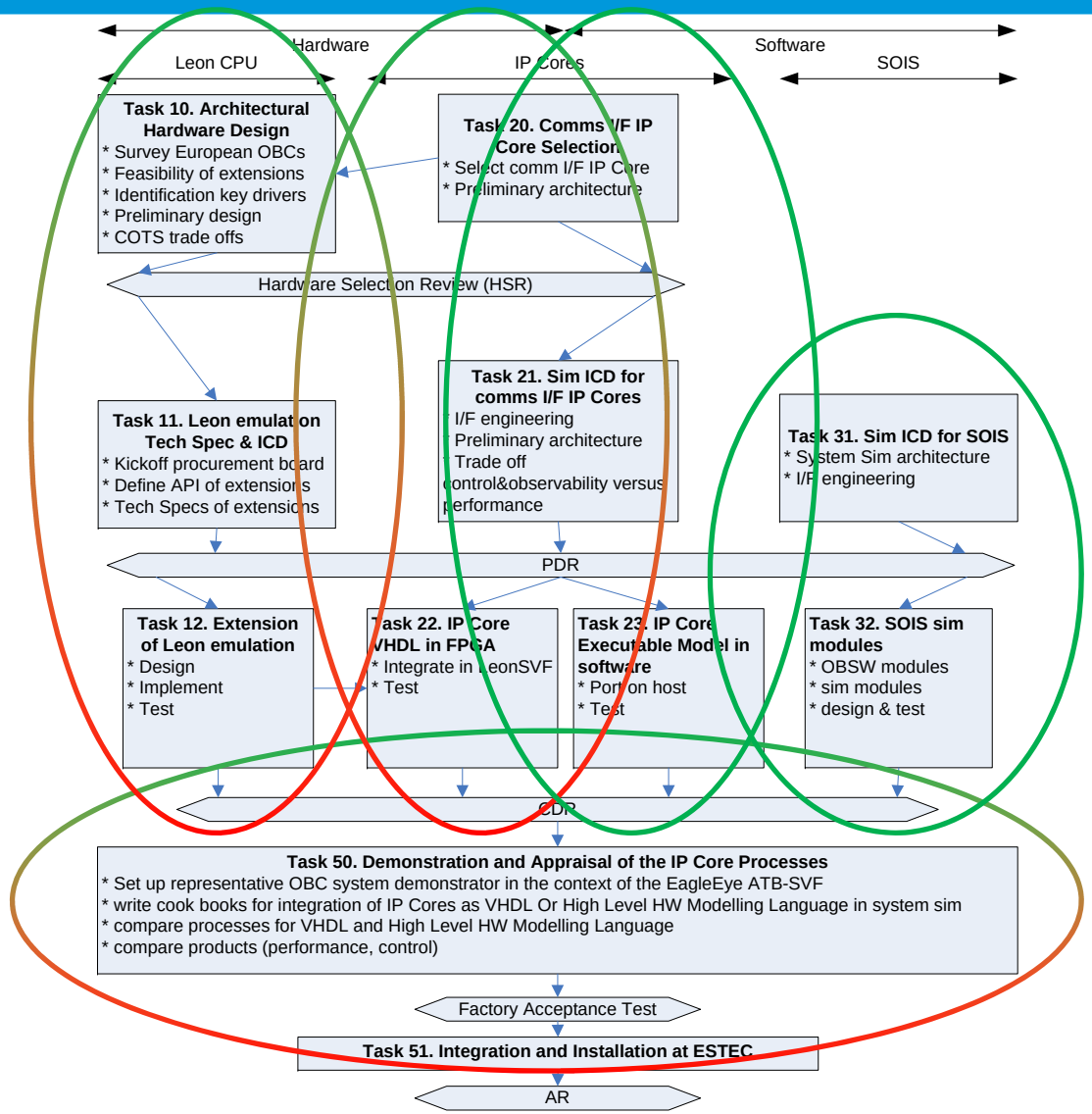
Hybrid SoC Emulation
(some IP Cores of SoC in HW)

Hybrid SoC Emulation
(IP Cores of SoC in SW
Via HW/SW co-engineering)

No IP Cores of SoC:
abstracted at SOIS level

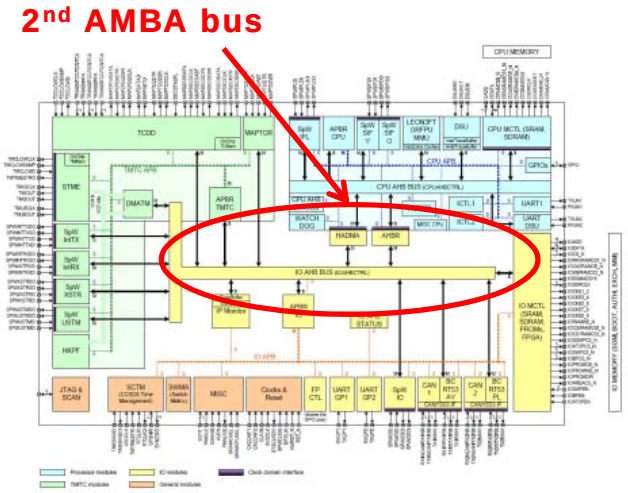
Demonstration:
- EagleEye@Eurosim/SMP2
- SPOT6(SCOC3)@SimTG

Project status



LEB (hybrid proc&SoC emu):

- Baseline functions: CDR
- Optional functions (CCN):
  - sDram: PDR
  - 2nd AMBA: CDR



Demonstration: in progress

- EagleEye@Eurosim/SMP2
  - with LEB and with TSIM
- SPOT6(SCOC3)@SimTG

LEB: simulation functions

LEON2 configuration	LEON3 configuration	SCOC3-inspired configuration (extension of LEON3 configuration)
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from processor to SoC

LEB: simulation functions

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From old HIL emulators (ASIC) to new HIL emu (SoC in FPGA)

LEB: fundamental operational principle

- Simulated Real Time counter (SRT) ←→ Leon clock
- Leon clock & SRT are suspended/frozen when:
  - OBSW accesses I/O
  - OBSW accesses AMBA
  - SoC Tx/Rx a SpW packet / UART character / PIO pin toggles…
  - Simulation Time Events expires
- LEB calls back simulation SW via the PCI express bus (comm overhead)
- Simulation SW do their work:
  - provide data to / retrieves data from SoC (I/O, AMBA, RAM…)
  - Raise interrupts…
- Leon clock & SRT are resumed
- … and so on…

LEB: Performance

example	
n. APB AMBA read / sSRT (suspend on PCIexpress)	5,000
n. APB AMBA write / sSRT (suspend on PCIexpress)	5,000
n. time events/sSRT (suspend on PCIexpress)	1,000
throughput simulations → I/O mapped memory (across PCIexpr) [KBytes/sSRT]	130 KB/s
throughput simulations ← I/O mapped memory (across PCIexpr) [KBytes/sSRT]	130 KB/s
max OBC Frequency while real time [Mhz]	68 Mhz

sSRT = second of simulated time

LEB: performance

Stress Test : Airbus DS SCOC3 Simulation with small OBSW derived from SPOT6

Suspend Cause	Average number of occurrences per second SRT
Read into I/O Suspend Area	3452
Write into I/O Suspend Area	867
Amba Slave APB read	65
Amba Slave APB write	65
Amba Slave AHB read	1
Amba Slave AHB write	1
UART Byte sending	2
Timed event trigs	70
SPW packet emission	7521
Time Windows	128

More than 12 000 suspend per second

60Mhz OBC Simulation run in real-time

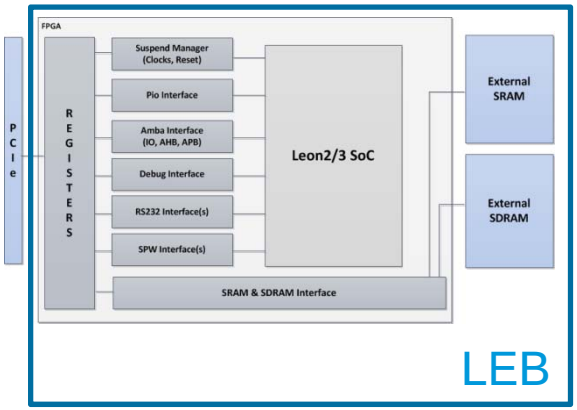
Read/Write Accesses on I/O Space	Data rate
OBSW read to IO Exclusion Area	8.12 MB/s
OBSW write to IO Exclusion Area	16.79 MB/s
OBSW read to IO Suspend Area	13.52 kB/s
OBSW write to IO Suspend Area	13.44 kB/s

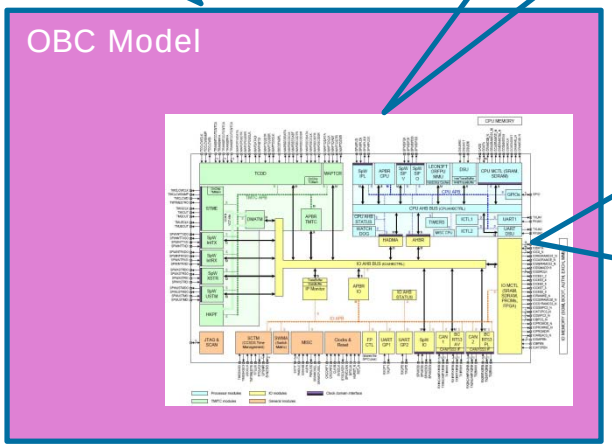
Interfaces

OBC Simulator Architectures and Interfaces to System Test Benches

OBC Model within System Simulator:
- SMP2
- SpW packets between models

Processor or SoC emulator within OBC Model:
TSIM with extensions





Internals of processor or SoC emulator:
- Reusable VHDL simulation building blocks interface SoC at signal level where possible

HW/SW Co-engineering

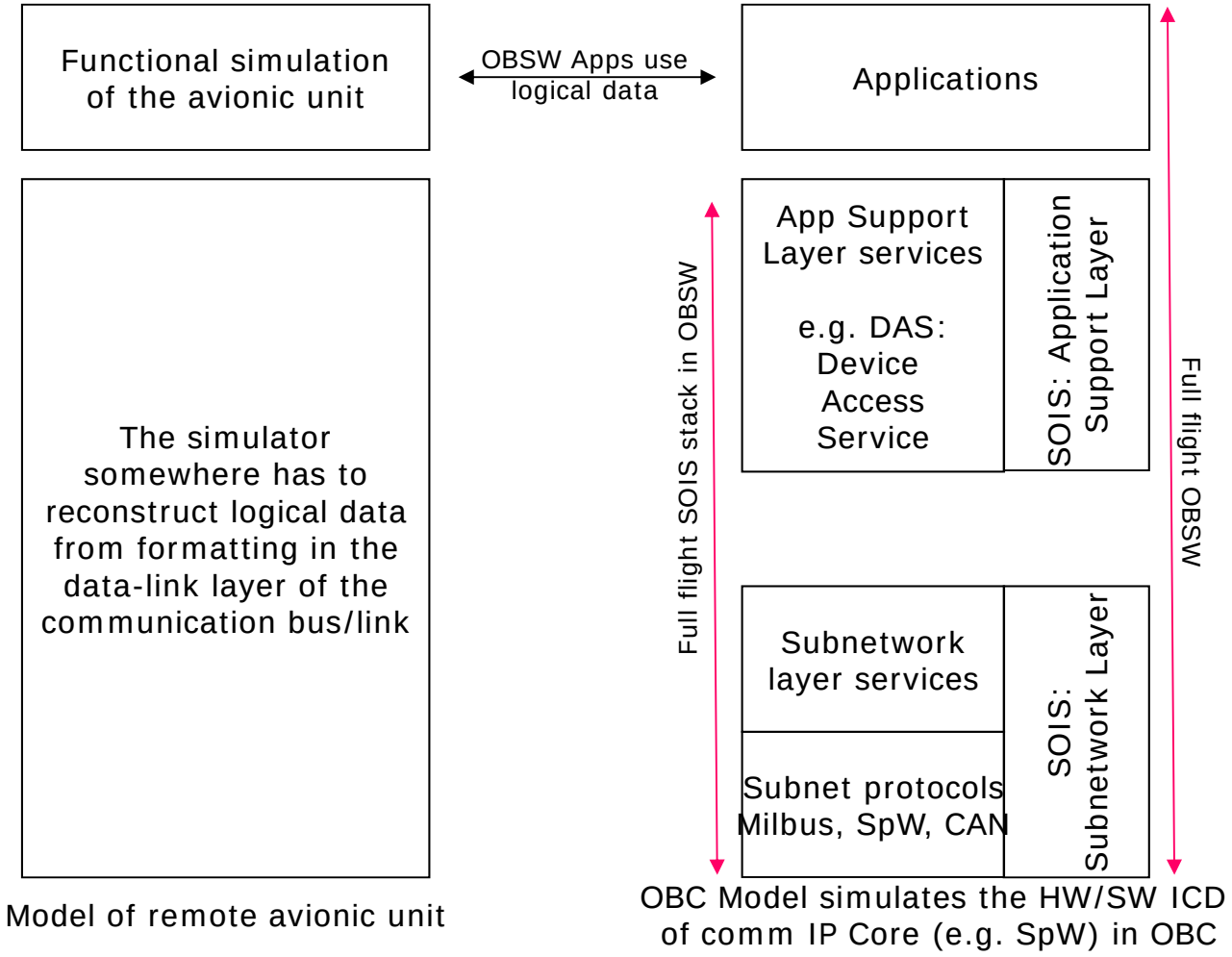
1. HW-engineer and SW-engineer cooperate on a single model (e.g.) of a functional block within a System On Chip

2. Used pre-existing SpaceWire SystemC/Transaction Level Model
3. Issues irrelevant to the goal of the SoW impaired the activity:
    a. Documentation hard-to-read
    b. HW/SW interface missing (the model targets the co/dec) → need to re-try with both goals in mind, HW-engineering, SW-engineering
    c. could have reinterfaced → performance certainly poor for SVF
    d. pushed out in favour of other key goals

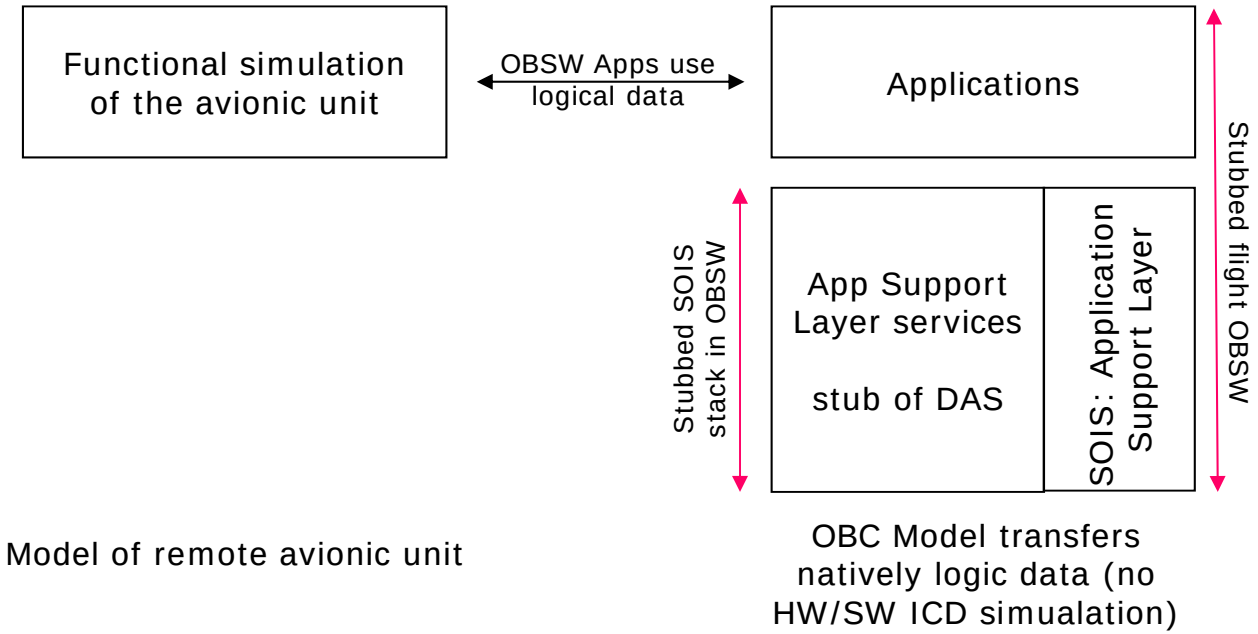
4. Conclusion: need to try again

Interfaces:
ignore IP Core, cut&simulate SOIS (1/2)

Can system simulator take advantage of SOIS-based OBSW in OBC?



Interfaces:
ignore IP Core, cut&simulate SOIS (2/2)



Conclusion: we can swap between full OBSW&Payload and stubbed OBSW&Payload in the EagleEye@Eurosim.

Works in progress...

Conclusions

1. The Leon Emulation Board is
    a. a mature product for processor and SoC HIL emulation
    b. a building block for system simulators (SVF, FV, Ops Sim)
    c. representative (real Leon VHDL)
    d. high-performance: 60 MHz in real time in representative load
    e. TSIM compatible, works in Eurosim & SimTG
2. **Please contact me if you want to try out an LEB**
3. LEB-ecosystem: mature and attractive technology for SoC simulation
    a. will be even richer at next FPD
    b. reusable blocks to tailor LEB easily to specific SoC
    c. Multicore? FPGA-in-the-loop (LEB) or ASIC-in-the-loop
4. HW/SW co-engineering: to be tried again
5. SOIS stack offers convenient cuts in the simulators for high-level early software validation (nothing really new)