Dynamically Reconfigurable Hardware for Resource Efficiency and Fault Tolerance in Space Applications

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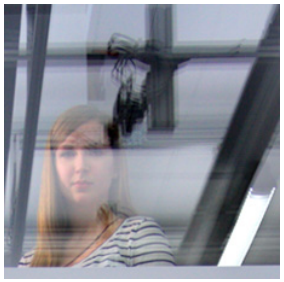
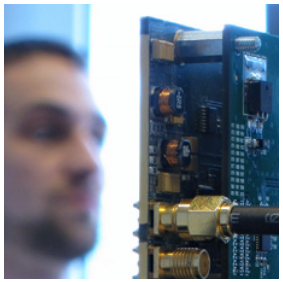
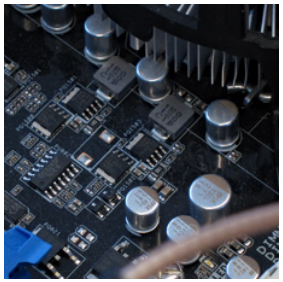





Outline

- **Dynamically Reconfigurable Processing Module (DRPM)**
  - **Architectural overview**
  - **Run-Time Reconfiguration**
  - **Communication and Processing Modules**
  - **Communication interfaces incl. SpaceFibre**
- **Online Testing and Patching Permanent Radiation Effects in Reconfigurable Systems (OLTRE)**
  - **Idea and first results**

Why reconfigurable computing in space?

The need for high performance processing

- Performance of application-specific standard products (ASSPs) often not sufficient
- FPGAs are advantageous for high data rate applications like image processing, signal processing, and software-defined radio

The need to fine-tune payload processing

- Changing or adapting payload processing during the mission
- Time-Sharing of reconfigurable resources between different applications
- Self-Healing mechanisms to fix errors caused by single event effects

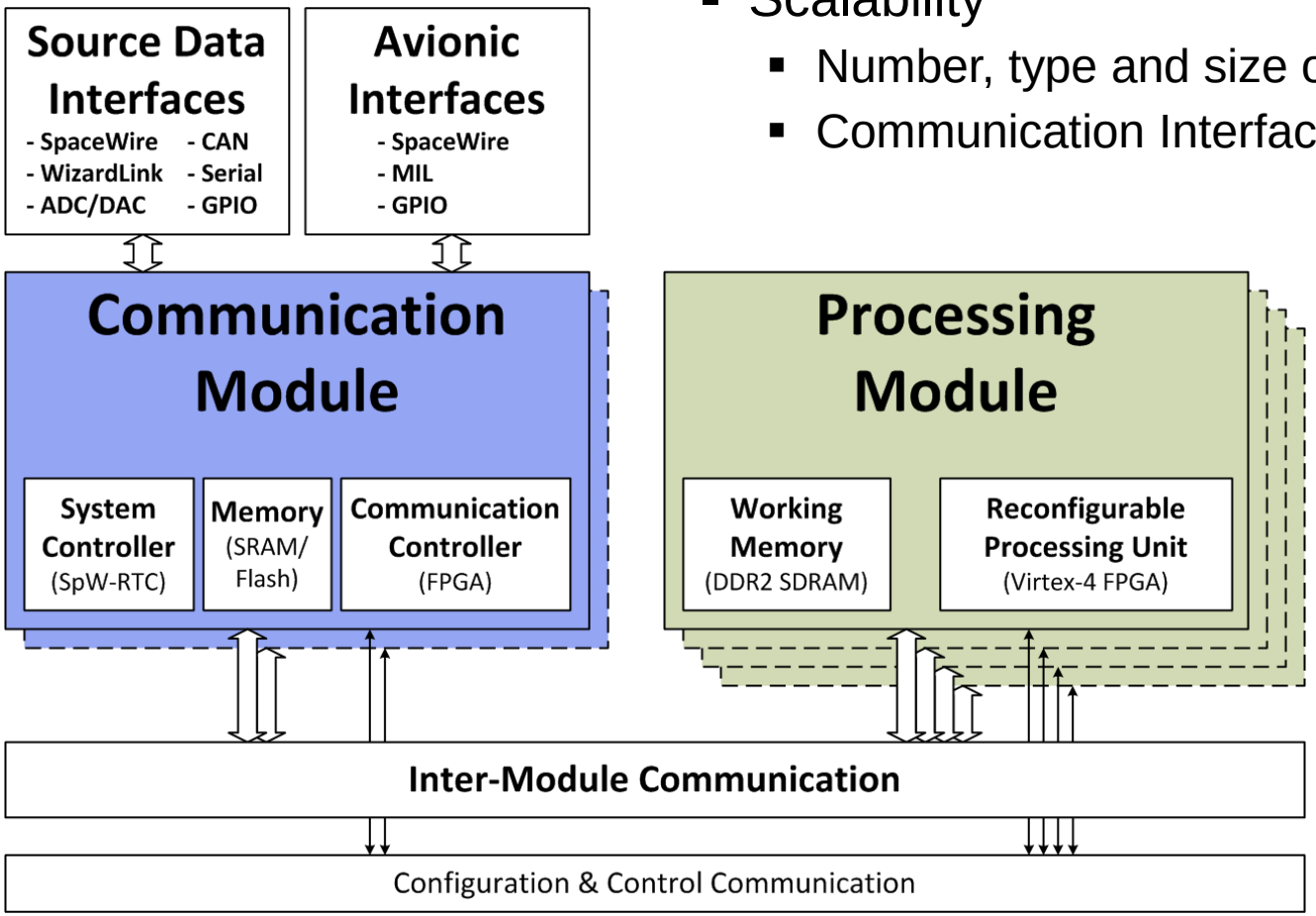
The need for a generic reconfigurable module

- Development is reduced to custom mission-specific modules
- Reduces development costs

Requires

- Sophisticated concepts for dynamic and partial reconfiguration
- Prototyping environments for the evaluation of new architectural concepts

DRPM System Design goals

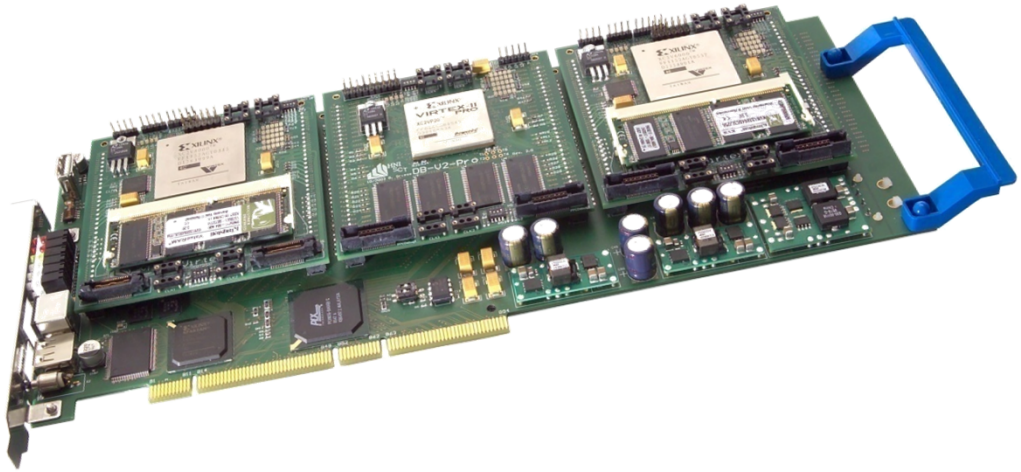


- Scalability
  - Number, type and size of FPGAs
  - Communication Interfaces

Partners

DRPM – Dynamically Reconfigurable Processing Module

Platform for DRPM implementation

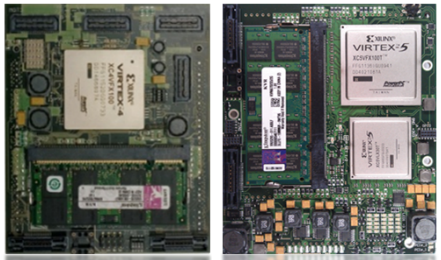


RAPTOR Prototyping Systems

Prototypic Implementation of Microelectronic Circuits on FPGAs

- PCI-X / PCIe Mainboard
- Up to 6 modules
- High bandwidth between modules
- Partial dynamic reconfiguration

FPGA-Modules

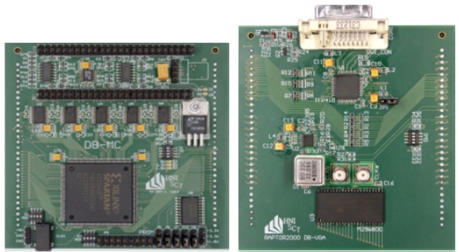


- Xilinx FPGAs up to Virtex 5 (7-series in design)
- Embedded processors
- Up to 4 GB SDRAM

Communication

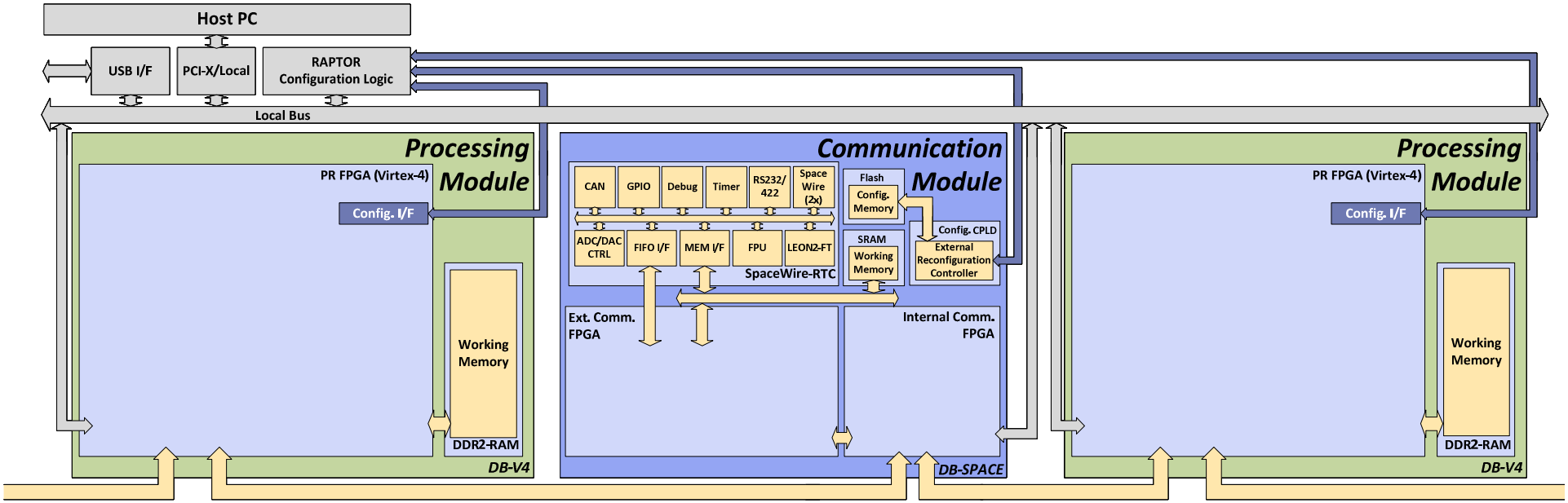
- Ethernet
- FireWire, USB
- CAN, LON, EIB, Interbus
- Serial, Parallel

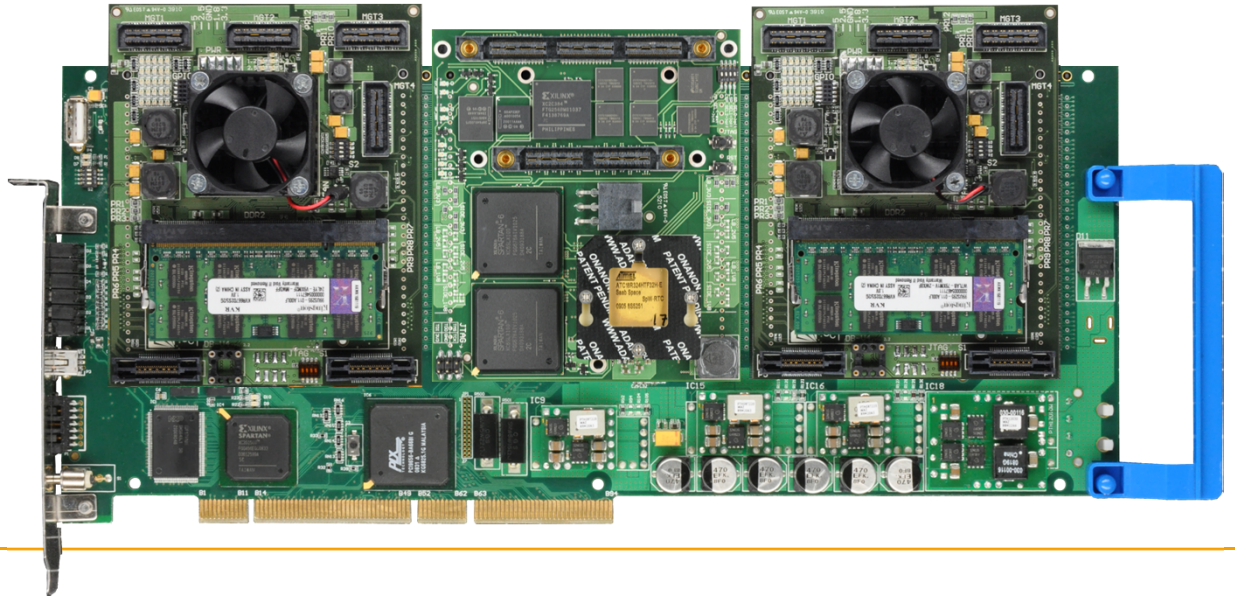
I/O-Modules



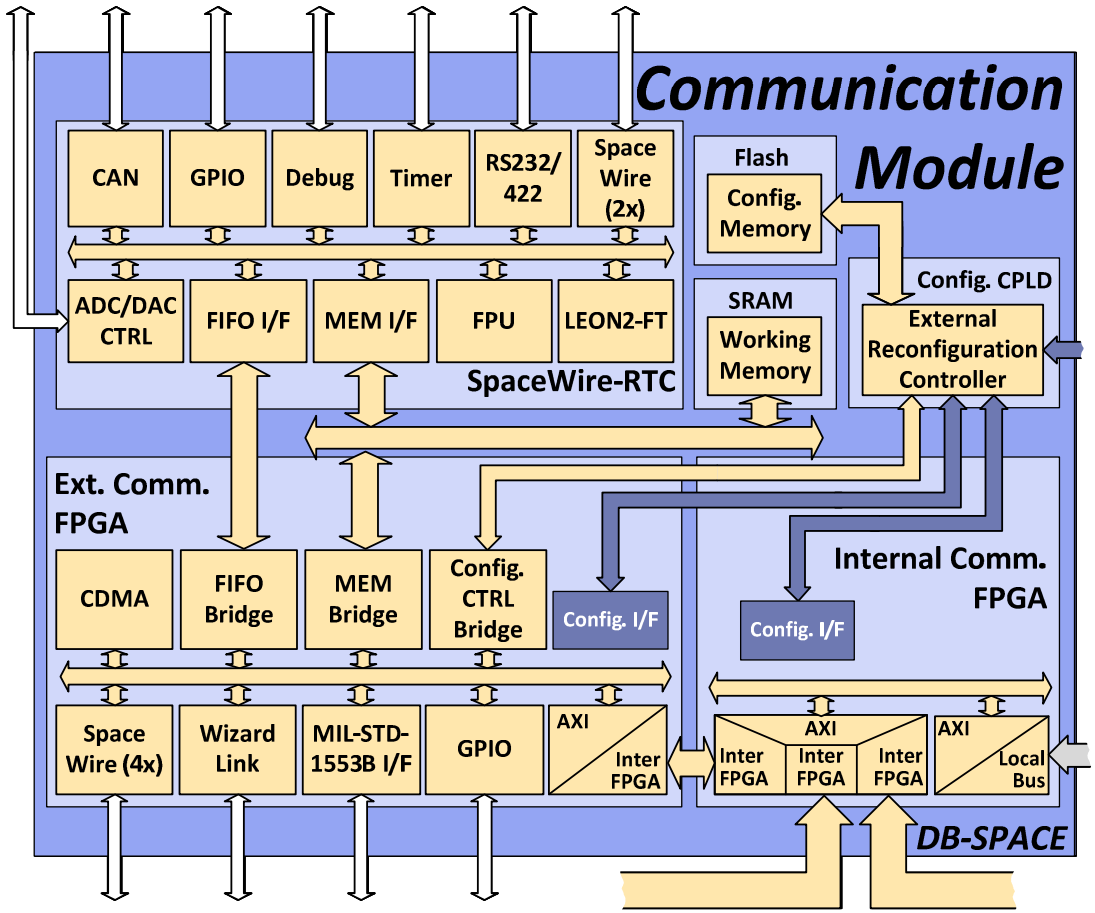
- Analog I/Os
- Digital I/Os
- SSI interfaces
- VGA interface

DRPM Overview





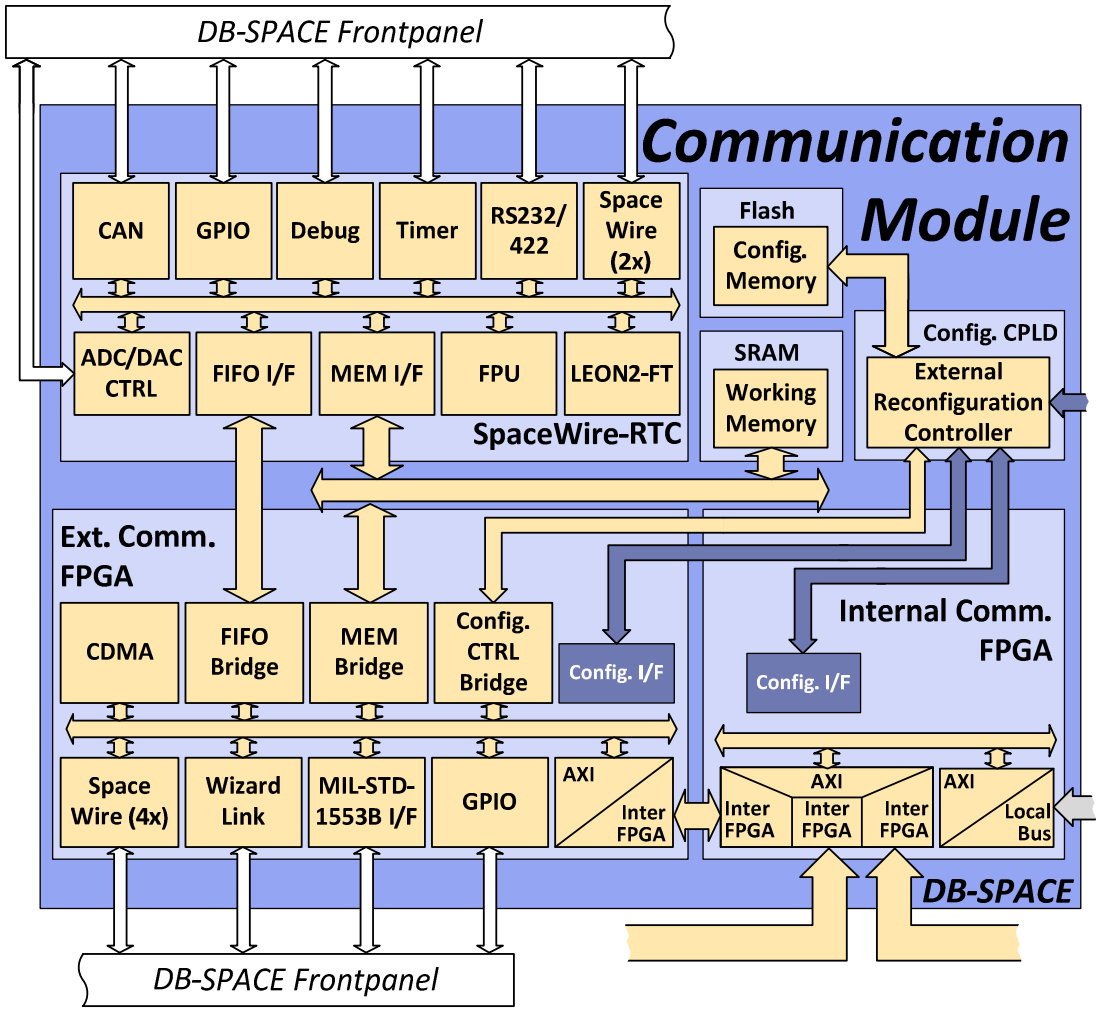
Communication Module DB-SPACE

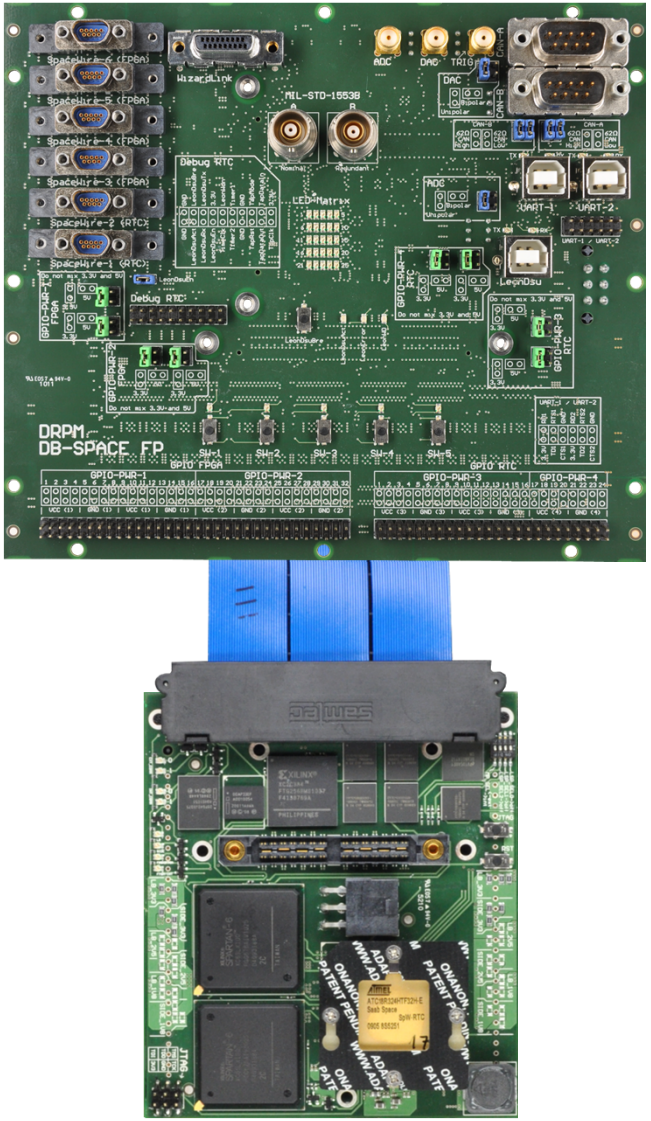


- System Controller: SpaceWire RTC AT7913E
  - LEON2-FT CPU
  - 2 SpaceWire Interfaces
  - CAN, ADC/DAC, GPIO, …
- External Comm. FPGA (XC6SLX150)
  - 4 SpaceWire Links
  - SpaceFibre Interface (2.5 Gbit/s)
  - MIL-STD-1553B
  - 32 GPIOs
- Internal Comm. FPGA (XC6SLX100)
  - Flexible communication to other modules
- AMBA AXI4 communication among IP cores
- Ext. Reconfiguration Controller

DB-SPACE Frontpanel

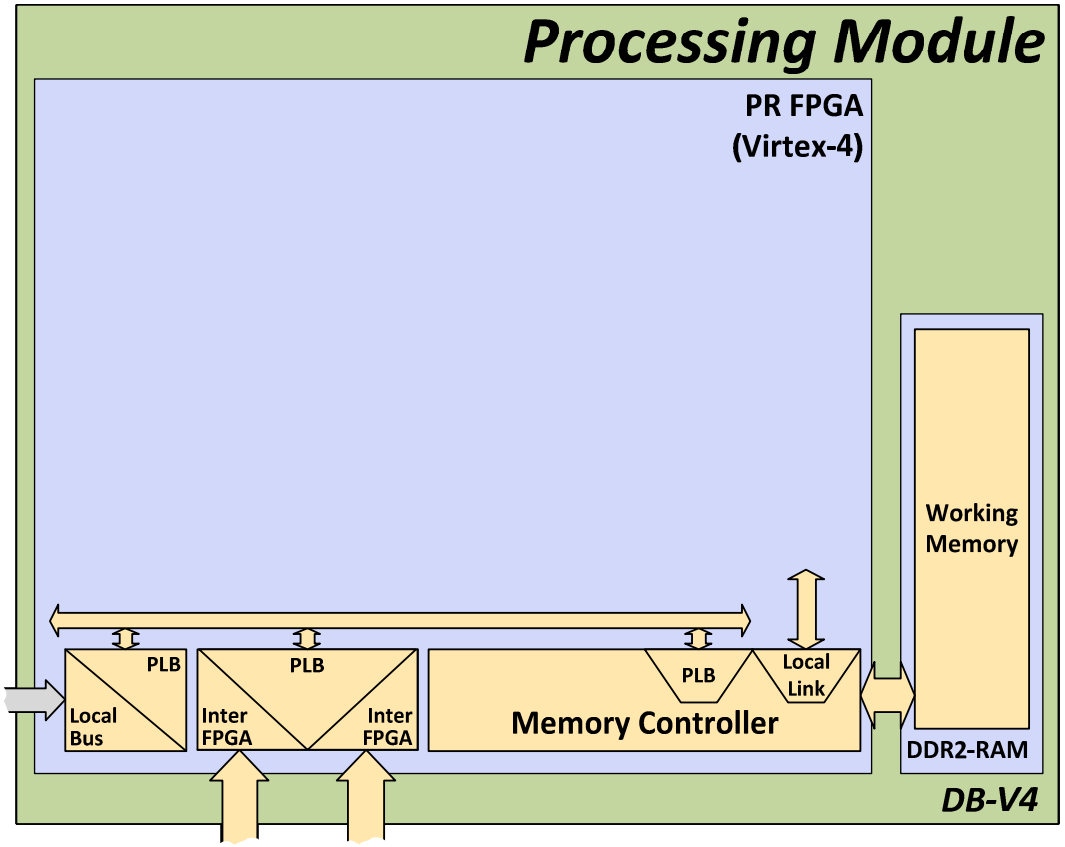
- Easy access to the interfaces of DB-SPACE





Galvanic isolation of all interfaces,
including SpaceWire, CAN, GPIO, ADC

Processing Module DB-V4

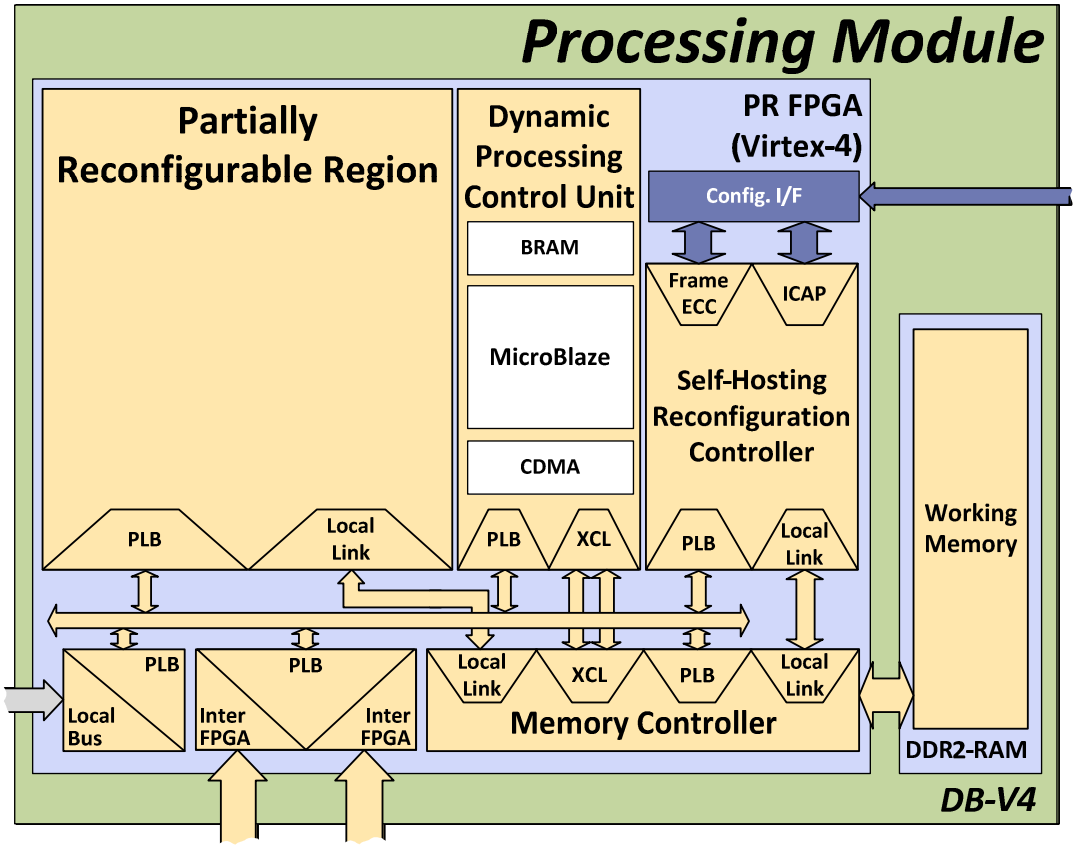


- PR FPGA (XC4VFX100)
- 4 GByte DDR2 SDRAM

FPGA Static Area

- Multi Port Memory Controller
  - 32b data, 7b ECC (BCH 32,7)
  - Integrated ECC statistics unit
  - Integrated fault injection
- Communication
  - PLB based module interconnect
  - Bridge to other modules
  - Monitoring and debug bridge
  - Local Link for streaming data

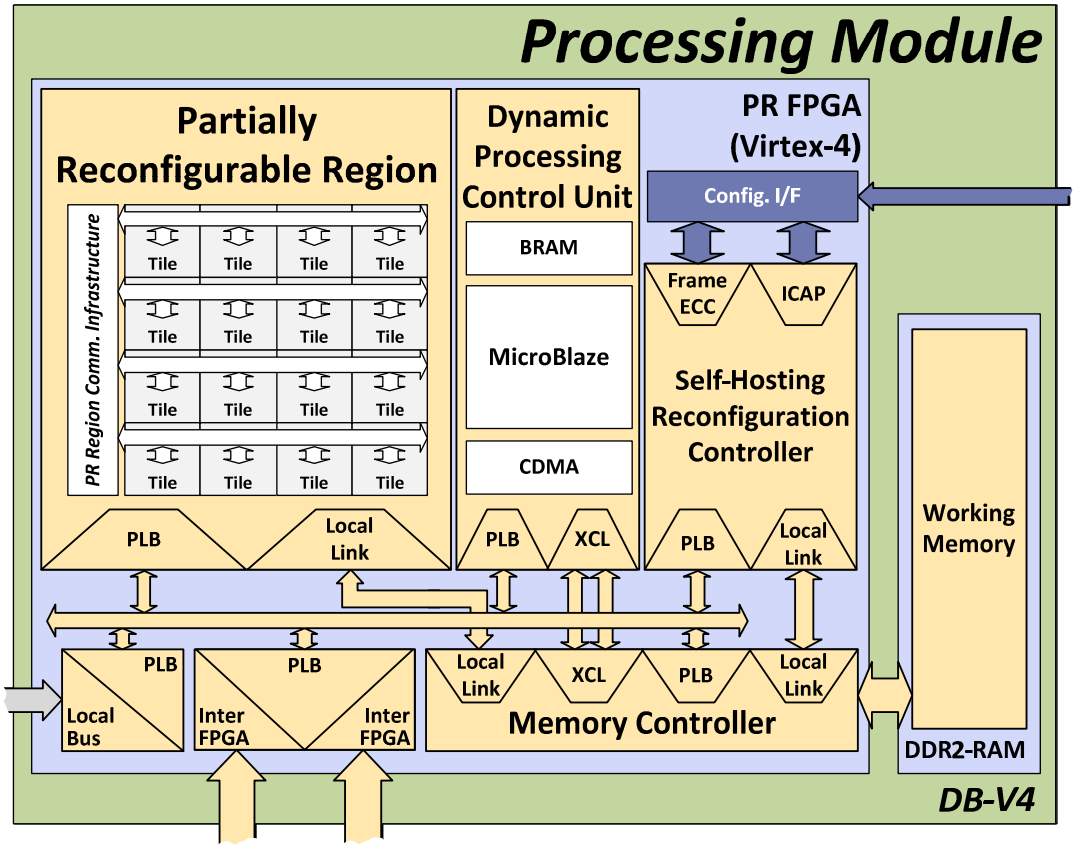
Processing Module DB-V4



- Self-Hosting Reconfiguration controller
  - Performs bitstream relocation, transfers bitstream to ICAP
  - Individual scrubbing rates for different FPGA regions
  - Fault injection utilizing partial reconfiguration
- Dynamic Processing Control Unit
  - Maintains the free resources, determines feasible position for new modules
  - Reconfiguration is triggered internally or via external interfaces

Partially Reconfigurable Region

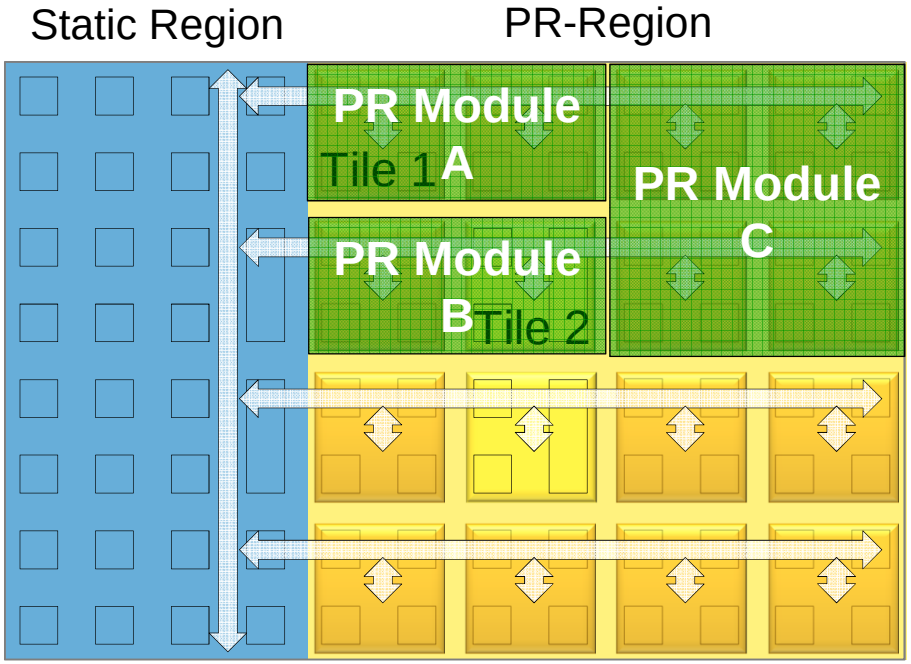
Partially Reconfigurable Region



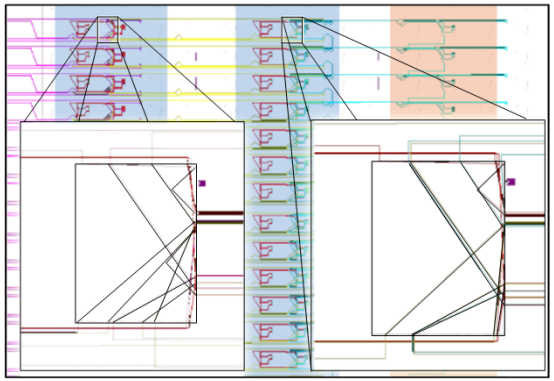
- Tiled PR-region
  - Flexible module placement
  - PR-modules can be placed at any position within the partially reconfigurable region
- Homogeneous communication infrastructure
  - Integrated address decoder and PR tile management
  - Enables relocation of modules

Dynamic Reconfiguration of FPGAs

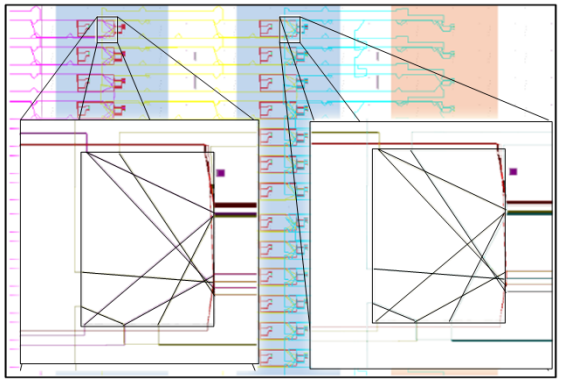
- Homogeneity allows placement of modules at any position with the same type of tiles
- Communication macro must occupy the same resources in every tile
- Automatic generation of communication infrastructure based on VHDL specification
- DHHarMa: Dedicated placer and router for homogeneous macros up to Xilinx 7-Series [FCCM 2011]



Xilinx Router



DHHarMa Router



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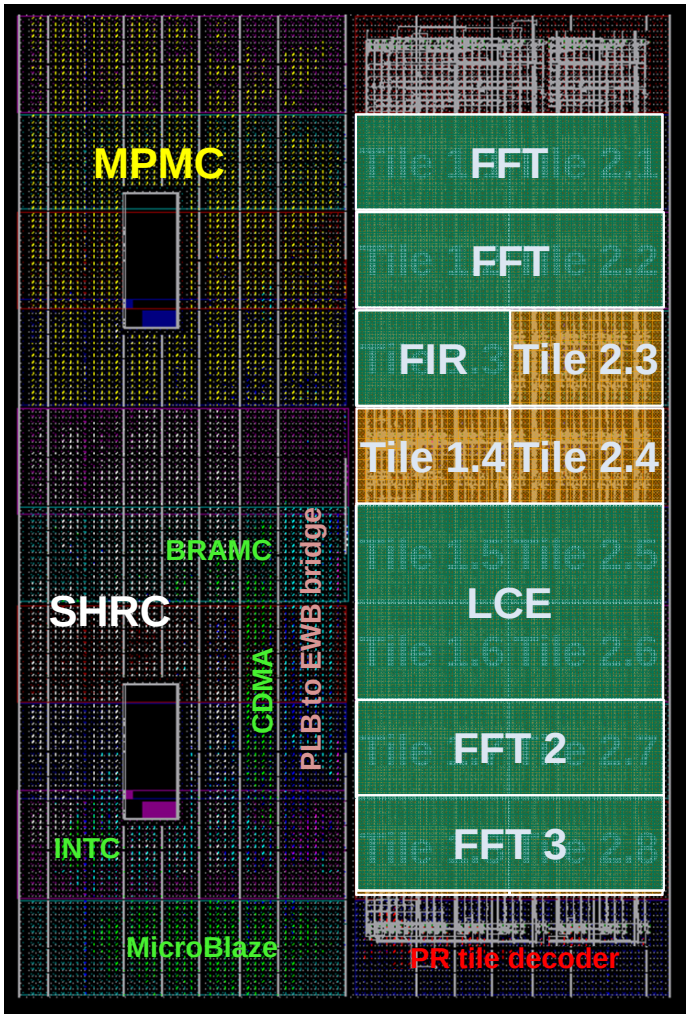
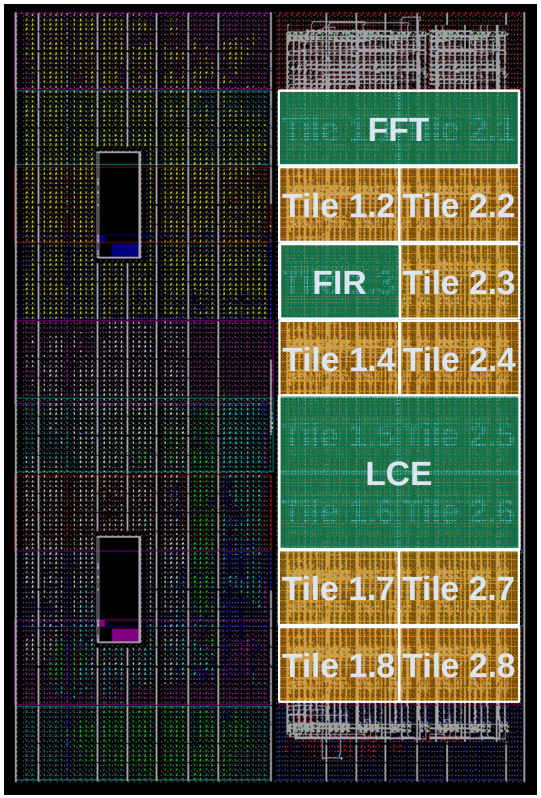


Xilinx Virtex-4 FX100

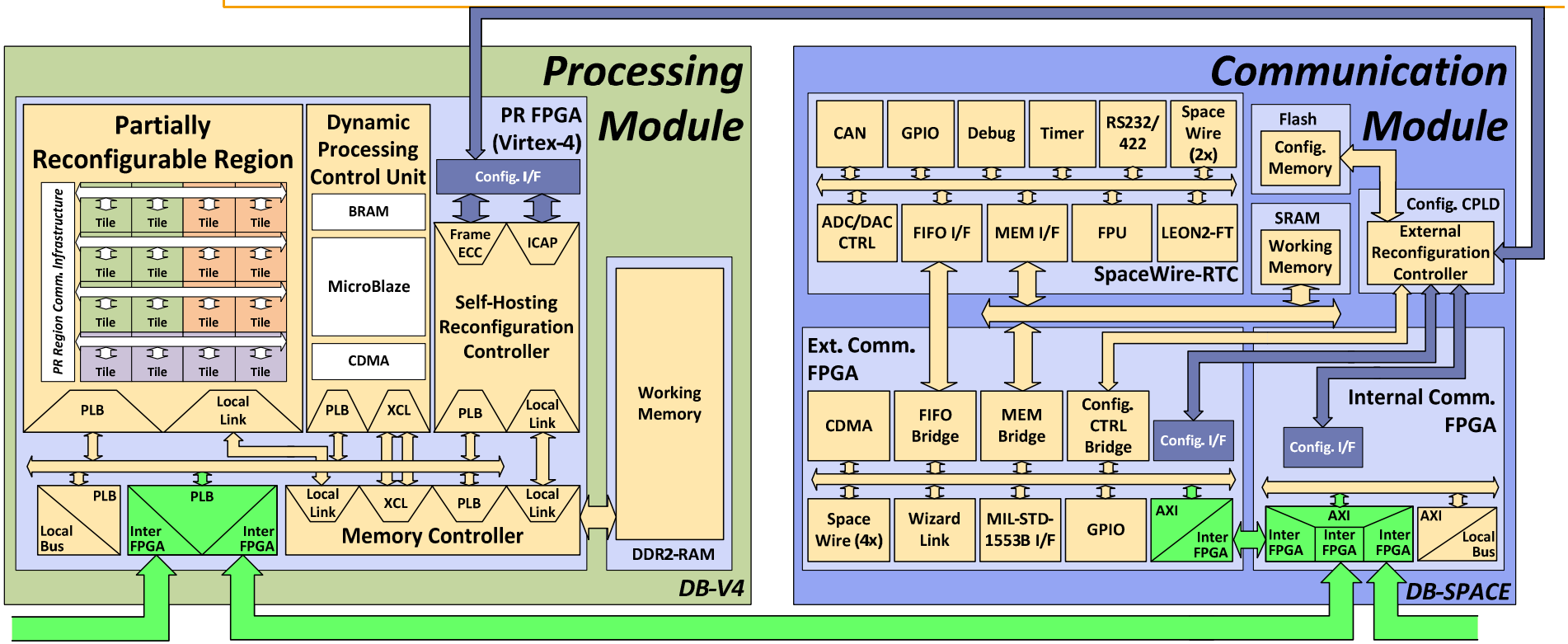
SHRC - Scrubbing Unit

- Combined solution for partial reconfiguration and readback-scrubbing
  - Completely autonomous
  - Scheduling parameterisable for each module, maintained internally
  - Automatically corrects all 1-bit errors, detects 2-bit errors
  - Provides error statistics (number of errors, time, location)
- Performance
  - Achieved reconfiguration rate: 400 MByte/s
  - Readback-scrubbing of complete Xilinx XCV4FX100:
    3,9 MByte => 10 ms (100 scrub/s)
  - Readback-scrubbing of one tile:
    66 kByte => 170 µs (5.900 scrub/s)
- Error mitigation
  - DPCU detects errors of scrubbing unit (heartbeat)
  - Scrubbing unit detects errors of the ICAP
    SEFI-test (Single Event Functional Interrupt)
    before each scrubbing/reconfiguration task



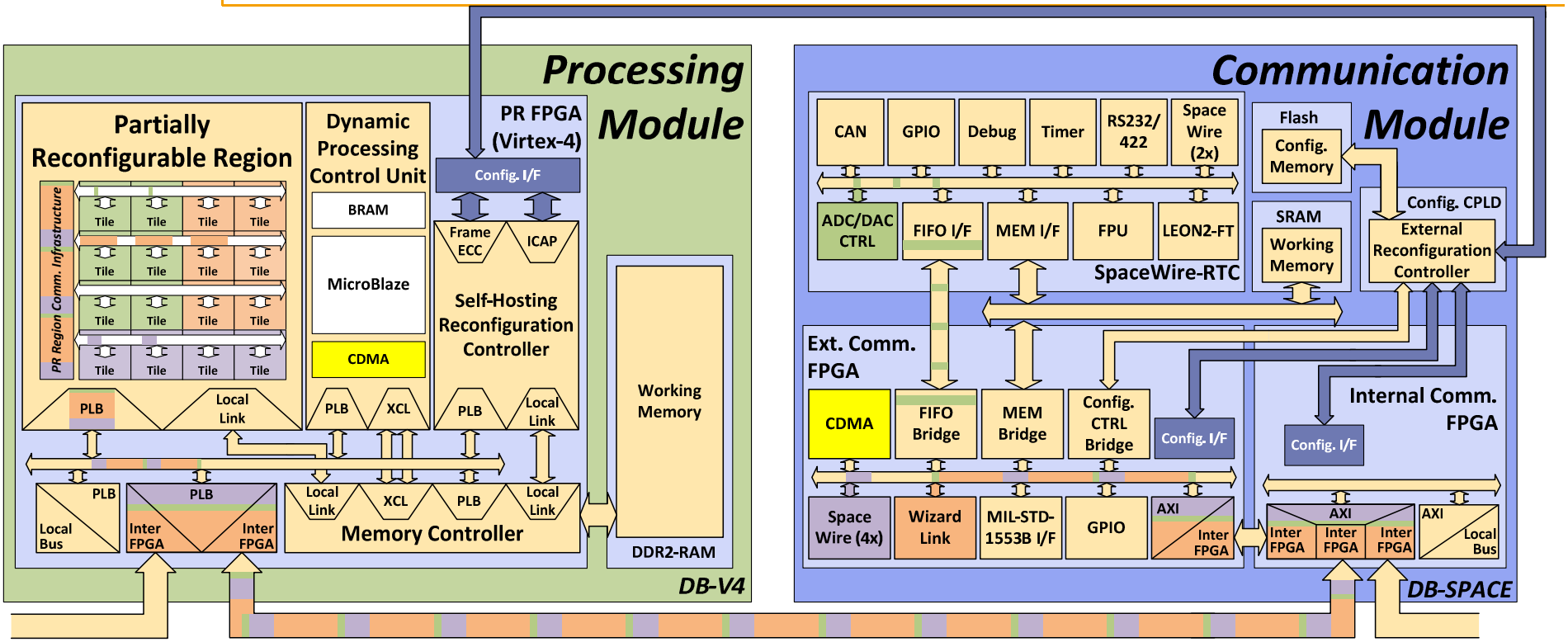
Xilinx Virtex-4 FX100

Communication Infrastructure



- Inter-FPGA interface for communication between FPGAs
  - Abstracts from physical interface between FPGAs
  - Master/Slave interface to AXI/PLB bus
  - Integrated packetizer and flow control

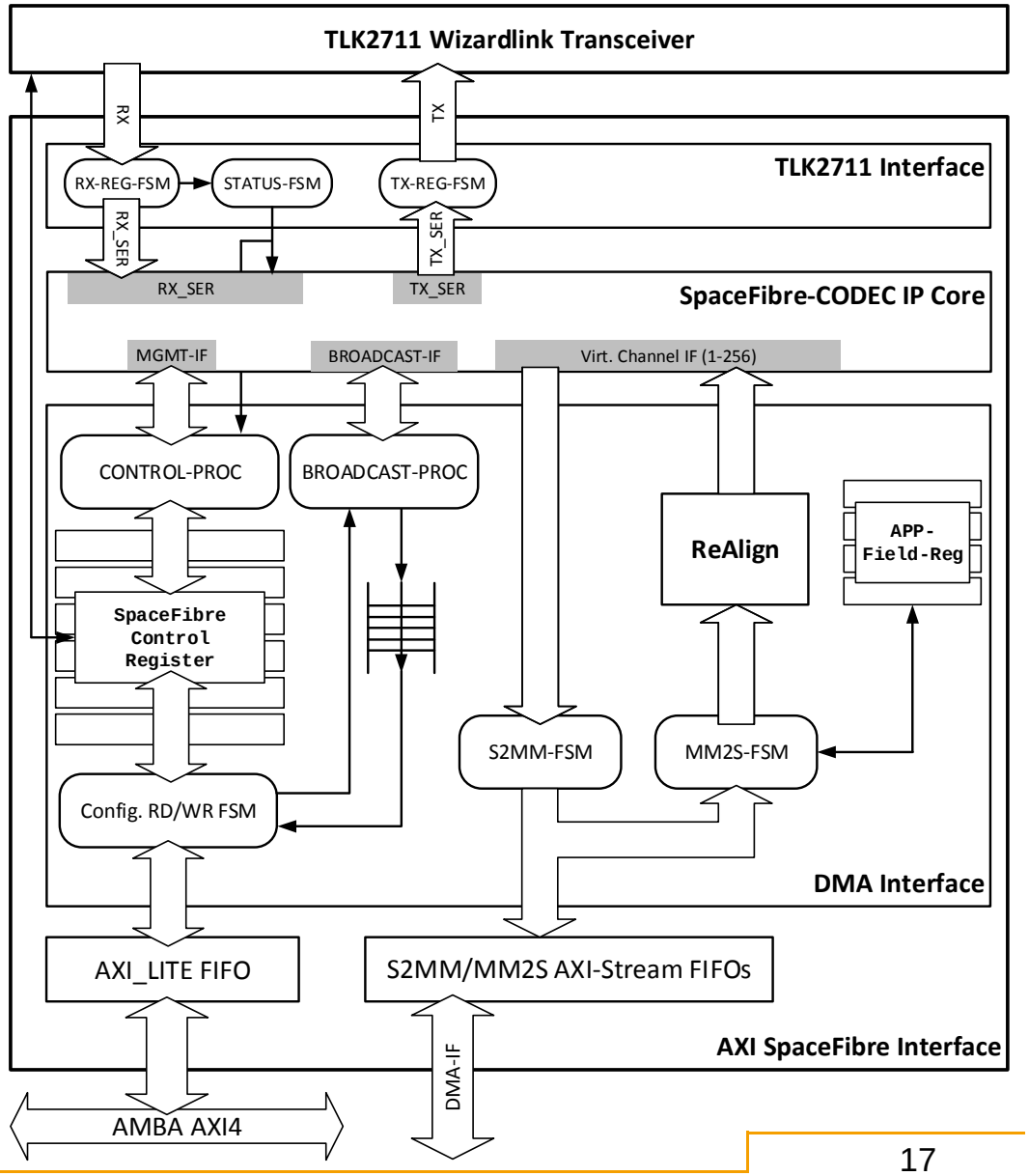
Communication Infrastructure



- Inter-FPGA interface for communication between FPGAs
  - DMA unit enables burst transfers
  - RRMU (Resource and Reconfiguration Management Unit) schedules parallel data transmission and controls the involved DMA units

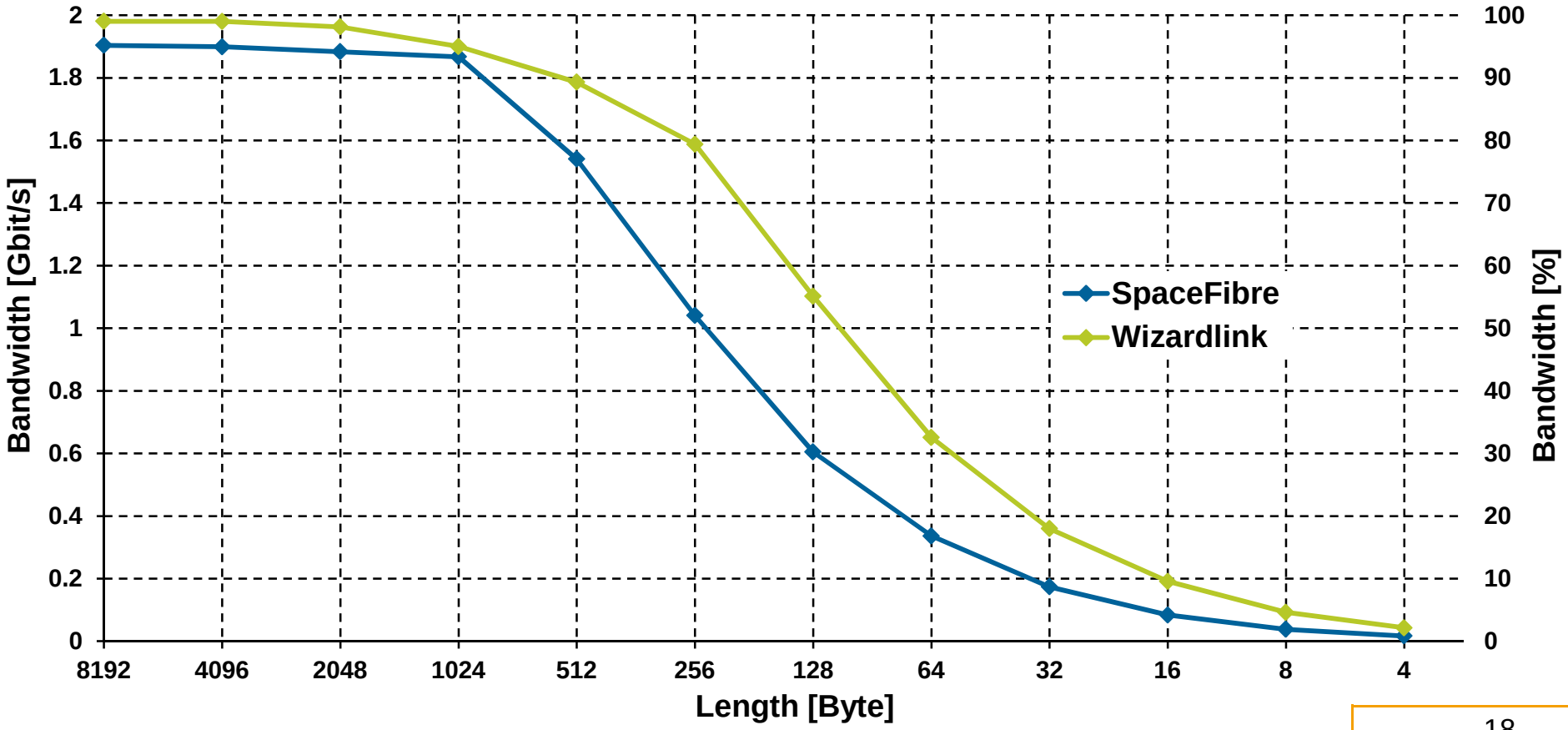
SpaceFibre

- Based on Star-Dundee IP-Core
- 1.6 Gbps – 2.7 Gbps line rate
- Scatter/Gather feature of DMA-Core used for efficient data transfer
- Data streams used for payload information, control streams used for selection virtual channels and routing information
- FIFO-based broadcast interface
- Available as Xilinx EDK Core



SpaceFibre/Wizardlink

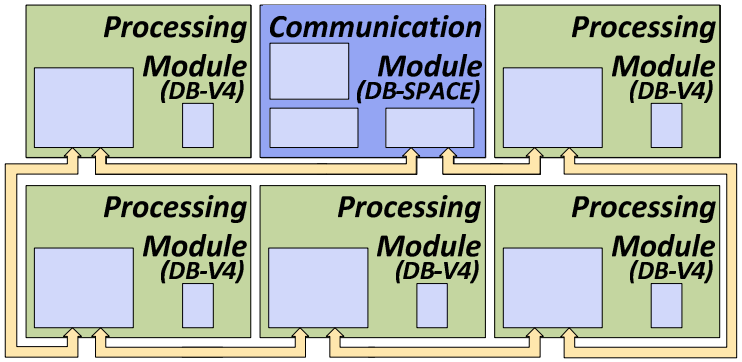
- Bandwidth dependent on packet length
  - WizardLink
  - > 90 % for packets longer than 512 Byte
  - > 98 % for packets longer than 2048 Byte
  - SpaceFibre
  - > 90 % for packets longer than 1024 Byte
  - not more than 95 % achieved



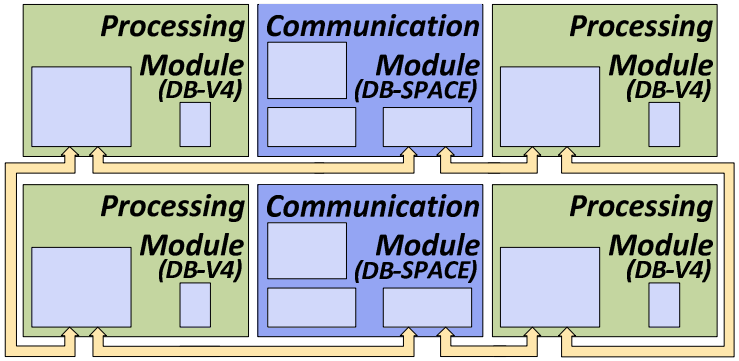
Communication Infrastructure

		Signaling Rate	Effective Bandwidth
External Interfaces	MIL-STD-1553B	1 Mbit/s (HD)	0.7 Mbit/s (HD)
	SpaceWire-RTC	200 Mbit/s (FD)	160 Mbit/s (FD)
	SpaceWire-FPGA	200 Mbit/s (FD)	160 Mbit/s (FD)
	SpaceFibre	2500 Mbit/s (FD)	1900 Mbit/s (FD)
Internal Comm.	Inter-FPGA	3200 Mbit/s (FD)	3100 Mbit/s (FD)
	AMBA AXI4	3200 Mbit/s	3100 Mbit/s
	PLB	6400 Mbit/s	6200 Mbit/s

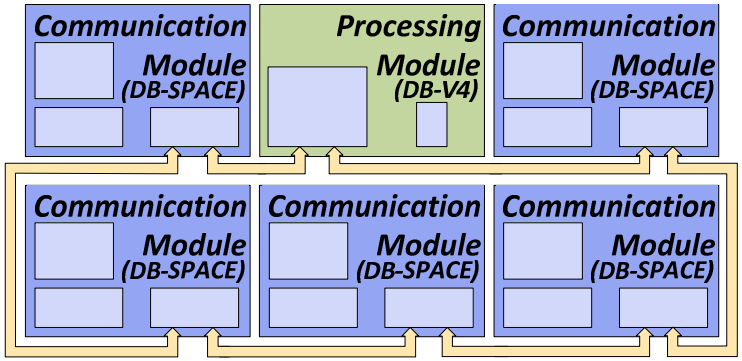
DRPM – Scalability



- 6x SpaceWire
- 1x SpaceFibre, MIL, CAN, ADC/DAC
- 54x GPIO
- 20 GByte DDR2, 1 Gbit Flash
- 5 Xilinx Virtex-4 FX100 FPGAs



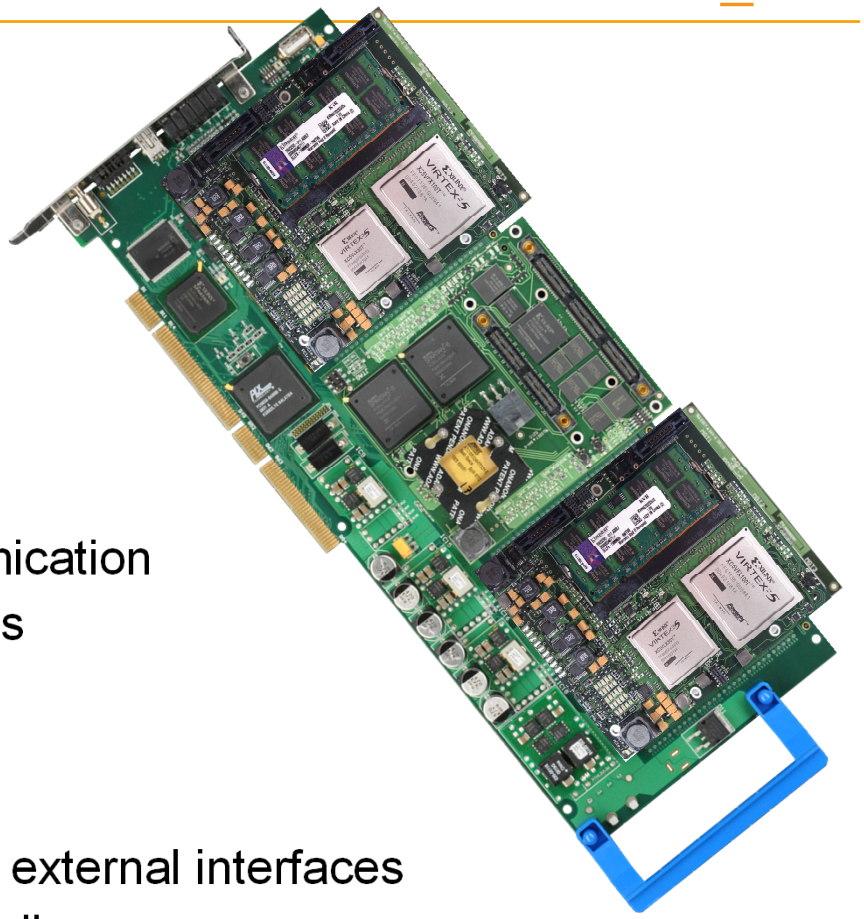
- 12x SpaceWire
- 2x SpaceFibre, MIL, CAN, ADC/DAC
- 108x GPIO
- 16 GByte DDR2, 2 Gbit Flash
- 4 Xilinx Virtex-4 FX100 FPGAs



- 30x SpaceWire
- 5x SpaceFibre, MIL, CAN, ADC/DAC
- 270x GPIO
- 4 GByte DDR2, 5 Gbit Flash
- 1 Xilinx Virtex-4 FX100 FPGA

DRPM – Conclusion

- **Scalable system architecture**
  - Number of FPGAs and Interfaces
  - New FPGAs (Xilinx Virtex-5 FX100T)
  - New host interfaces (PCIe)
- **EDK based design flow**
  - Easy IP-core reuse for other systems
  - IP-cores for internal and external communication
  - ESA IP-cores extended with AXI interfaces
- **Partial run-time reconfiguration**
  - 400 MByte/s reconfiguration bandwidth
  - Self-reconfiguration or reconfiguration via external interfaces
  - High scrubbing-rates with dynamic scheduling



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  - **Architectural overview**
  - **Run-Time Reconfiguration**
  - **Communication and Processing Modules**
  - **Communication interfaces incl. SpaceFibre**
- **Online Testing and Patching Permanent Radiation Effects in Reconfigurable Systems (OLTRE)**
  - **Idea and first results**

OLTRE - Goals

FPGAs can be affected by **SEE** and **TID**

- Single Event Effect: Effect of a particle causing soft error(s)
  - ⇒ Memory elements (SEU)
  - ⇒ Transient effects (SET), …
- Total Ionizing Dose: effect of charge accumulation
  - ⇒ Permanent errors
- **Idea:** Flow capable to detect and patch partially damaged FPGAs used in space flight missions
- **Key Aspects:**
  - On-line testing of partially FPGAs resources
  - SEUs tools utilized for detection of permanent fault
  - Design flow suitable for Xilinx Virtex-4, -5, -6, -7 and Spartan-6

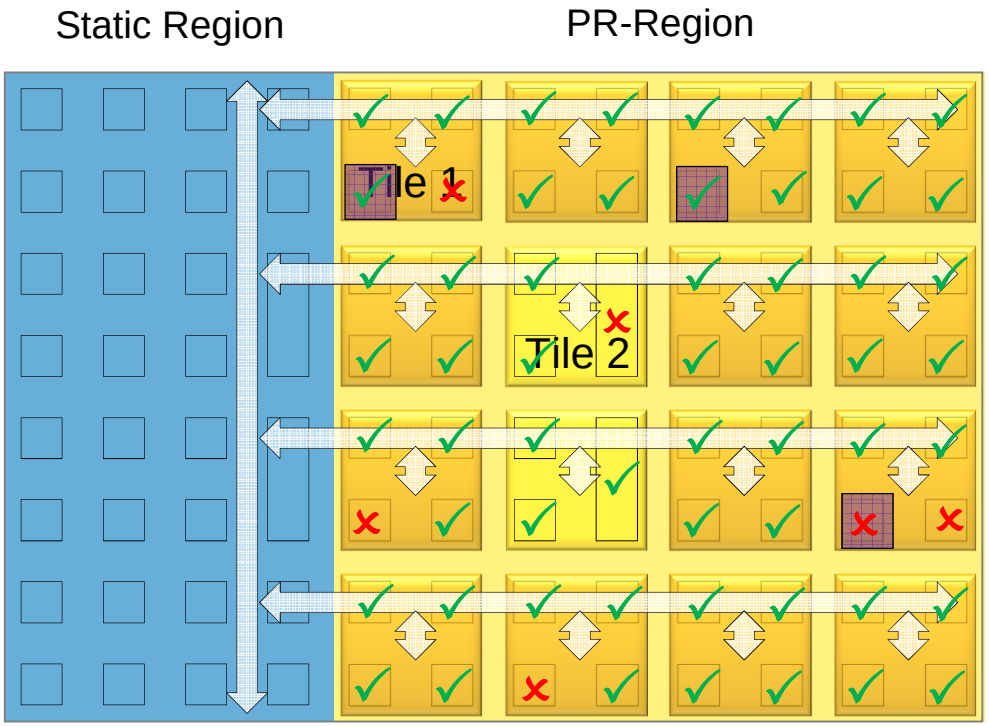
University of Pisa

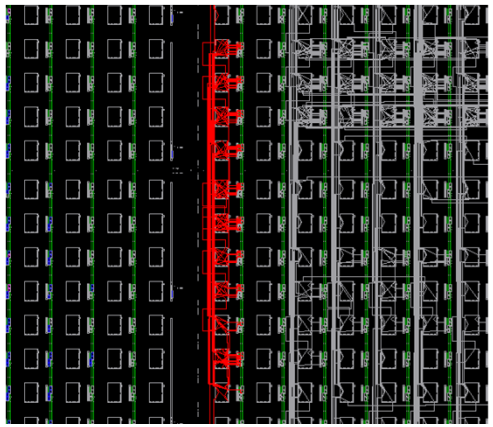
Politecnico di Torino

ITI A ongoing

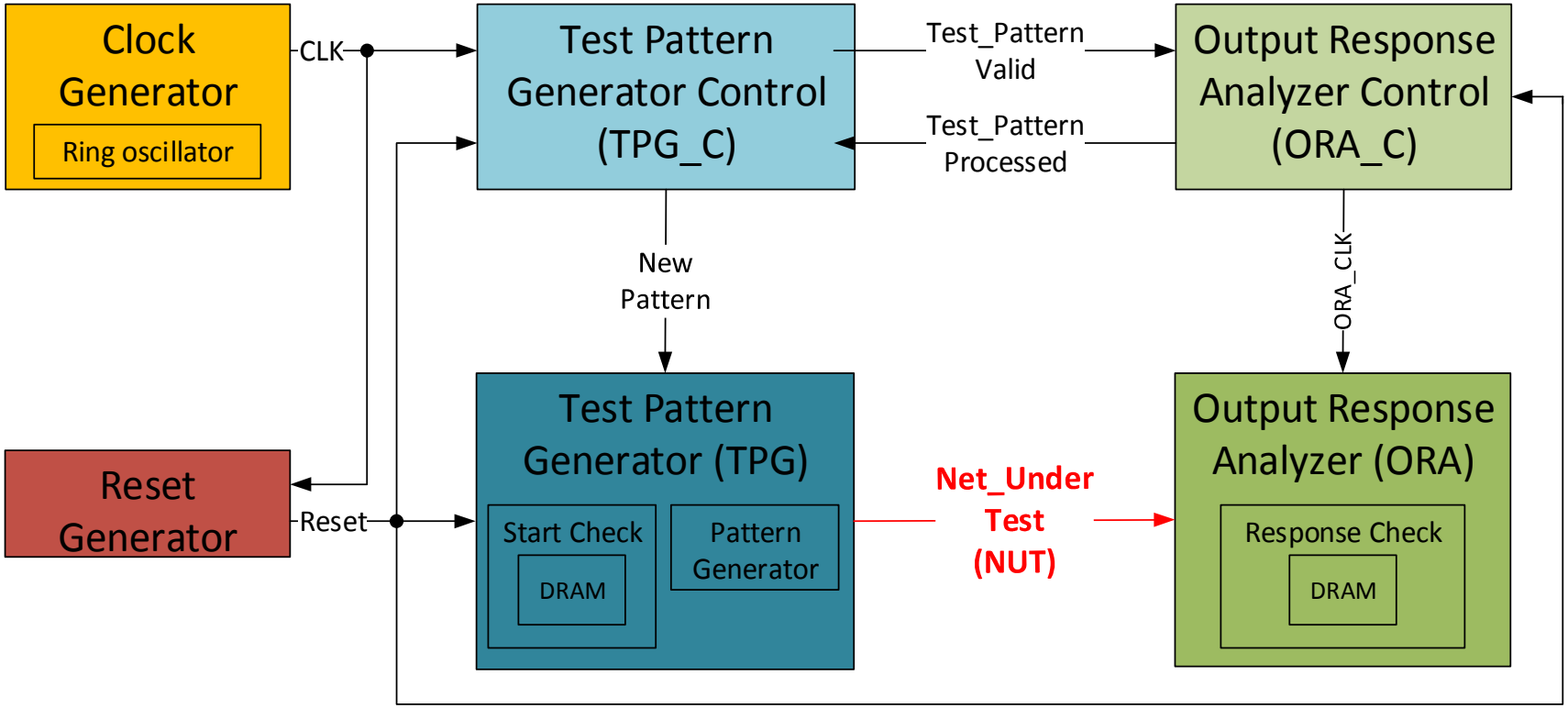
OLTRE - Online Testing and Patching Permanent Radiation Effects in Reconfigurable Systems

- Online testing of permanent radiation effects
- System stays operational during tests, ideal for runtime reconfigurable systems like the DRPM
- Hierarchically approach, coarse/fine grain testing
- Faulty resources are patched – all Tiles remain operational
- Self-contained testing macro – can be used without clock/reset/IO
- Runtime reconfiguration used to perform test/readback results
- Methodology can be extended to detect aging/degradation





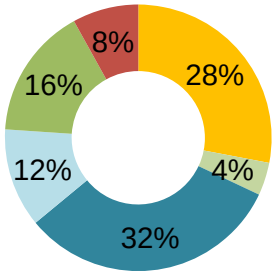
OLTRE – Testing Circuit



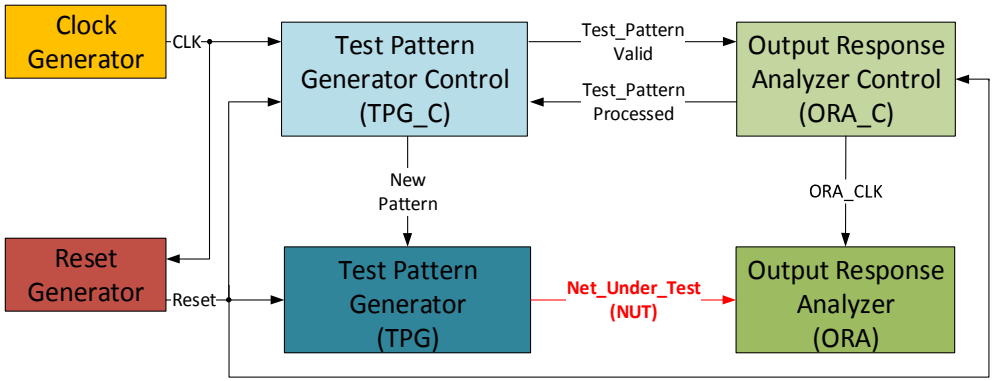
- IOB independent / self-contained circuit using ring oscillator
- Small FPGA resource footprint (~25 slices)
- Testing circuit is placed using dynamic partial reconfiguration
- Readback is used to evaluate results

OLTRE – FPGA Resource Usage

	Basic Testing Components (XC4VFX100)	SLICEs	REGs	LUTs	LUTRAM
8 NUT	Clock Generator	7	1	6	0
	Reset Generator	1	0	1	1
	Test Pattern Generator	8	4	6	1
	Test Pattern Generator Control	3	4	2	0
	Output Response Analyzer	4	0	4	2
	Output Response Analyzer Control	2	0	2	0
	Total	**25**	**9**	**21**	**4**



- Clock Generator
- Reset Generator
- Test Pattern Generator
- Test Pattern Generator Control
- Output Response Analyzer
- Output Response Analyzer Control

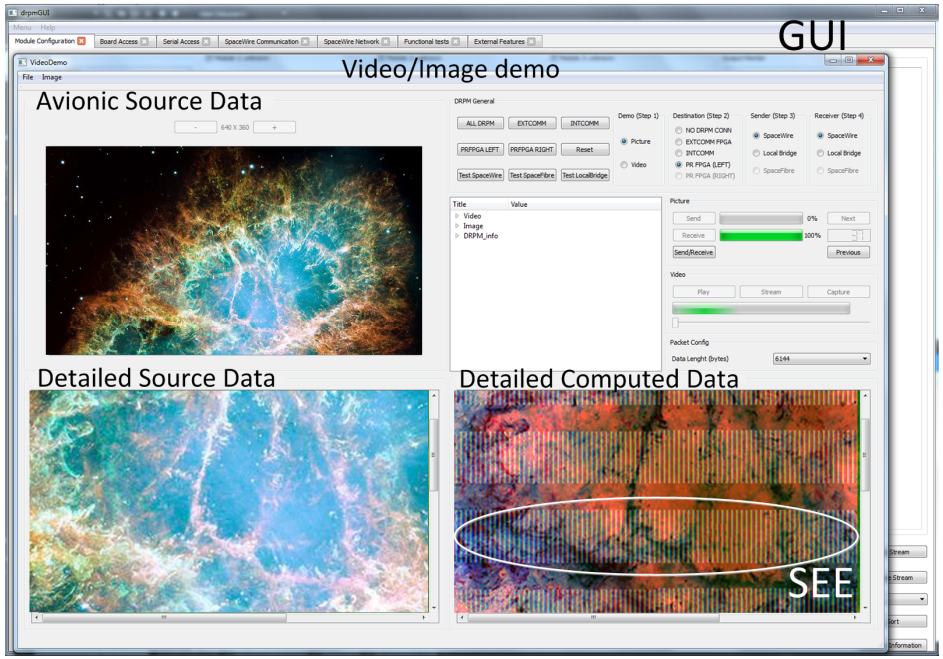


Publications

	Publication	Title
DRPM	SpaceWire Conference (**SpaceWire,** 2014)	AXI-based SpaceFibre IP Core Implementation
	Design & Technology of Integrated Systems (**DTIS**, 2014)	An Inter-Processor Communication Interface for Data-Flow Centric Heterogeneous Embedded Multiprocessor Systems
	Design, Automation &Test In Europe UBOOTH (**DATE**, 2014)	Leveraging dynamic reconfiguration to increase fault-tolerance in FPGA-based satellite systems
	IEEE Transactions on Computers Vol. 62 (**IEEE-TC**, 2013)	A Novel Fault Tolerant and Runtime Reconfigurable Platform for Satellite Payload Processing
	Military and Aerospace Programmable Logic Devices (**MAPLD**, 2013)	Dynamically Reconfigurable Hardware for Satellite Payload Processing
	Adaptive Hardware and Systems (**AHS**, 2012)	A Scalable Platform for Run-time Reconfigurable Satellite Payload Processing
	Field-Programmable Custom Computing Machines (**FCCM** 2011)	Automatic HDL-Based Generation of Homogeneous Hard Macros for FPGAs
	SpaceWire Conference (**SpaceWire,** 2010)	Implementation of a Dynamically Reconfigurable Processing Module for SpaceWire Networks
OLTRE	Defect and Fault Tolerance in VLSI and Nanotechnology Systems (**DFT**, 2014)	Exploiting Dynamic Partial Reconfiguration for On-Line On-Demand Testing of Permanent Faults in Reconfigurable Systems
	Military and Aerospace Programmable Logic Devices (**MAPLD**, 2013)	A CAD Flow for On-Line Testing and Patching Permanent Radiation Effects in Reconfigurable Systems
	Design, Automation &Test In Europe (**DATE**, 2013)	On-Line Testing of Permanent Radiation Effects in Reconfigurable Systems

DRPM – Demonstration

- Dynamically reconfigurable image processing
  - Change of filters at run-time
- Communication via SpaceWire/SpaceFibre
  - Processed image data
- Fault injection by partial dynamic reconfiguration
  - Bit-flip in configuration file leads to pixel-fault
- Fault is automatically corrected by self-hosting reconfiguration controller



Thank you for your attention!

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