Overview of the XRTC Single-Event Test Results on the Xilinx 7-Series FPGAs

Gary M. Swift
Swift Engineering and Radiation Services, LLC

Overview

- Introduction and Background
  - Comments on Commercial Parts Use in Space
  - Xilinx Radiation Test Consortium
- Four Recent Papers
  - E. Crabill (Xilinx) on SEM-IP at SELSE
    - × Available at: http://softerrors.info/selse/images/selse_2014/papers/selse_2014_13_paper.pdf
  - D.S.Lee (Sandia) on Kintex-7 SEE at NREC REDW
    - × Proceedings in press; preprints on request.
  - G.M.Swift (SwiftERS) K-7 Current Steps at MAPLD
  - Prof. M.Wirthlin (BYU) on CRAM MBU/MCUs at NSREC
    - × In review cycle for TNS Dec 2014

COTS in Space

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- "Right" reasons
  - Speed
  - Size
  - Power
  - More I/O
- WRONG Reason
  - Cost
  - Be prepared for lots of expensive testing and waiving requirements and operational difficulties

Xilinx Radiation Test Consortium

XRTC Setup Evolution

000 | 2001 | 2002 | 2003 | 2004 | 2005 | 2006 | 2007 | 2008 | 2009 | 2010 | 2011 | 2

Virtex-2

Virtex-IIpro

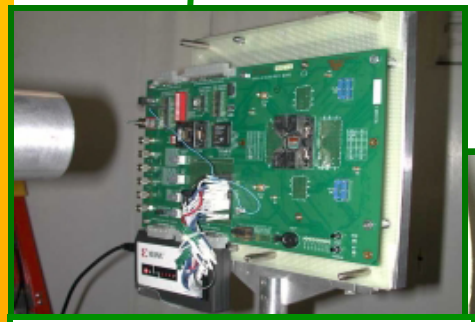
Virtex-4

Virtex-5

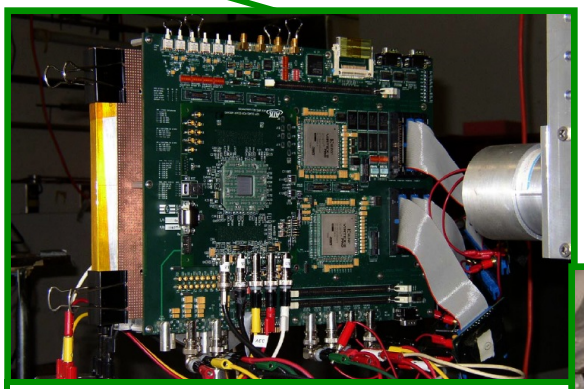
JPL & Xilinx partner up

Consortium formation

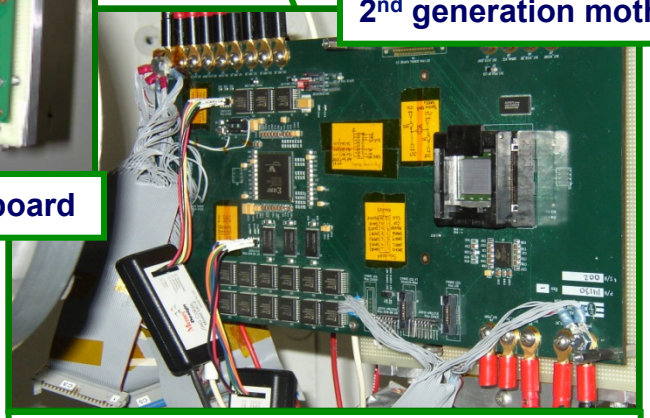
1st Annual Meeting



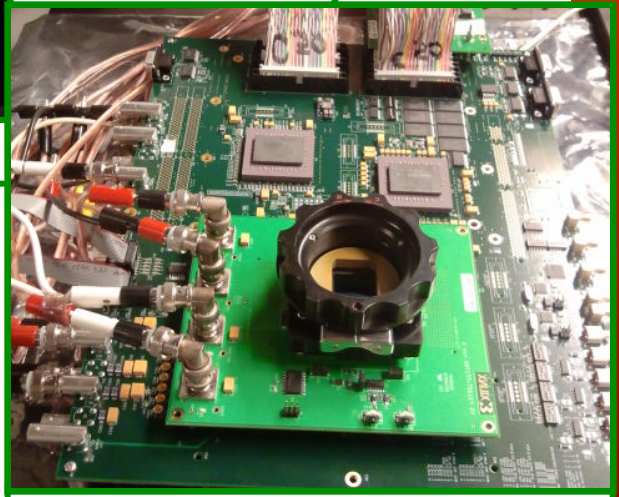
0th generation motherboard



2nd generation motherboard



1st generation motherboard



3rd generation motherboard

Upset Results Overview

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- Configuration Upsets
  less than 100 per day
- BRAM Upsets (100% use)
  less than 50 per day
- Flip-flop Upsets (100% use)
  less than 1 per week

Investigation of High Current Events in 28nm 7-Series FPGAs

Gary M. Swift
Swift Engineering and Radiation Services, LLC

Overview

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- Introduction
  - DUT - 7-Series
  - Review of Latchup Basics
- Test Setup
- Observed: Single-event Current Steps ???
- Possible Explanations
- Working Hypothesis:

  Latchup with Significant Series Resistance
- Mitigation Ideas and Future Work

7 Series Xilinx FPGAs

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- Current generation is 28 nm, TSMC process

- Four families
  - Artix – high volume FPGA
  - Kintex – mid-range FPGA
  - Virtex – high performance FPGA
  - Zynq – high-performance dual ARM processors
    plus large FPGA fabric and I/Os

Latchup Basics

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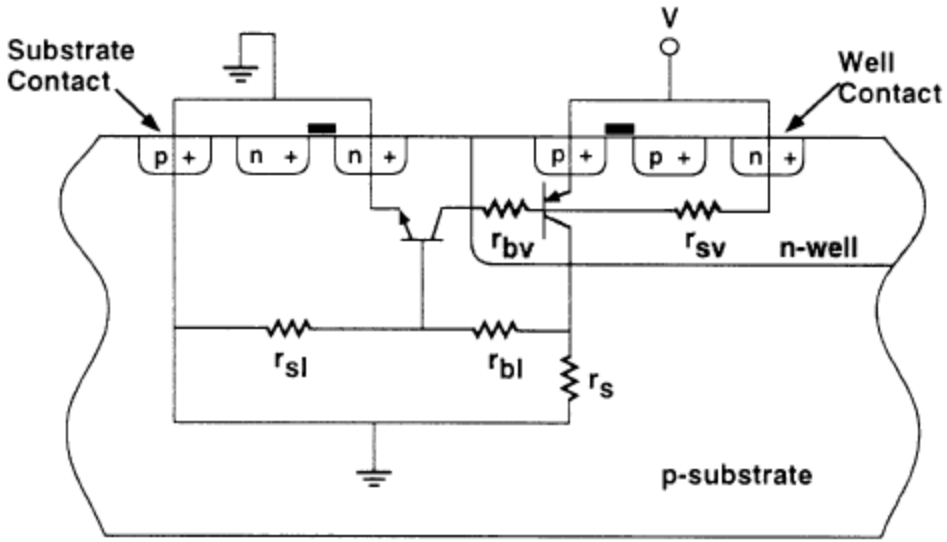
- SCR-like action, due to parasitic bipolar transistors
- All CMOS inherently susceptible
- Can be suppressed by reducing carrier lifetime
- May be destructive or cause latent damage (or not)

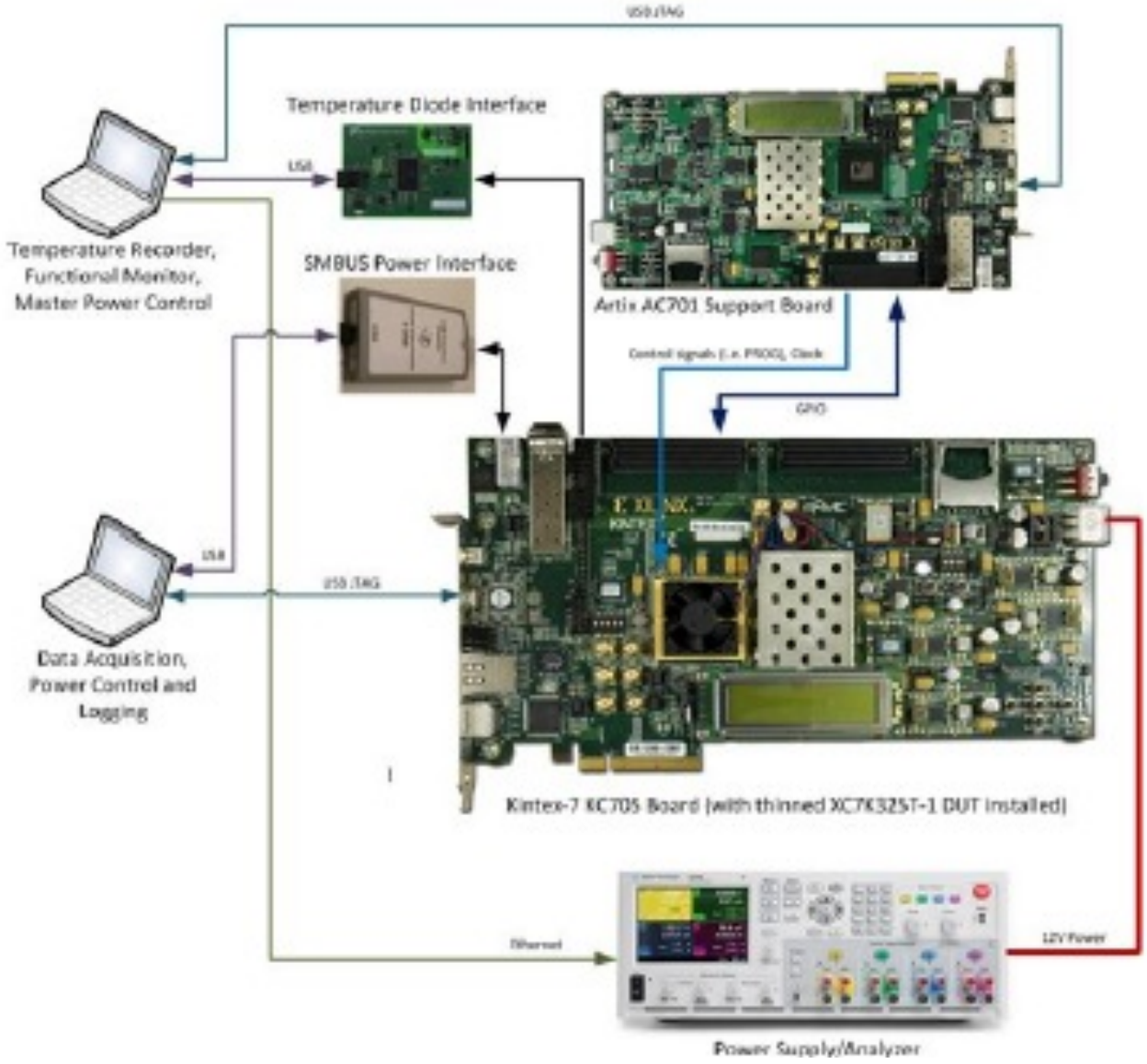
Latchup's I-V Characteristics

Gain of two transistors > 1 causes regenerative feedback resulting in runaway current

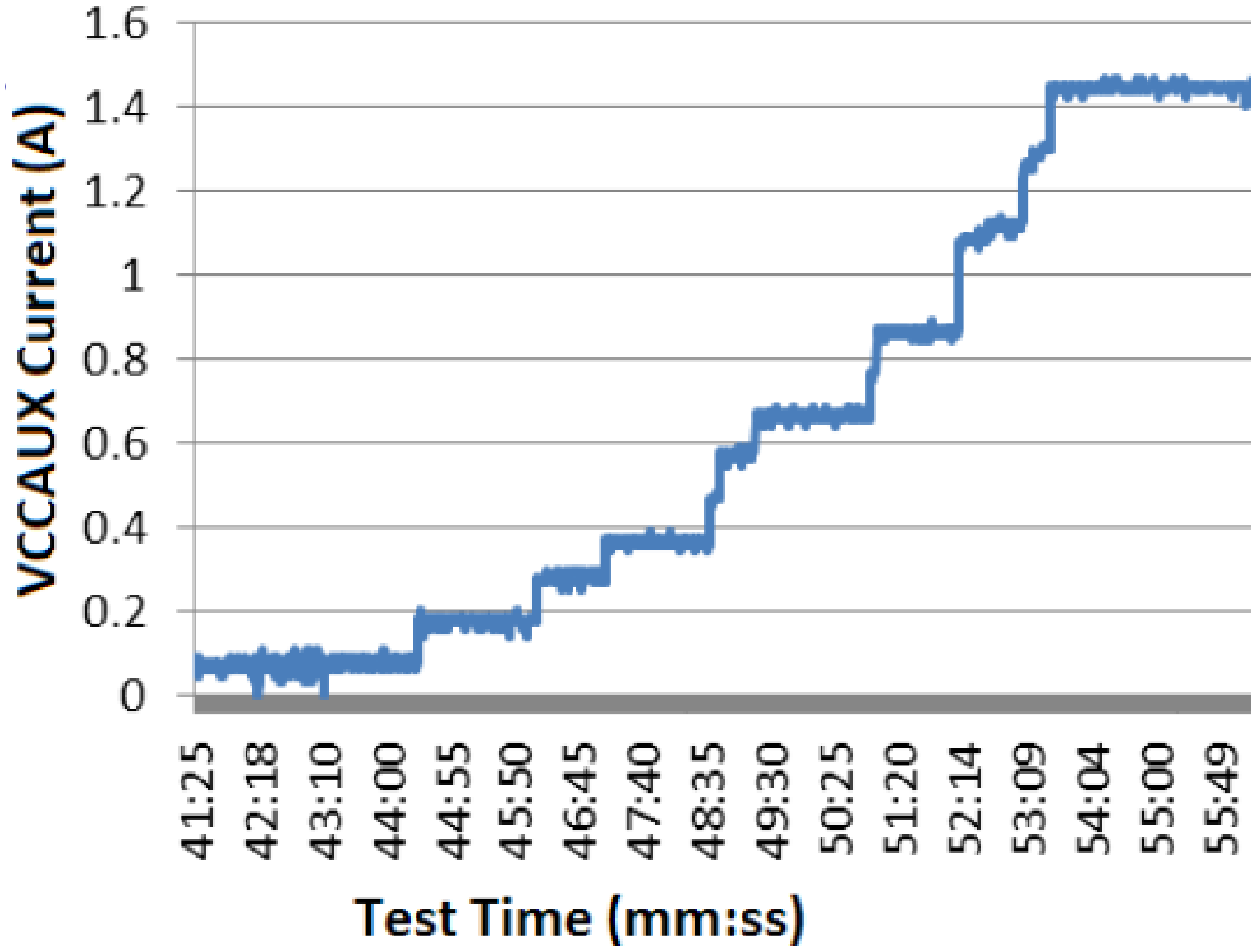
In latchup, lowering the voltage lowers transistor gain; below "holding voltage" gain < 1 releasing the latchup



Test Setup


USB
Temperature Diode Interface
USB
Temperature Recorder,
Functional Monitor,
Master Power Control
SMBUS Power Interface
Artix AC701 Support Board
GPIO
USB
USB JTAG
Data Acquisition,
Power Control and
Logging
Kintex-7 KC705 Board (with thinned XC7K325T-1 DUT installed)
Ethernet
12V Power
Power Supply/Analyzer

Current Steps on Vaux



Observed Characteristics

- No functional problems observed
- What restores nominal current?
  - ✗ Resetting user circuit does not
  - ✗ Scrubbing configuration does not
  - ✗ Reconfiguring device does not
  - ✓ Power cycle does
- Distribution of current step sizes*
  - 105 mA average, 25 mA std.deviation at room temp.
  - 125 mA average, 40 mA std.dev at elevated temp.
- Higher cross section at high temperature

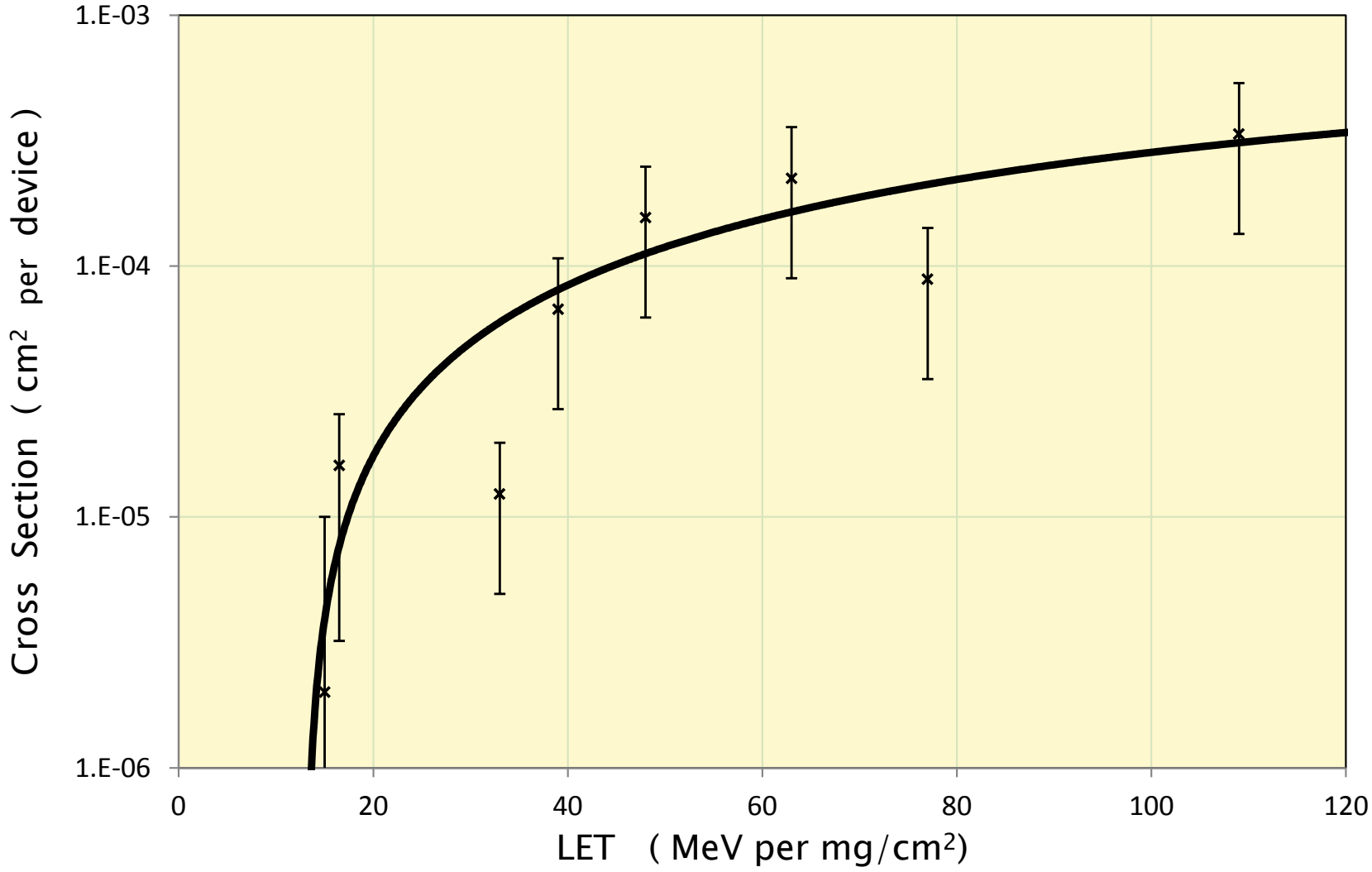
* Baseline is 80 mA and 210 mA for the two test designs used

Powered by Vaux = 1.8V

Vaux powers “mfg” level misc’l functions

- Configuration engine
- Efuse programming
- XADC (previous name: ‘system monitor’)
- I/O pin optional function(s)
  - .
  - .
  - .

Measured Susceptibility



Is it latchup?

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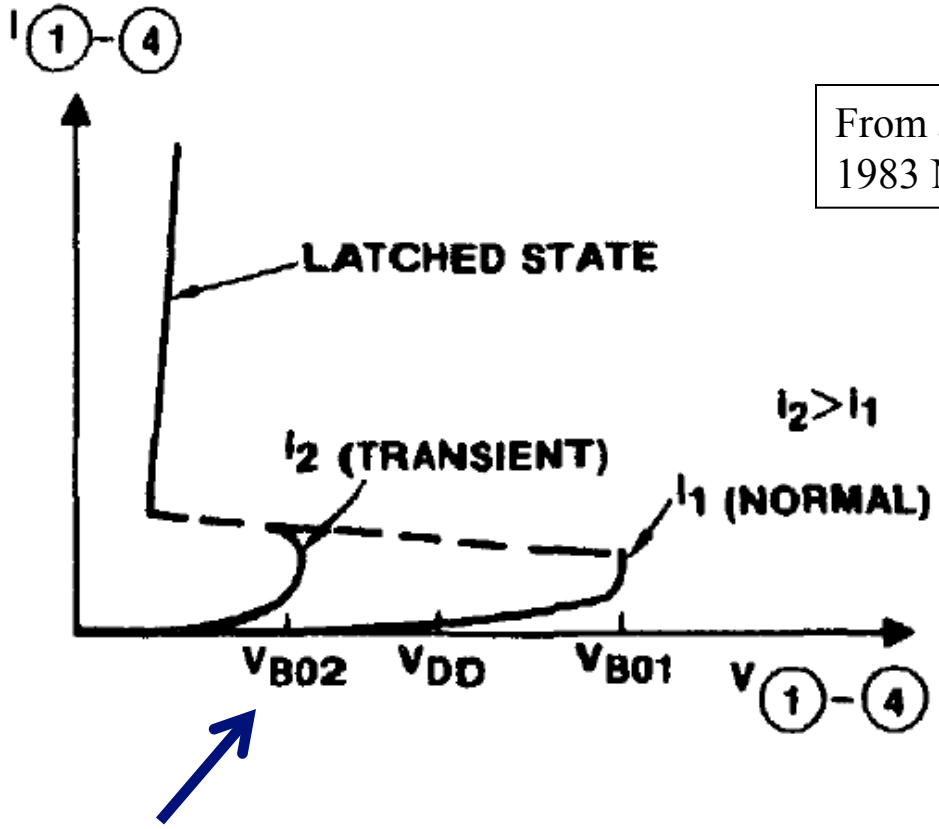
- ✗ No functional problem observed
- ✓ Only fix is power cycle
- ✗ Current step size, roughly 100 mA
  - Note this implies 18 ohms impedance
- ✓ Worse at elevated temperature

What else can it be?

- Upset-induced internal contention
  - ✘ Current too big
  - ✘ Typical contention current is < 0.5 mA
- Dielectric Rupture
  - ✘ Power cycle restores nominal current
- Snapback
  - ?

Additional Experiment

Current steps exhibit a holding voltage signature



From J. Pickell,
1983 NSREC Short Course Notes

Holding voltage is between 1.20V and 1.25V

What are current steps ??

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- Working hypothesis –

  Latchup with series impedance

- More questions –
  - What's acting as the current limiting resistor ?
  - Where are the high current sites on the die ?
  - What circuit function(s) is/are involved ?
  - Is this the mythical creature: micro-latchup ?

  Most important of all:
  - How to prove it's non-destructive, non-damaging

Results Update

NASA/Goddard confirms they've seen these current steps

- The XADC block is likely culprit, Melanie Berg hypothesized

New XRTC test results from Berkeley (6/20/14) show XADC is not a source of these single-event current steps

- With separated XADC power from Vaux,
  - × Current steps are only observed on Vaux
- With XADC turned off via control bit and powered with 0.7 V (well below the holding voltage),
  - × The measured cross section did not change at LET=41
    - – 20 events vs. 21 events for fluence of 6.0×10^5 / cm^2

JPL test results from Indiana (July 2014) with

200 MeV protons: NO proton-induced current steps.

Possible Future Work

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- Localize structure involved
  - In-situ, thorough electrical “wring-out” test
  - Collimators (millimeter resolution)
  - Infra-red camera (ten micrometer resolution)
  - Micro-beam (few micrometer resolution)
  - Laser (micrometer resolution)
- Pursue damage questions
  - Do irradiated DUTs pass full production test ?
  - What’s the current density? Is it capable of producing damage?
  - Do irradiated DUTs pass accelerated life testing?

Implications

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If it is low-current latchup,

- Any SEL is scary to fly, but
  - × The rate's really low (GEO: 1 in 5-20 years)
  - × No obvious functionality problems or damage
- Mitigation options (though not very attractive)
  - × Running with Vaux below spec. min. reduces rate
  - × Minimizing time in SEL lowers damage risk
  - × Test neutron irradiated part
- Proving non-destructiveness is very difficult

Further investigation is needed