Results of Heavy-Ion Broad and Micro Beam Testing of Flash Based FPGAs

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Radiation Testing

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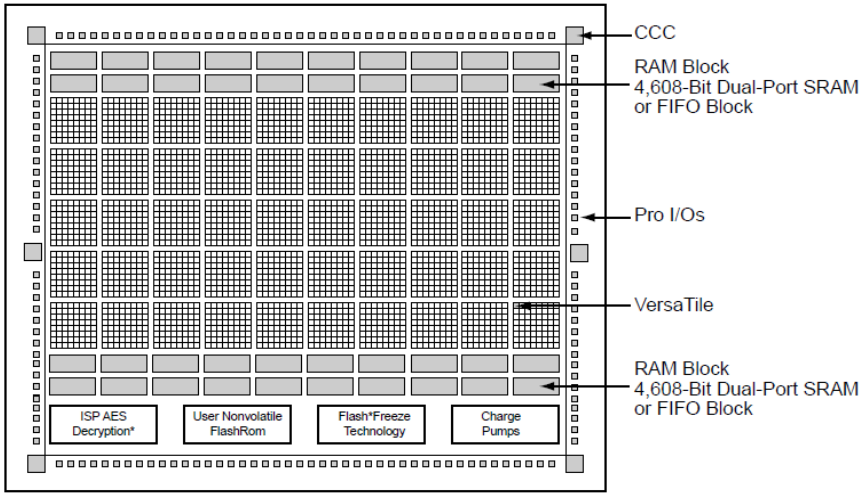
Outline

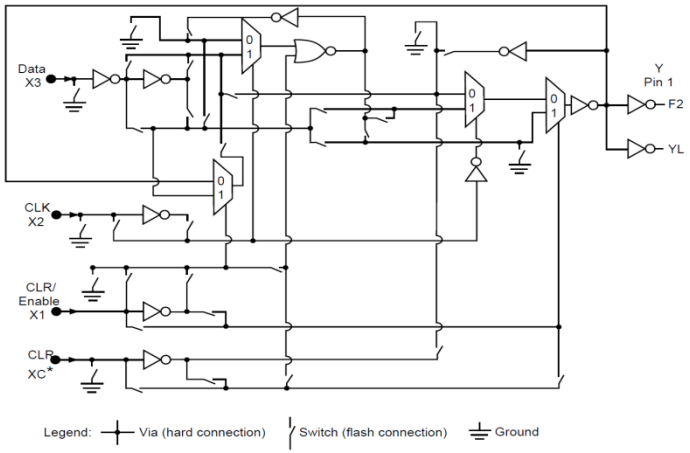
- Background – ProASIC3L, SETs
- SET Measurement Techniques
- Results of Heavy Ion (HI) SET measurements (UCL)
- HI Micro Beam Setup (GSI)
- Results of Micro Beam Testing
- Permanent Effects
- Conclusions and Future Work

Background - ProASIC3L, SETs

MicroSemi ProASIC3L

	A3PE3000L
Core Voltage (V)	1.2 .. 1.5
Technology	130nm, 7ML
VeraTiles	75 264
4608 bit BRAMS	112
CCC (including PLL)	6
VersaNet Globals	18





VersaTile

One VersaTile can implement:

- Any 3 input combinatorial function
- A DFF or latch with options for preset, clear, enable
- Configuration is controlled by floating gate switch

Single Event Transients (SETs)

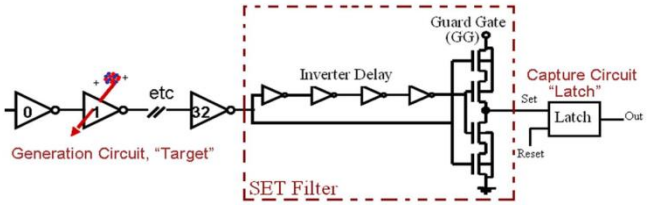
- Upsets in combinatorial logic (VersaTiles)
- Characterization requires :
  - Measuring rate of occurrence
  - *Distribution* of pulse widths
- Function of :
  - VersaTile configuration (AND,OR, XOR, MAJ,…)
  - Input state
  - Voltage, Temperature
- SETs in flash based FPGAs have been extensively studied [1..7]
  - New contributions : finer temporal resolution and complex circuits

[1] S. Rezgui, et al., “New methodologies for set characterization and mitigation in flash Based FPGAs,” TNS’07, vol. 54, no. 6.
[2] S. Rezgui, et al., “Configuration and routing effects on the set propagation in flash-based fpgas,” TNS’08, vol. 55, no.6.
[3] C. Poivey, et al., “Radiation characterization of Microsemi Proasic3 flash FPGA Family,” REDW , 2011.
[4] N. Battezzati, et al., “Analysis of SET Propagation in Flash-based FPGAs by means of electrical pulse injection,” RADECs 2009.
[5] M. D. Berg, et al., “A comprehensive methodology for complex FPGA SEE Evaluation,” TNS’09, vol. 56.
[6] L. Sterpone,et al. “Analysis of SET Propagation in flash-based FPGA by means of electrical pulse injection,” TNS’10, vol. 57.
[7] L. Sterpone, et al., “An Analytical Model of PIPB on SETs in flash-based FPGAs,” TNS’11, vol. 58.

SET Measurement Techniques

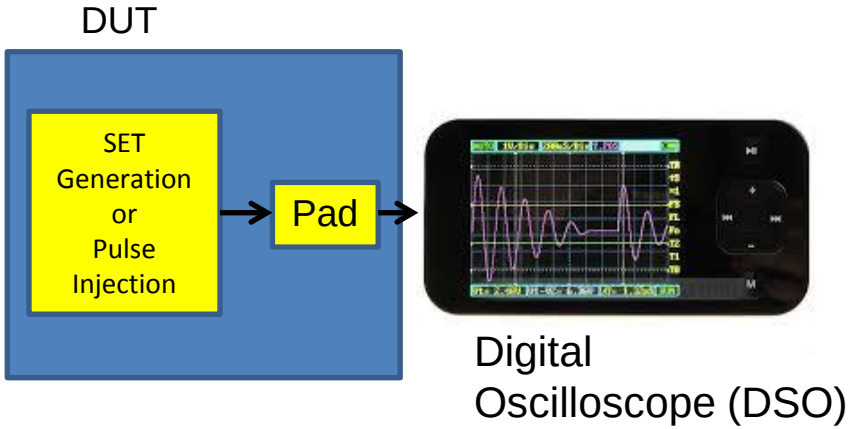
Existing SET Measurement Techniques

➢ Pulse Filter [1,2]



- ➢ Requires multiple filters to characterize pulse width distribution
- ➢ Subject to on-chip delay variation (voltage, variability, etc.)
- ➢ Resolution limited to 1 gate delay

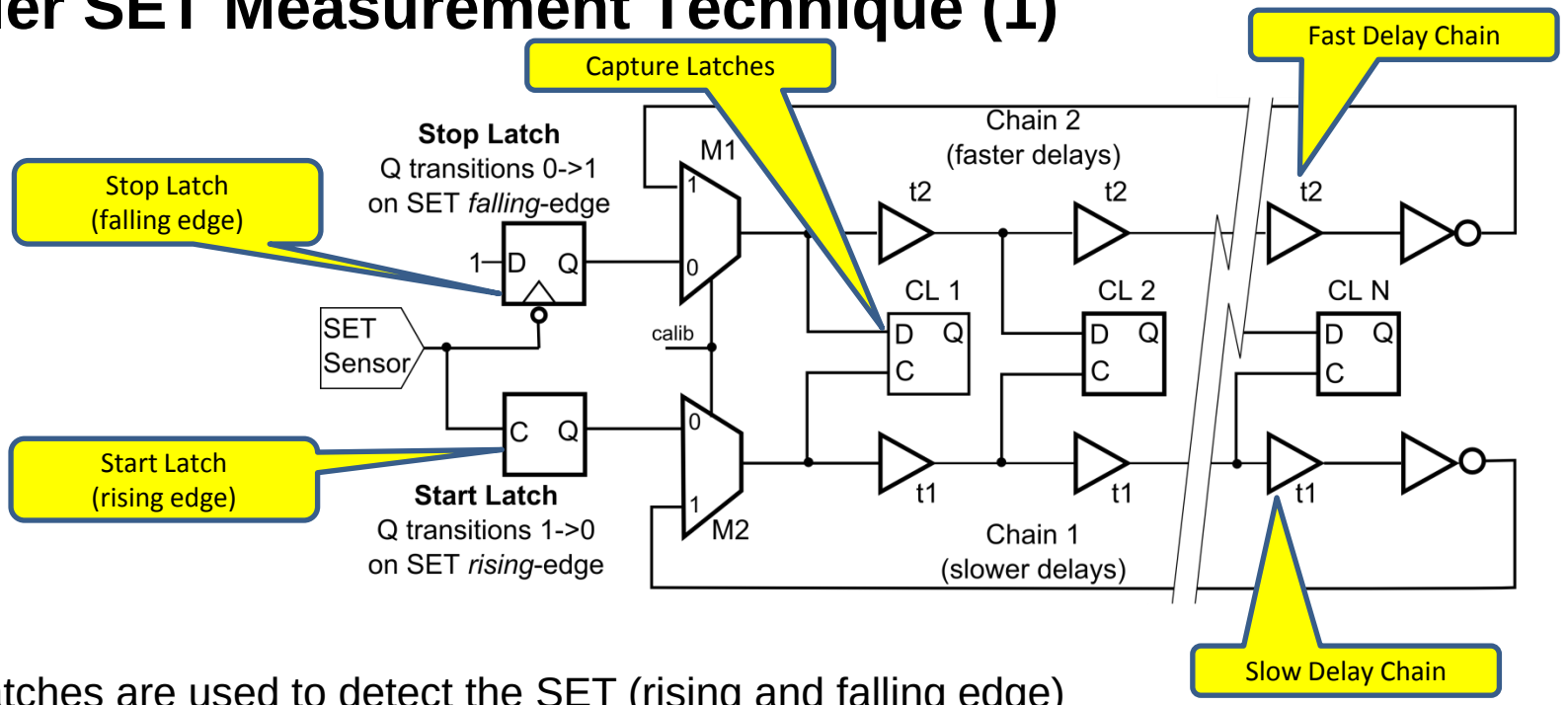
➢ Off-chip measurement [3]



- ➢ Subject to bandwidth of IO pads
- ➢ Number of observations limited by available channels on DSO

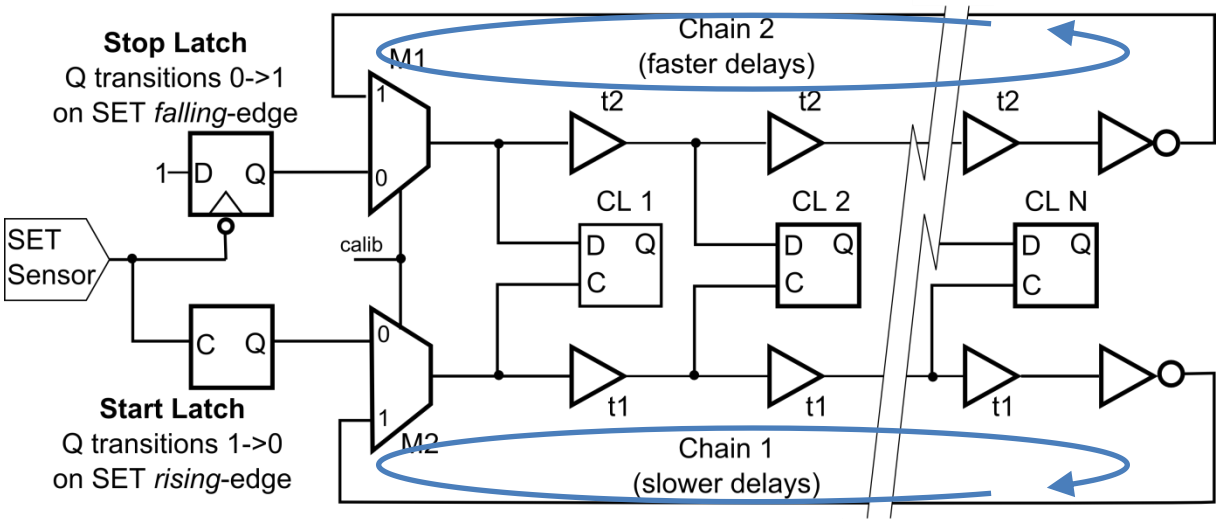
[1] S. Rezgui et al., "New methodologies for set characterization and mitigation in flash Based FPGAs," TNS'07, vol. 54, no. 6.
[2] S. Rezgui et al., "Configuration and routing effects on the set propagation in flash-based fpgas," TNS'08, vol. 55, no.6.
[3] L. Sterpone et al., "Analysis of SET Propagation in Flash_based FPGAs by means of Electrical Pulse Injection," TNS'10, vol. 57, no.4

Vernier SET Measurement Technique (1)



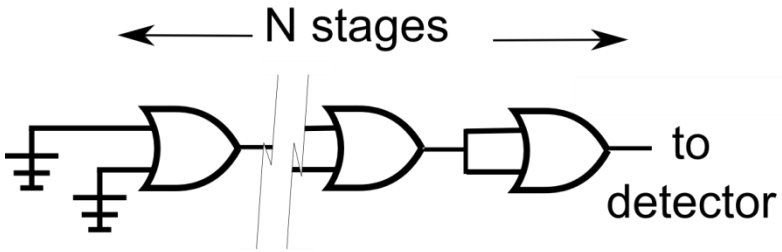
- Two latches are used to detect the SET (rising and falling edge)
- Exploit the difference in delay along two chains for finer delay resolution
- "Slow" delay chain (t1)
  - Triggered by rising (leading) edge of the transient
  - Feeds data input of transparent capture latches
- "Fast" delay chain (t2)
  - Triggered by falling (trailing) edge of the transient
  - Feeds clock input of transparent capture latches
- At each stage, the trailing edge catches up by (t2-t1) units of time
- After a number of stages equal to PW / (t1-t2), the edges cross

Vernier SET Measurement Technique (2)

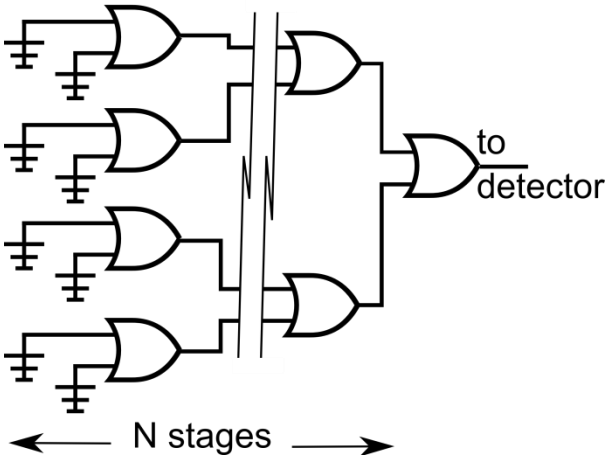


- Detector was designed with :
  - t1 ≈ 780 ps (AO1 VersaTile)
  - t2 ≈ 640 ps (BUF VersaTile)
  - 36 stages
  - ≈ 140 ps delay resolution ; ≈ 5 ns maximum transient detection
  - Placement all done by “hand” (TcL scripts)
- The detector is SEE robust
  - A valid event occurs only if both start and stop latches are triggered
  - The capture latches are normally open – not immune to upsets
- Delays are calibrated prior to radiation testing
  - Each delay chain can be configured as a ring-oscillator and the frequency is measured

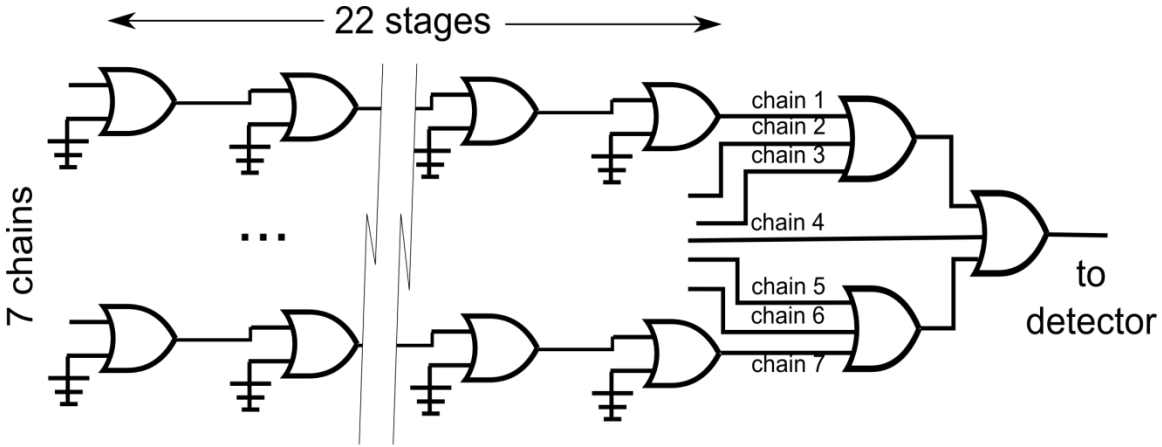
SET Sensors (3 Topologies)



Simple Chain of Gates

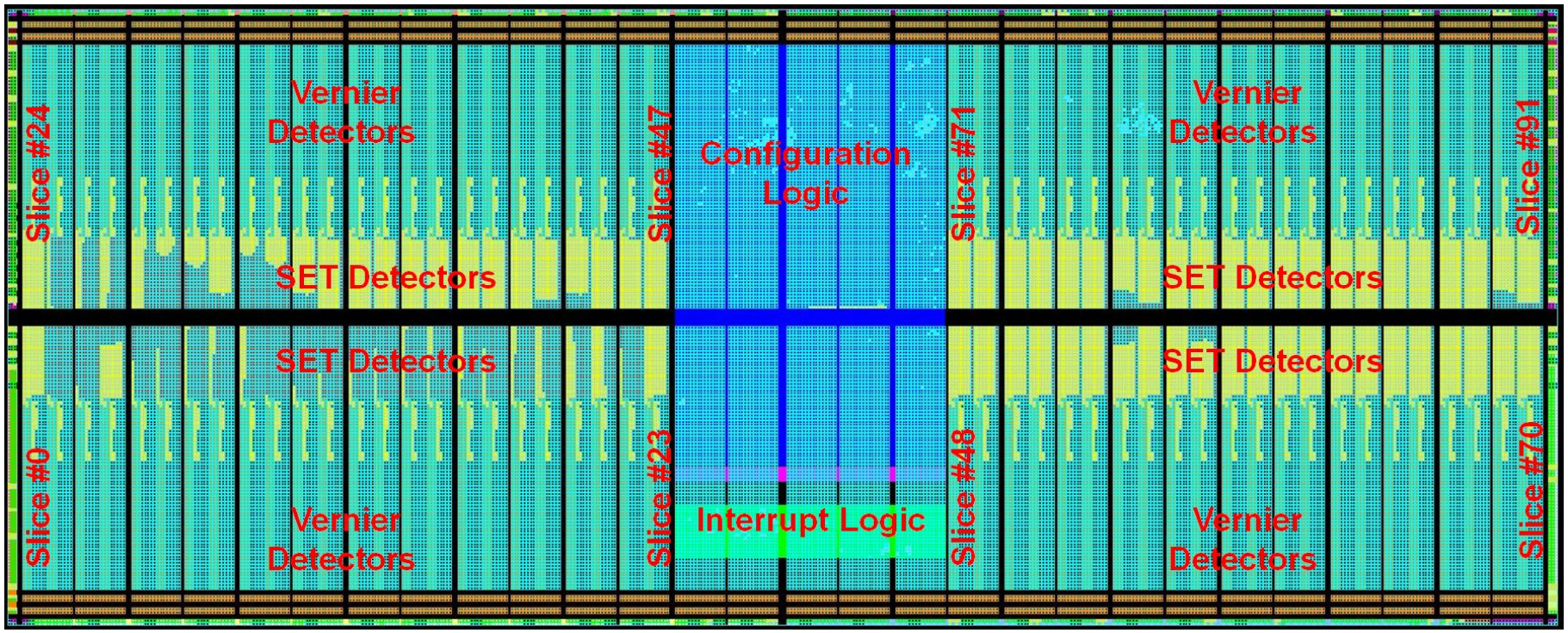


Tree Topology



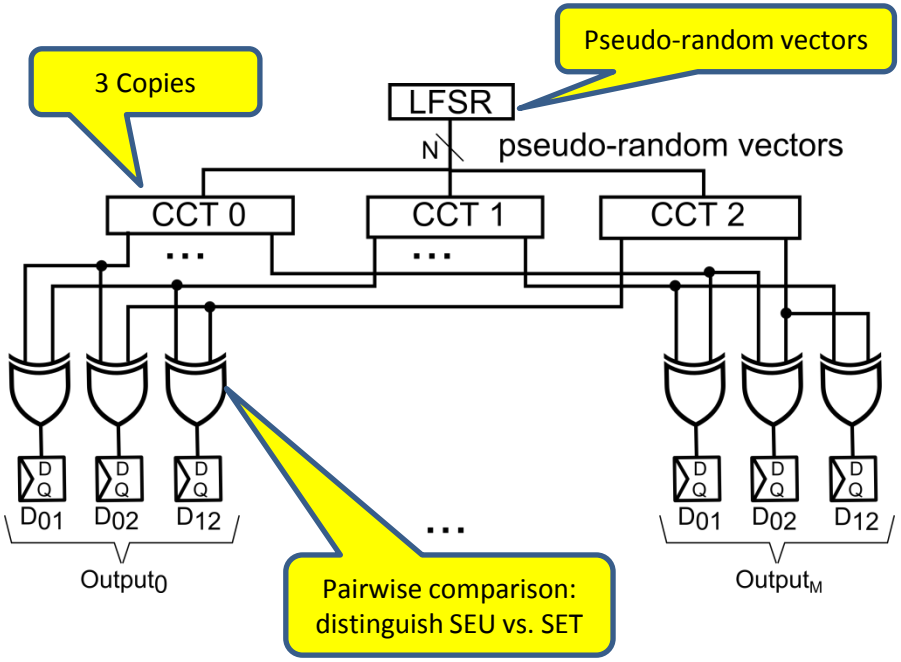
Multiple Parallel Chains

Full Device Under Test (DUT)



- In total 92 different detectors integrated into one A3P3000L
- Configuration logic and interrupt logic (DMR/TMR) used to multiplex detectors and report events

SETs in Clocked Circuits

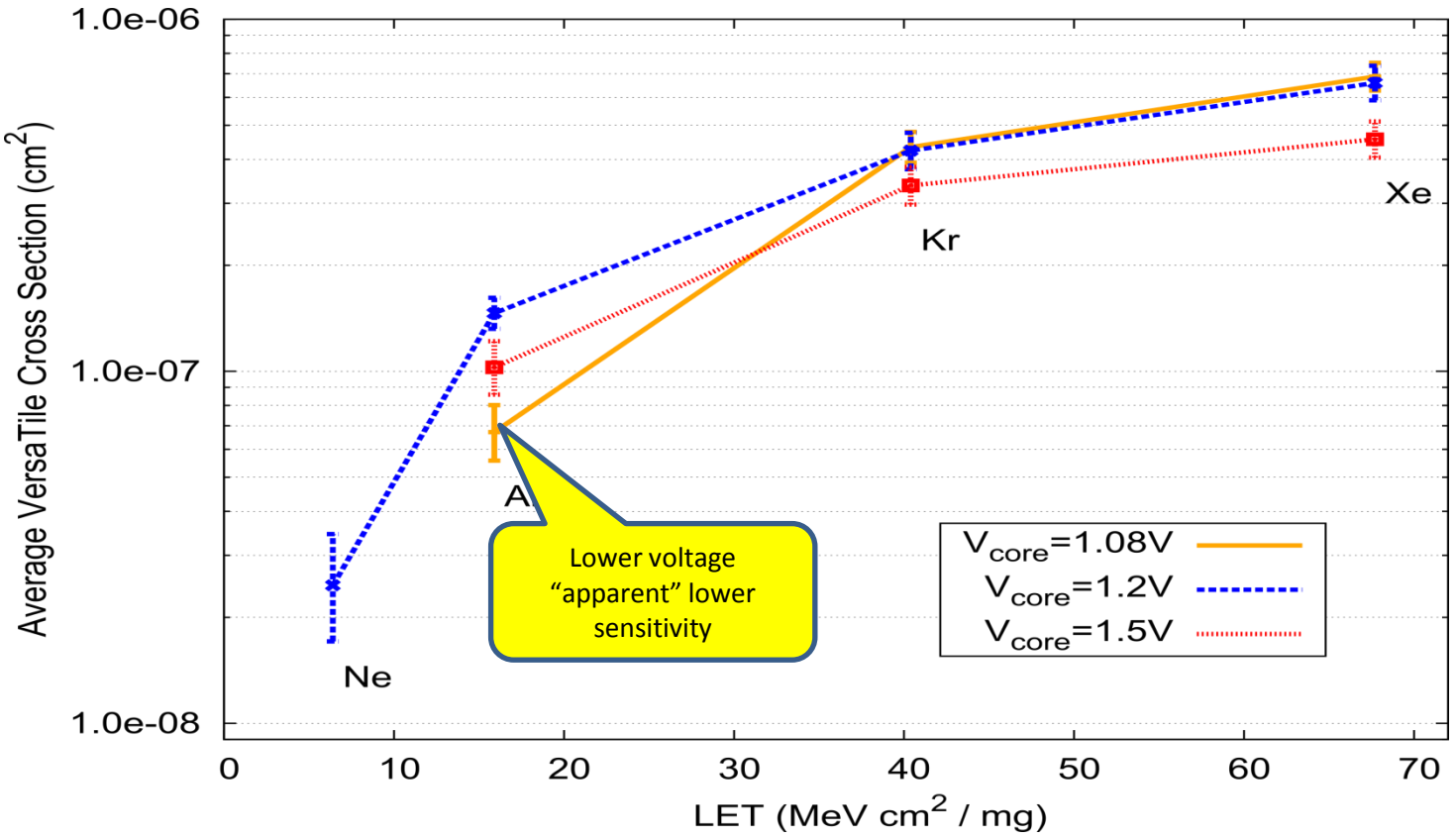


Combinatorial Network	PI / PO / VersaTiles
16-bit CLA Adder	33 / 17 / 136
32-bit priority encoder	32 / 6 / 76
State machine logic	25 / 12 / 63
4-bit, 8:1 MUX	35 /4 / 28
16-bit Hamming ECC Encoder	16 / 5 / 20
16-bit Hamming ECC Decoder	21 / 16 /60

- Objective is to measure SETs in clocked circuits (50 MHz)
- Study commonly used combo circuits (adders, state-machine…)
- Differentiate between SEUs and SETs
- SEU={001,010,100} ; SET={110,101,011}
- Measures “effective” impact of SET (post temporal, logical masking)

Broad Beam HI Test Results (UCL)

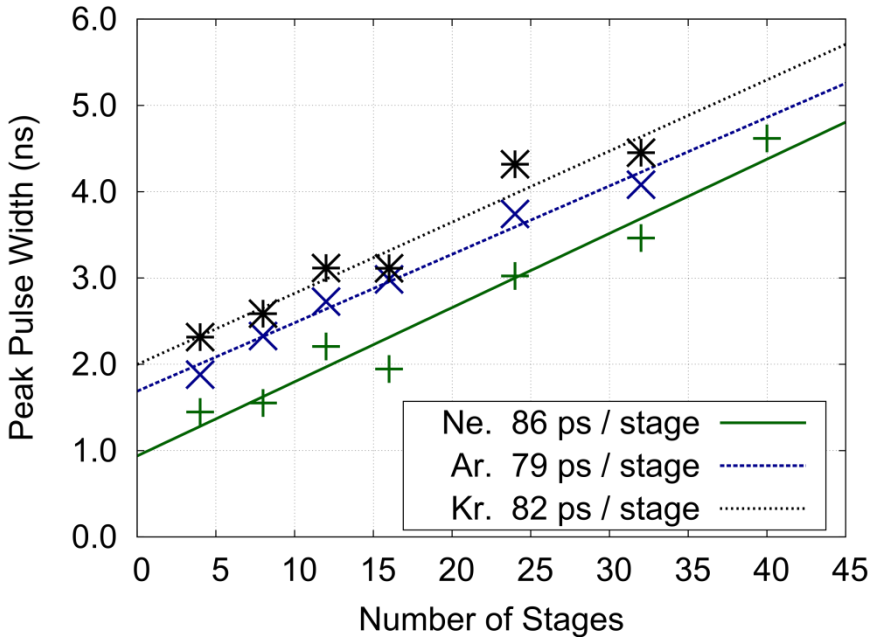
Voltage and LET



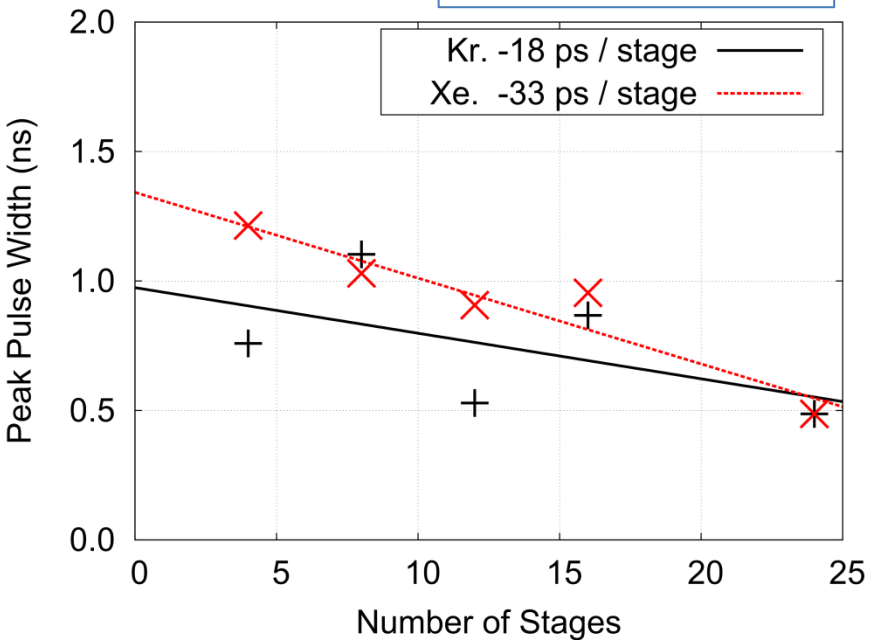
- SETs are observed even at low LET (6.4 MeV * cm^2 / mg)
- SET sensitivity reduces with higher voltage
- At lower voltage (1.08V) increased t_{setup},t_{hold} reduces detector sensitivity

Pulse Broadening / Narrowing

Ne : 6.4 MeV cm^2/mg
Ar : 16 MeV cm^2/mg
Kr : 40 MeV cm^2/mg



Broadening – BUF (0->1)



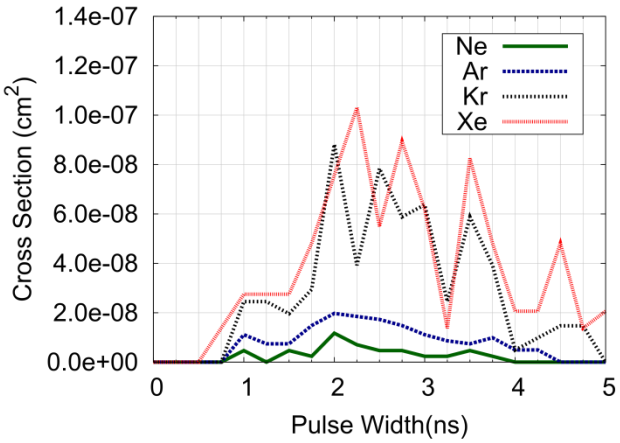
Narrowing – BUF (1->0)

- Pulse broadening[1,2] was studied using gate chains of different length
- In BUF VersaTiles, positive (0->1) transients are broadened and negative (1->0) transients are reduced in width

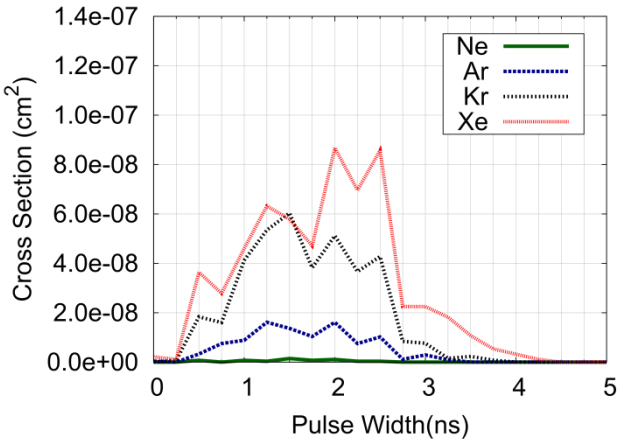
[1] V. Ferlet-Cavrois, et. al, “New insights into SET Propagation in Chains of Inverters; Evidence for PIPB,” TNS’07, vol. 54.
[2] V. Ferlet-Cavrois, et al., “Investigation of the PIPB effect on SET in SOI and bulk inverter chains,” TNS’08, vol. 55.

Variation Between VersaTiles

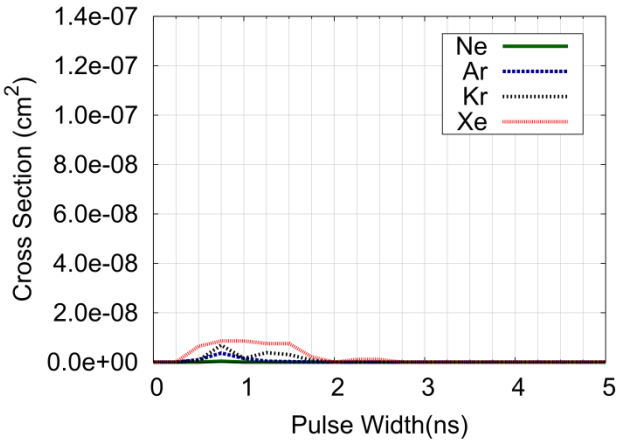
Ne : 6.4 MeV cm^2/mg
Ar : 16 MeV cm^2/mg
Kr : 40 MeV cm^2/mg



OR2
IN = 00



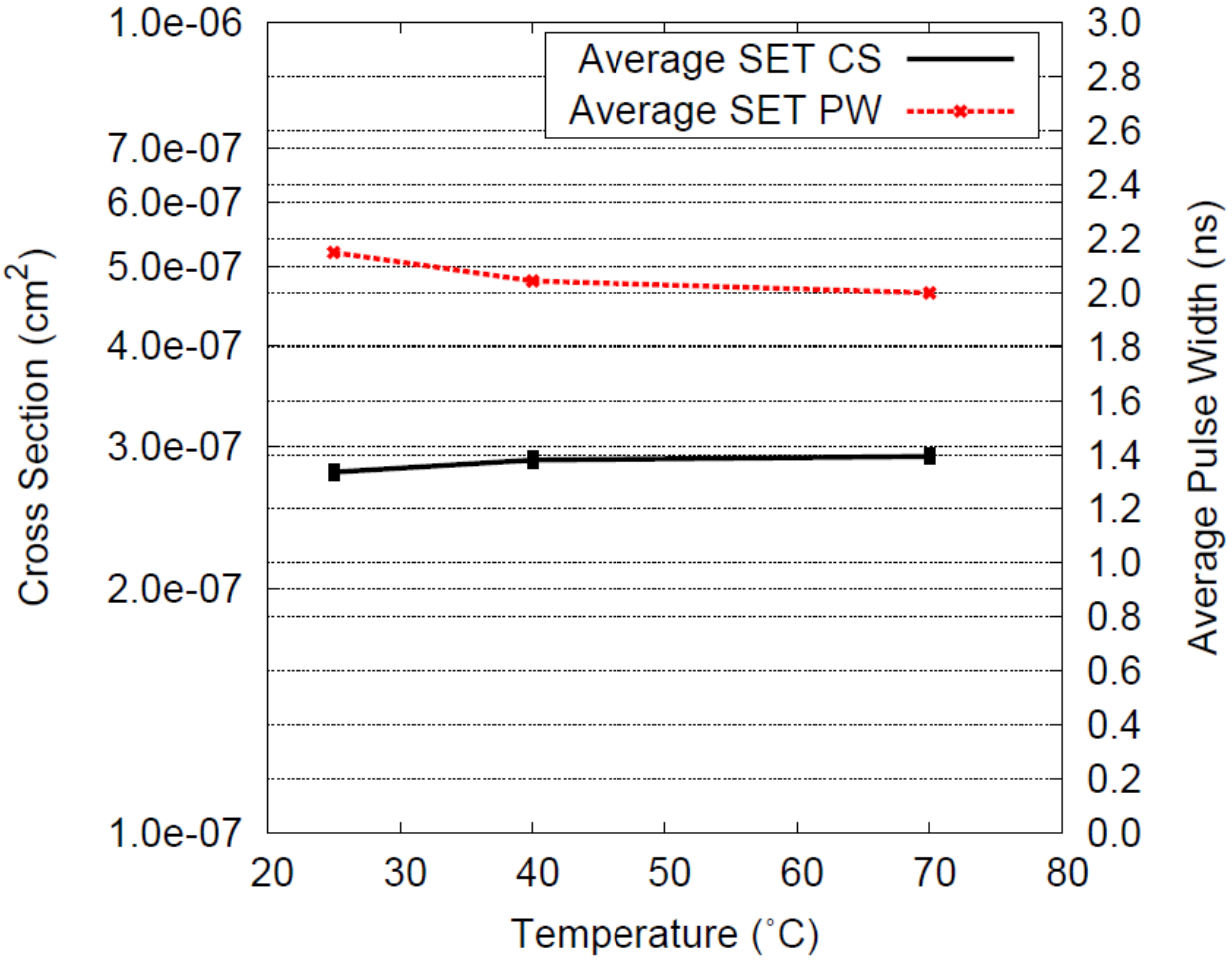
MAJ3
IN = 100



MAJ3
IN = 110

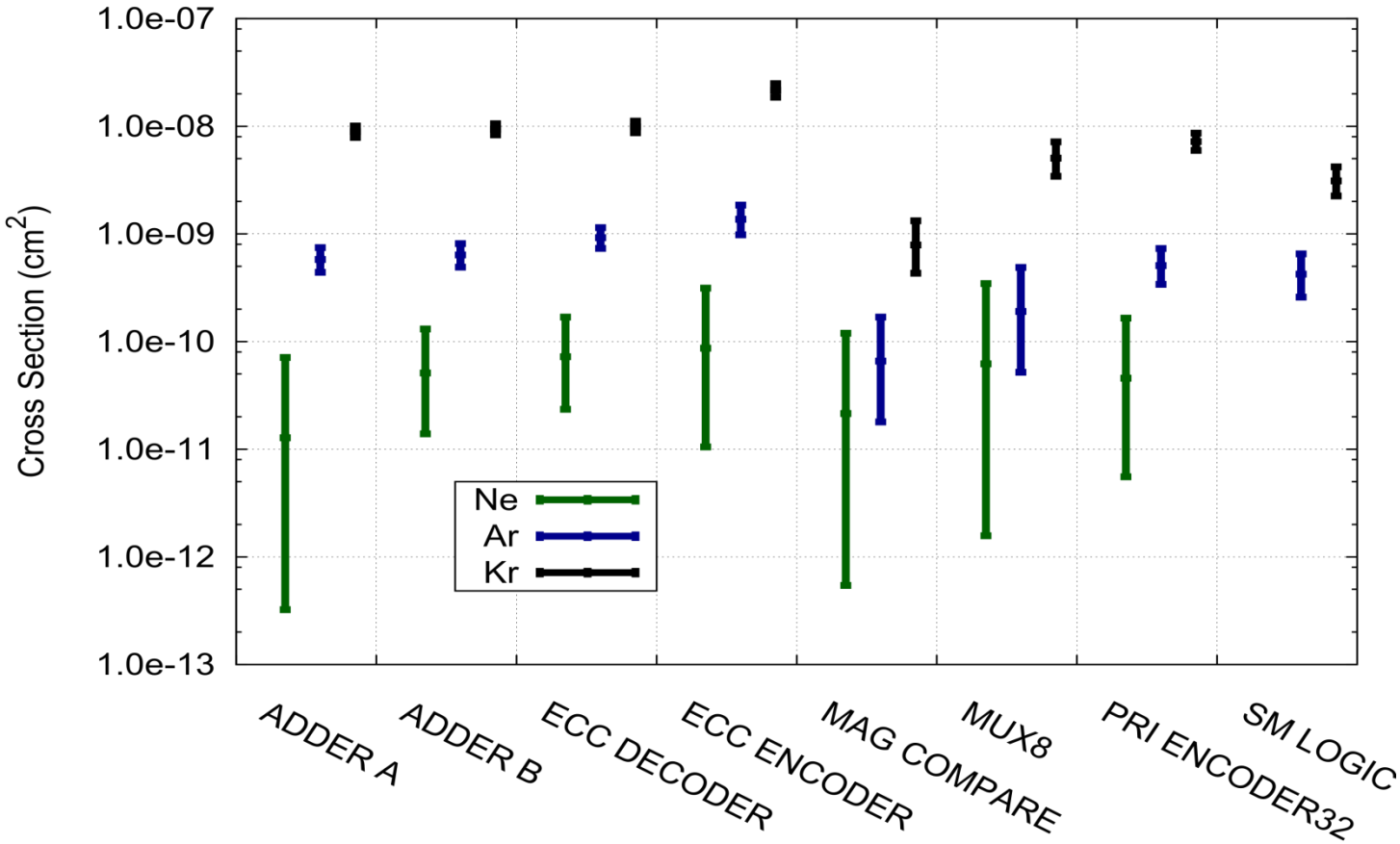
- Characterization of a VersaTile presented as Cross Section (CS) versus pulse width
- Measurement occurs at the output of detector chain (7x22 cells)
  - Measured pulse subject to broadening / narrowing
- Significant variation based on input state

Temperature Effect



- Little sensitivity in cross section or pulse width versus temperature

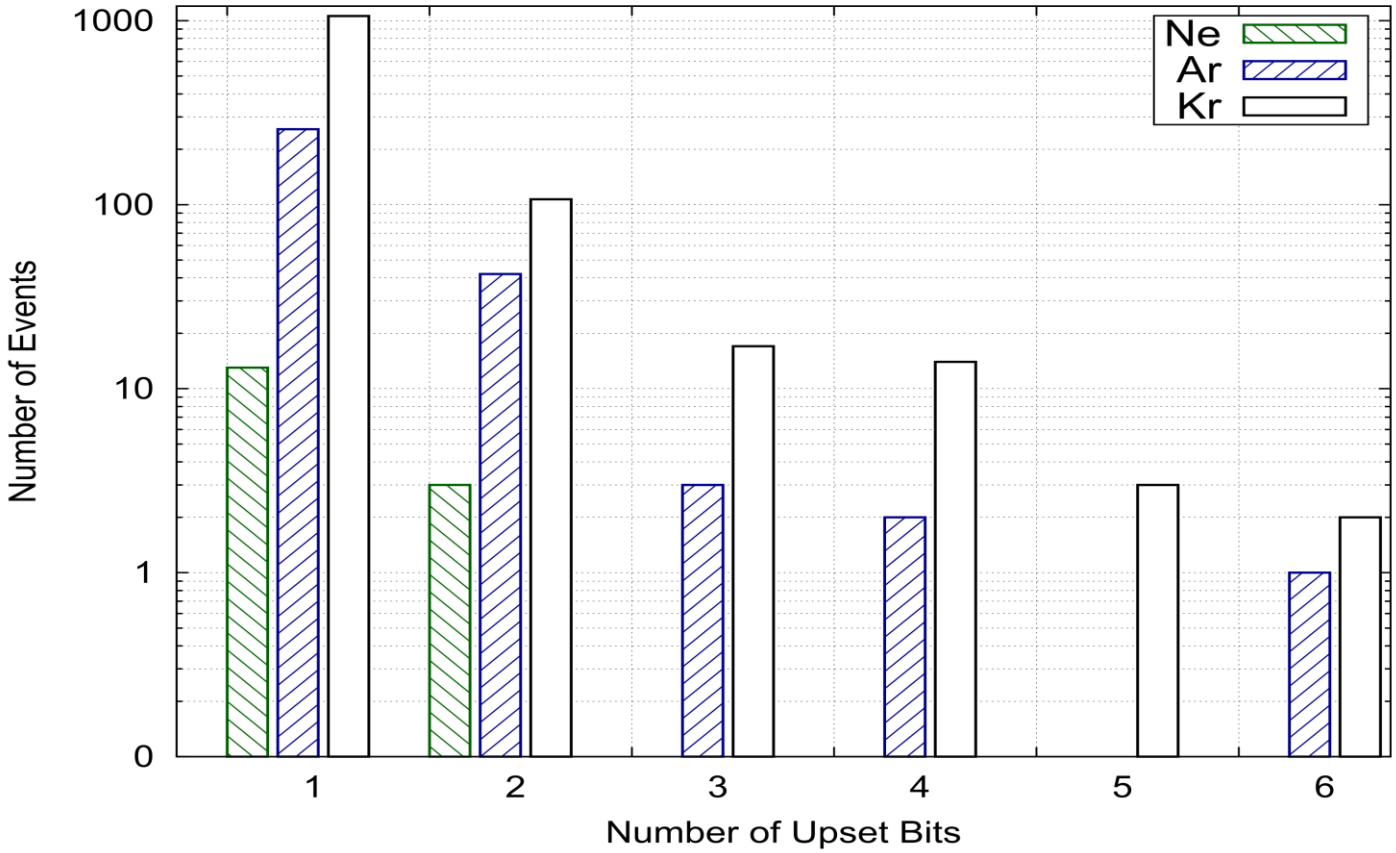
Complex Circuits : Cross Section



Ne : 6.4 MeV cm^2/mg
Ar : 16 MeV cm^2/mg
Kr : 40 MeV cm^2/mg

- Cross section has been normalized per-VersaTile (50 MHz operation)
- Significant variation (nearly 10x) depending on circuit function

Complex Circuits : Number of Affected Bits



Ne : 6.4 MeV cm^2/mg
Ar : 16 MeV cm^2/mg
Kr : 40 MeV cm^2/mg

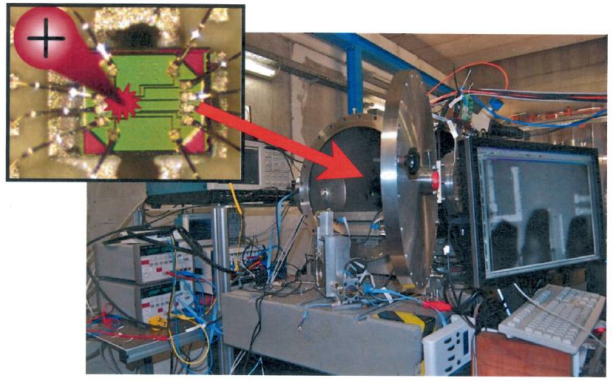
- Number of output bits that are affected by a single event
- Even at low LET (6.4 Mev cm^2/mg), multiple output bits can be affected
- At higher LETs – multiple output upsets are frequent
- Implications for parity protection techniques

Micro Beam Test Setup (GSI)

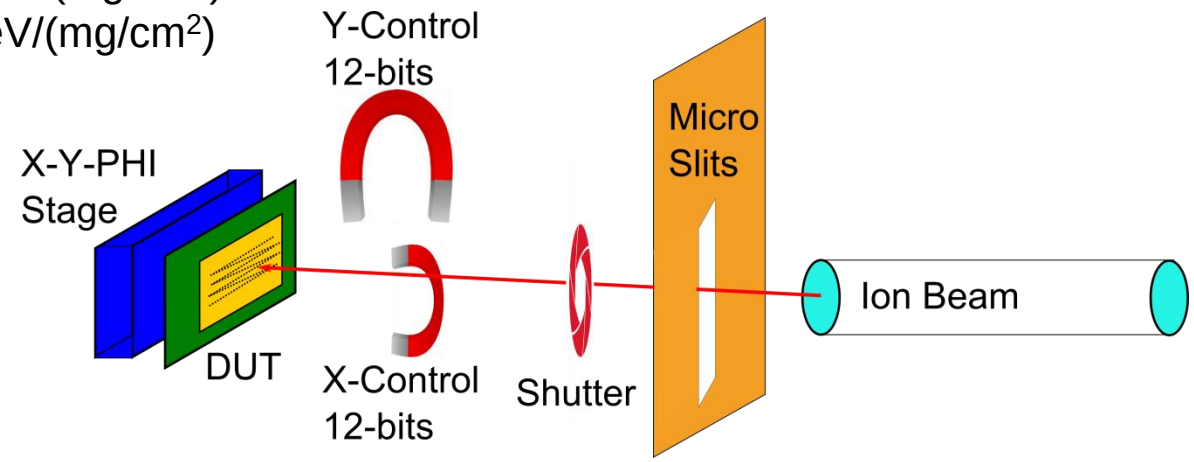
GSI Heavy Ion Micro-Beam

GSI Helmholtzzentrum für Schwerionenforschung GmbH

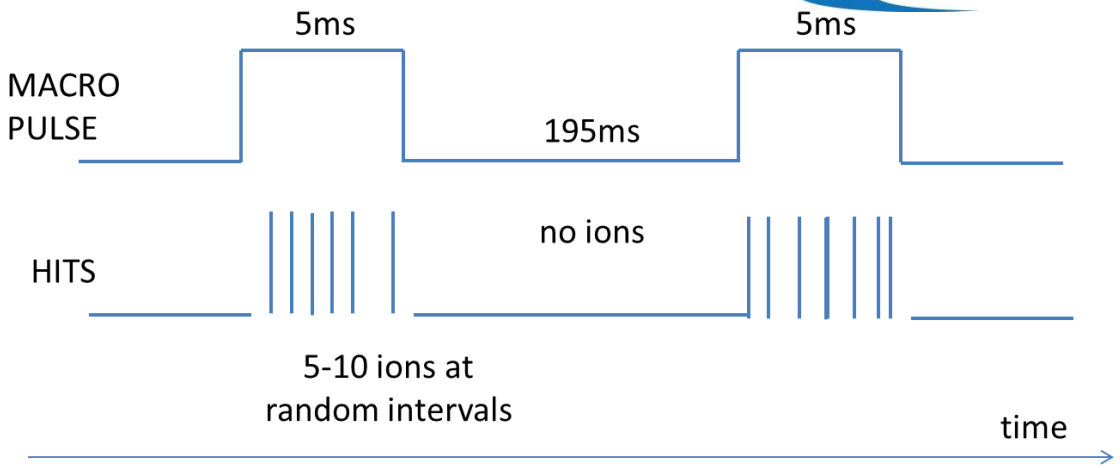
- Located in Darmstadt (near Frankfurt)
- Individual ions launched at specific x-y positions
- Beam is scanned over a region
  - 16 µm x 16 µm
  - 48 µm x 48 µm
  - 144 µm x 144 µm
  - 432 µm x 432 µm
- 500 nm resolution
- Ions accelerated up to 11.4 MeV/µm
  - Au – 4.8MeV/µm - 94 MeV (mg/cm^2)
  - Ti – 4.8 MeV/um - 19 MeV/(mg/cm^2)



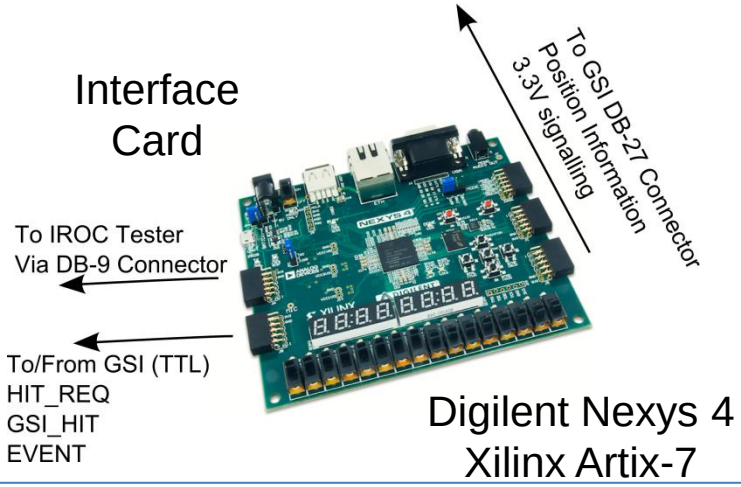
Opened
A3P3000L

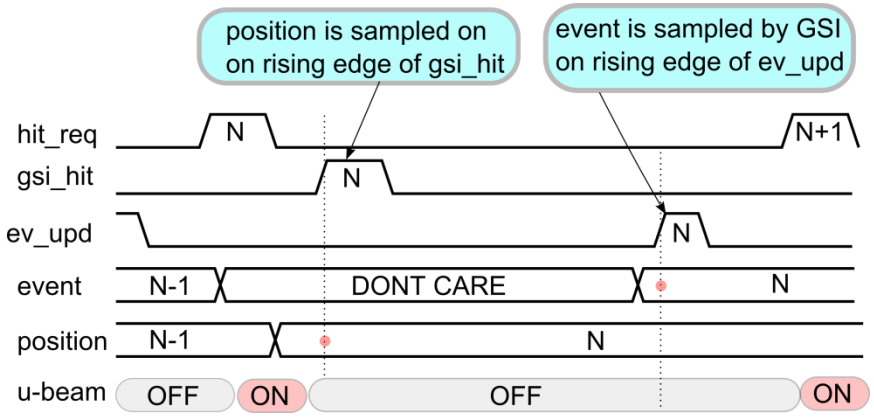


Beam Control

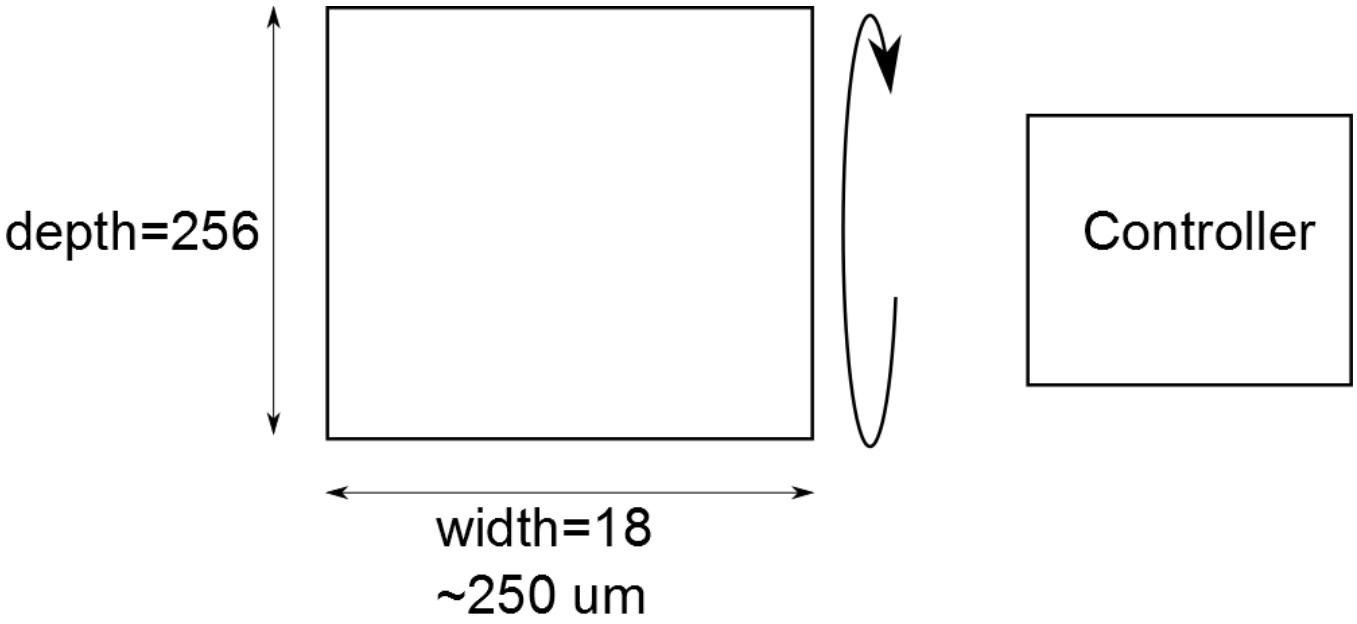


- User requests an ion (hit request)
- GSI responds saying ion detected (gsi hit)
- 5..10 ions available in a 5ms burst every 200 ms
- Typically repeat rate around 15..50 ions / second





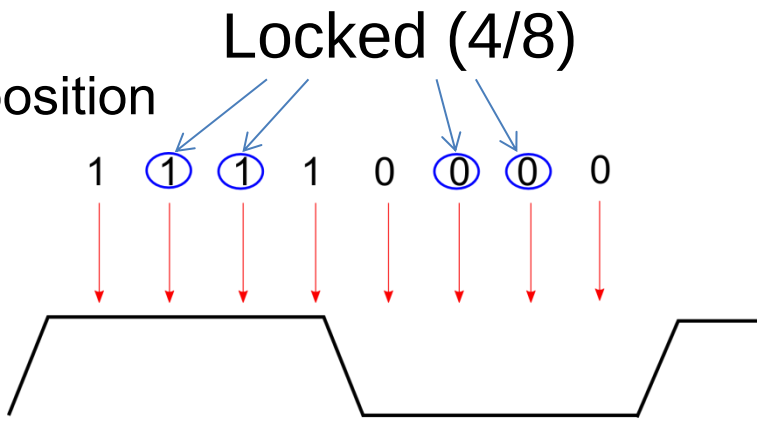
BRAM Test Flow

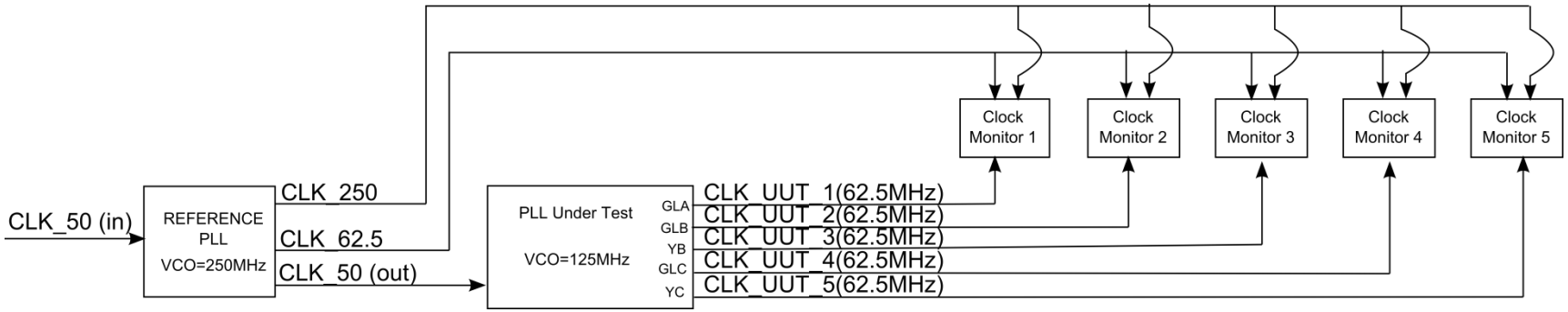


1. Write pattern into memory. (~1.3 usec).
2. Read back pattern from memory + check. (~1.3 usec).
3. Wait for ions. (Handshaking).
4. Read back pattern from memory. (~1.3 usec). -> Report errors (macro, addr, bit)
5. Read back pattern from memory. (~1.3 usec). -> Report errors (macro, addr, bit)

PLL Test Flow (On Chip Monitoring)

- Basic idea : sample CLK_UUT at 8x
- At power-up, each sample "detects" its position
- 4 of 8 sample points "lock" to CLK_UUT
- Error if locked position moves
  (eg. edge moves ≥ 25% cycle)



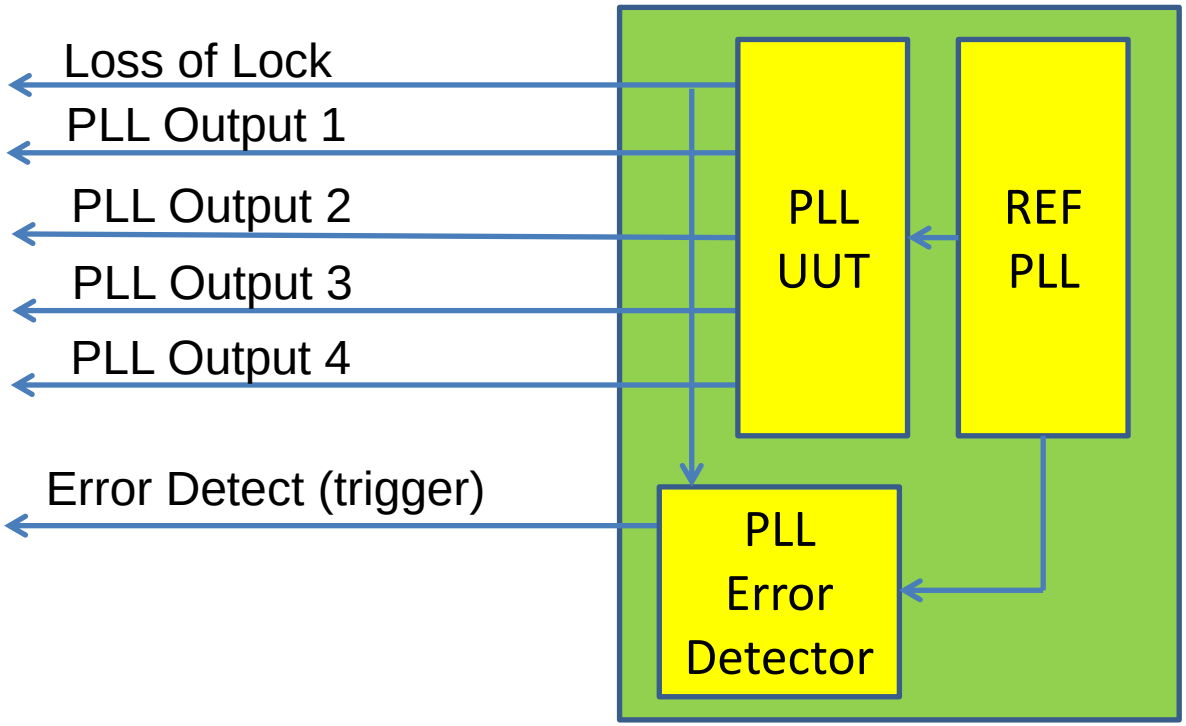


Reference PLL
In : 50 MHz
Out : 50,62.5,250 MHz

PLL Under Test
In : 50 MHz
Output : 5 x (62.5 MHz)

PLL Test Flow (Off Chip Monitoring)

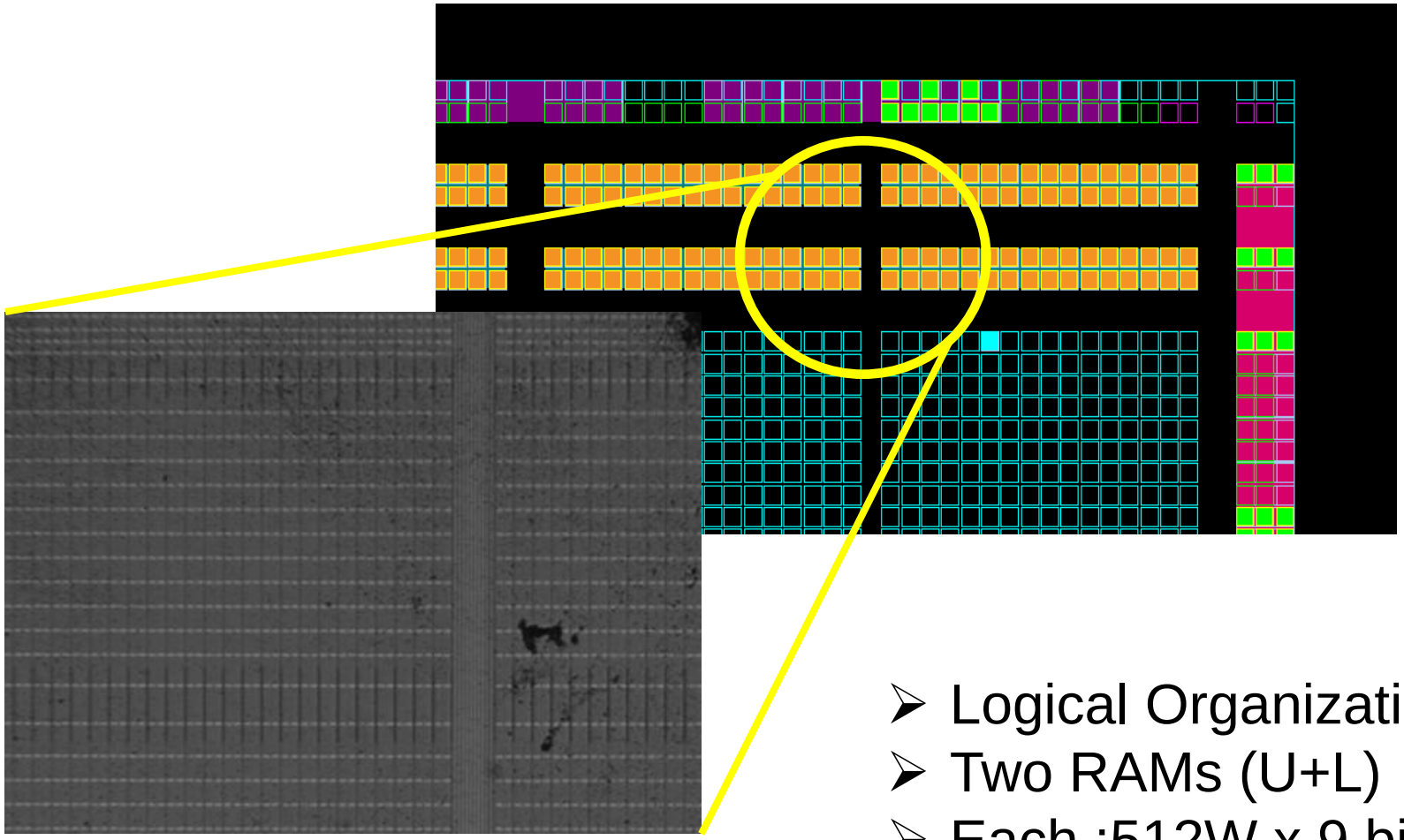
LeCroy
WaveMaster
DSO



- To gain better insight into what is occurring when the PLL “error detector” triggers
- External DSO samples 4 of 5 of the PLL outputs
- Record signal trace if on-chip circuit triggers a PLL error

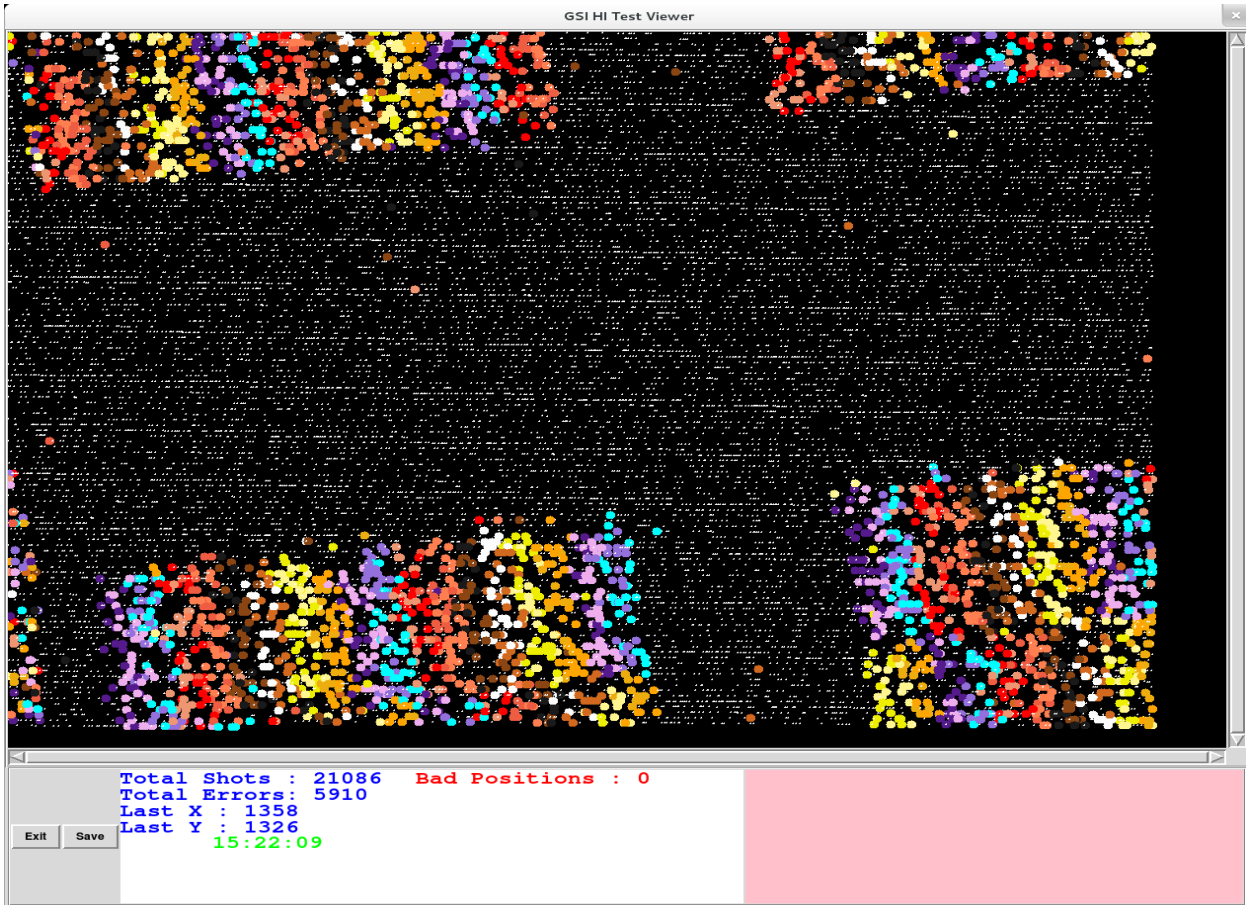
Micro Beam Test Results

Imaging of BRAM (1)



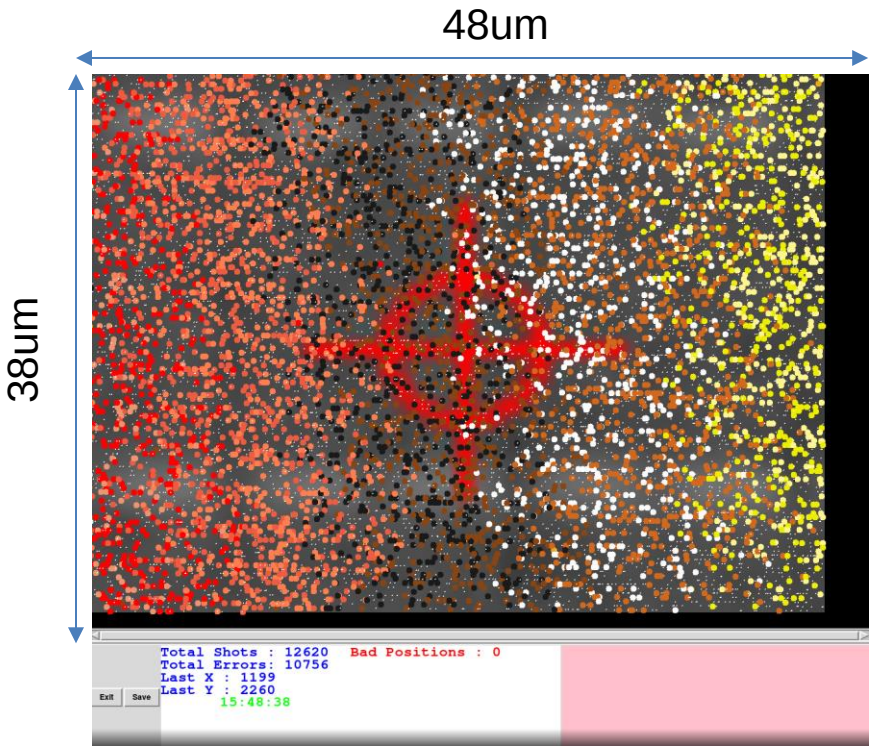
- Logical Organization:
- Two RAMs (U+L)
- Each :512W x 9 bits

Imaging of BRAM (2)

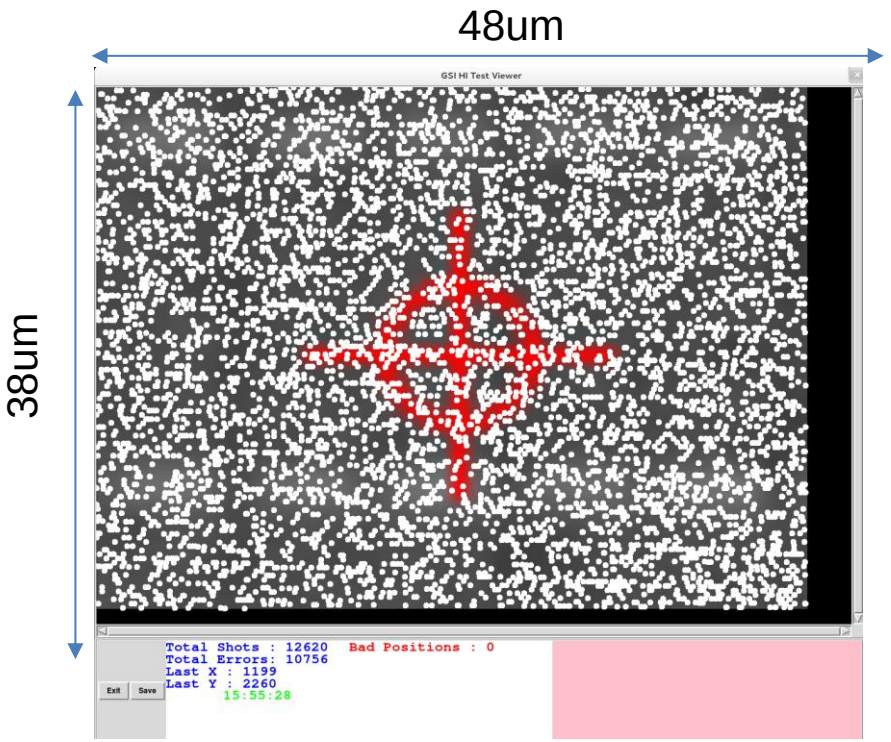


- Results from imaging with Au ions
- Each color represents a bit cell
- Note image from ion beam slightly rotated

Imaging of BRAM (3)



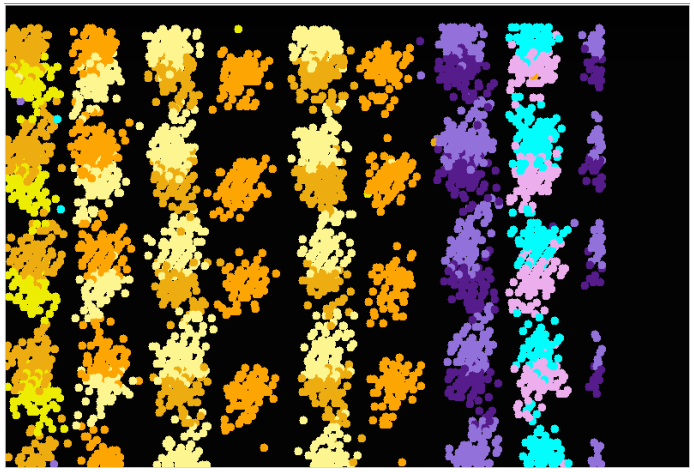
Coloured dots represent bit cells



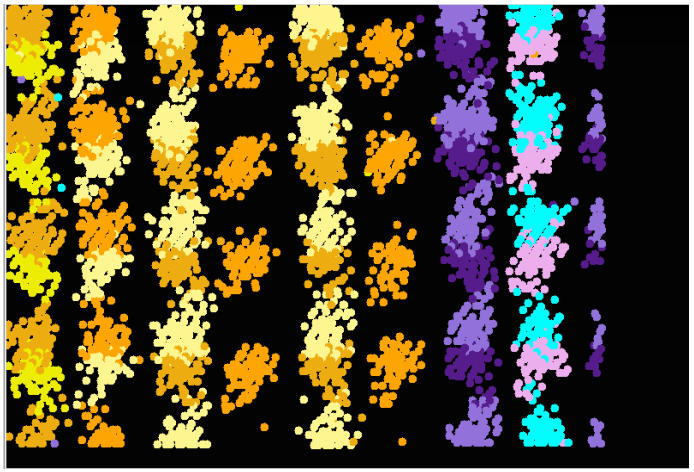
White dots represent points with no response

- Zoomed in scan on BRAM region – **Au ions**
- Bit cells overlap – not possible to identify shape of bit cells

Imaging of BRAM (4)



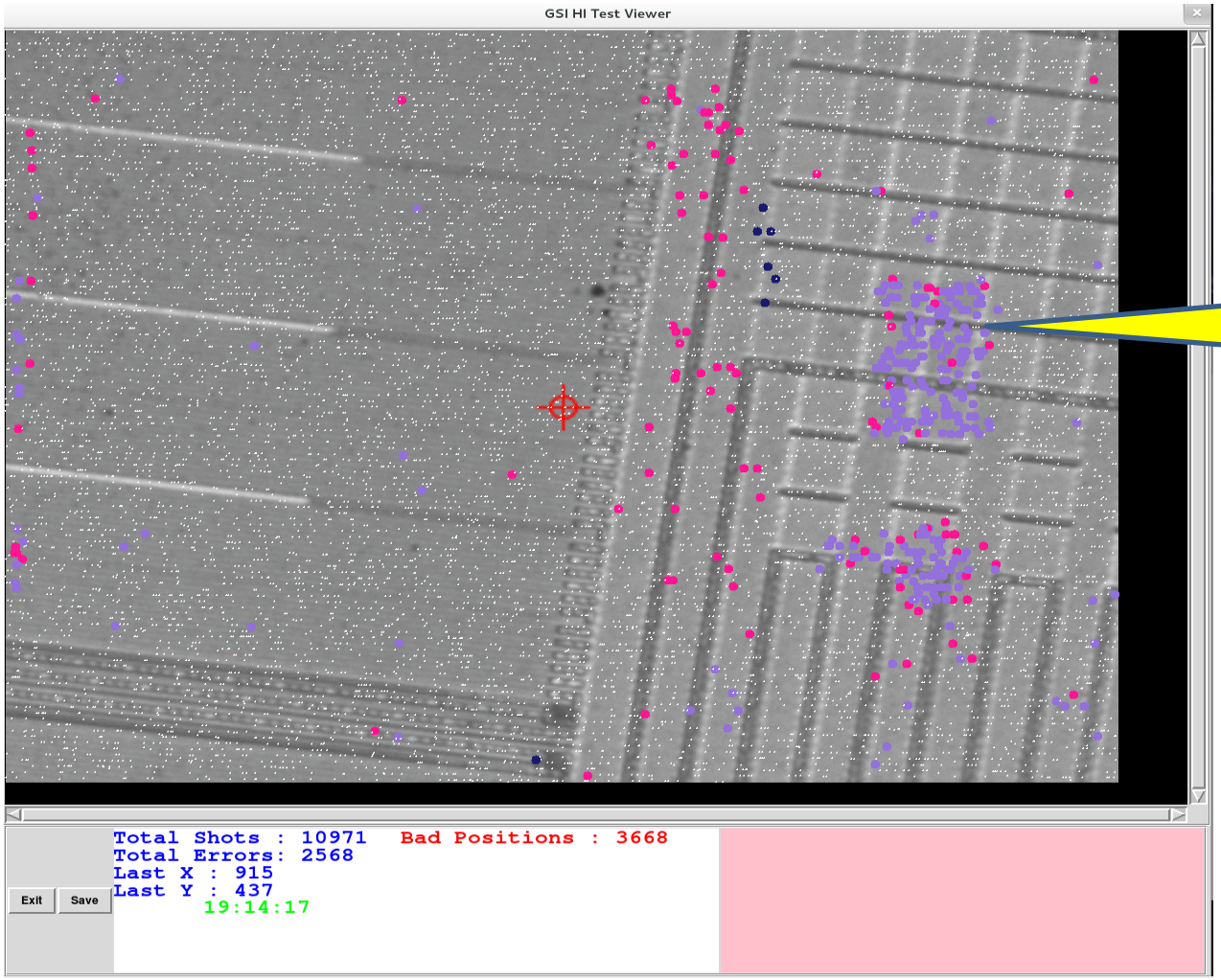
BRAM – All zeroes



BRAM – All ones

- BRAM image produced using **Ti ions**
- Colours represent individual bit cells
- Shape of bit cell can be discerned (e.g. vertical mirroring)
- Logic to physical mapping has been extracted

PLL Imaging (Au Ions)



Highly sensitive region where all outputs are affected but no loss of lock

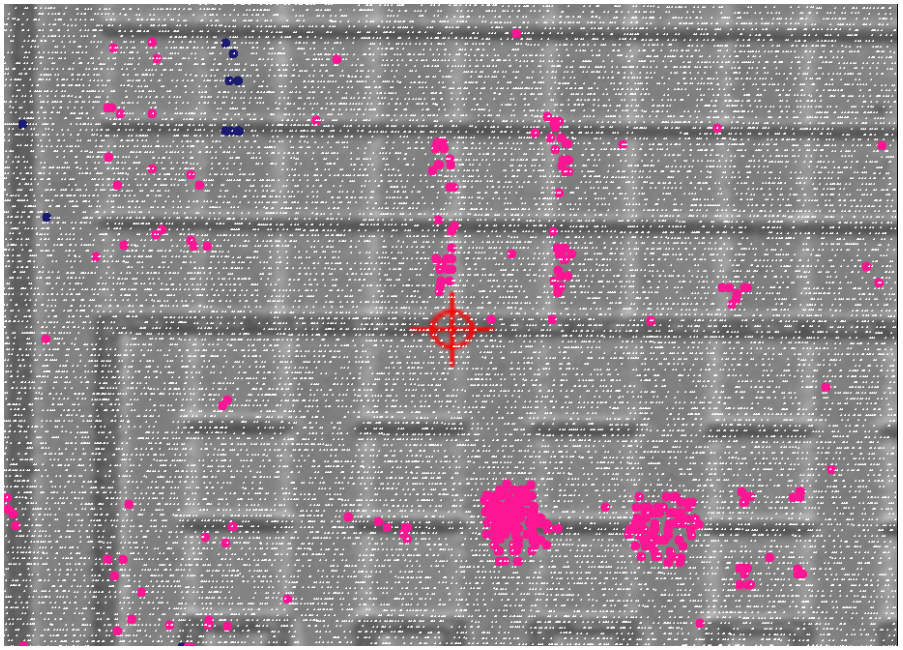
Purple = 5 outputs glitch

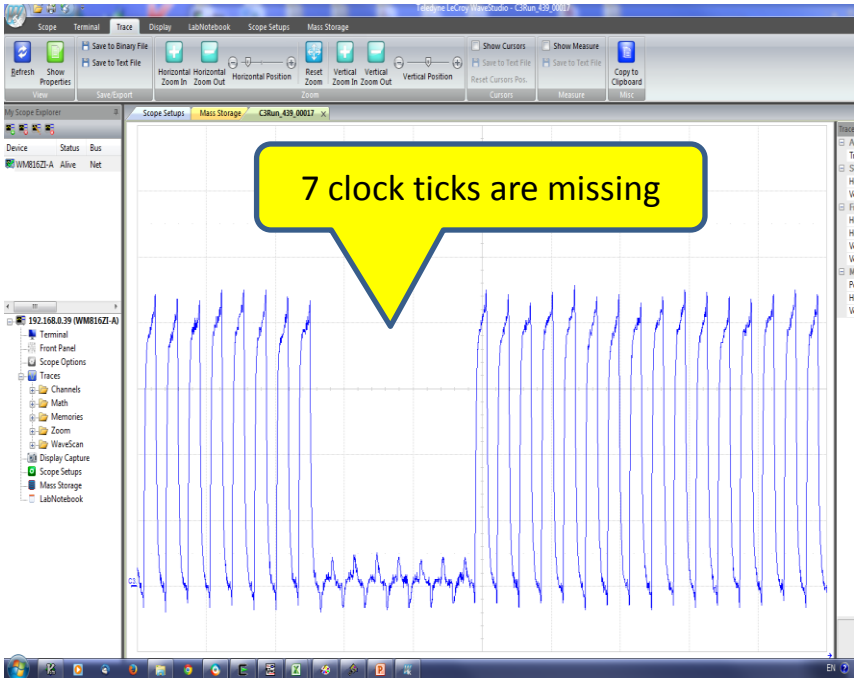
Pink = 1..4 outputs glitch

Dark Blue = Loss of lock ONLY

Yellow = Loss of lock + output glitches

PLL Imaging (Ti Ions)





Purple = 5 outputs glitch

Pink = 1..4 outputs glitch

Dark Blue = Loss of lock ONLY

Yellow = Loss of lock + output glitches

- Many cases where clocks glitch but no loss of lock
- From external captures, appears clock disappears for a handful of clock cycles

Permanent Effects

- Devices were re-programmed with beam OFF

- During broad beam testing (UCL)
  - One device failed to re-program after 1.37 part/cm^2 of Xe ions (≈4.2Krad)
  - Others failed after longer exposure

- During micro-beam testing (GSI)
  - One device failed to re-program after ≈1000 Au ions

- Messages were “Verification 0 failed at rows 7843”
- Devices *appeared* to function correctly if verification disabled

- Subsequent to the testing, some of the devices damaged at UCL could be successfully programmed at being annealed at 100˚C for four days

- More work required to understand this effect (not focus of current work)

Conclusions and Future Work

Conclusions

- Characterization of SETs is complex
  - Dependent on : VersaTile configuration, input state, propagation
- Vernier detector - good sensitivity and temporal precision
- SET characterization of complex circuits more exploitable

- HI micro-beam highly effective tool for investigating sensitive regions
- Selection of ion energy is important for resolution
- Setup of experiments and data logging is complex

Future and Ongoing Work

- Complete data analysis for GSI experiments
- Extend SET measurement circuits to characterize ASIC standard cells
- Continue investigation of destructive effects

Thank You!

Questions?