FPGA in Sodern recent projects

16-18 September 2014

Innovation based on Experience

FPGA in Sodern recent projects

- **Overview of the FPGA in 2 recent projects :**

1- TARANIS
2- BSA ATLID

BSME view

FPGA in TARANIS Project

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FPGA in TARANIS µ-Camera

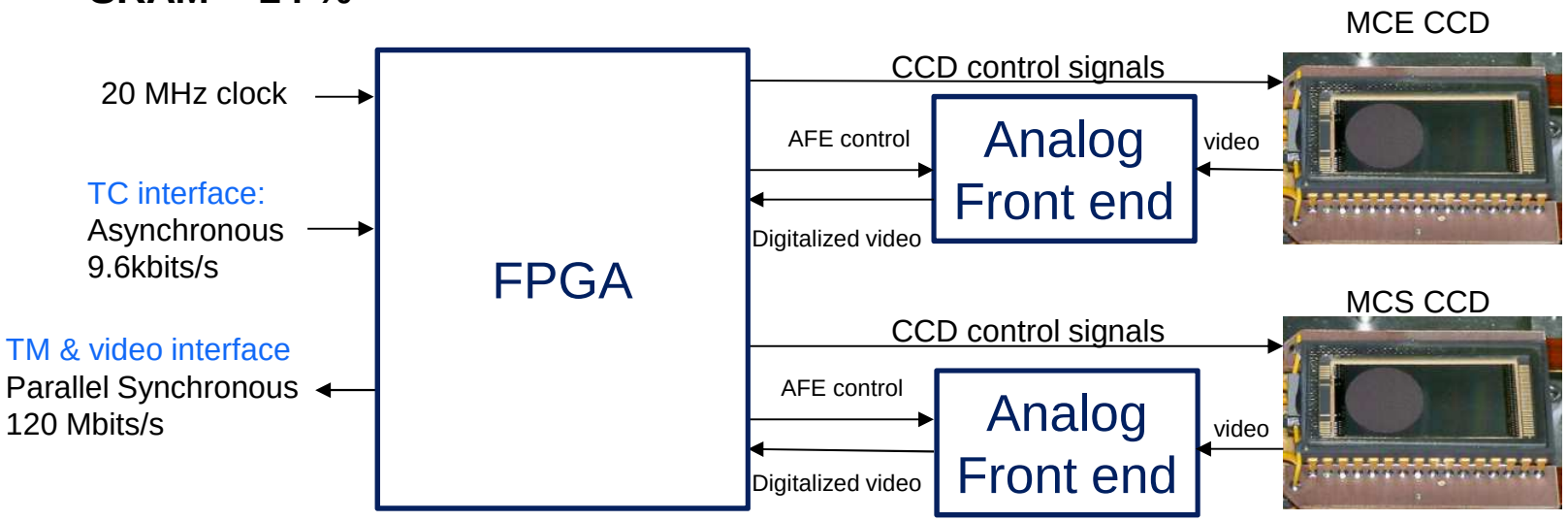
- TARANIS : micro satellite, MYRIADE series of CNES programs
- Tool for the Analysis of Radiation from Lightning and Sprites
- mission : to observe upper atmospheric optical phenomena (blue jet, red sprites, halo, elves)
- Project start : 2007 (studies)
- Launch : end of 2016

- Sodern is developing the micro camera (CCD)

FPGA in TARANIS µ-Camera

- **TARANIS FPGA : a simple design**
  - **Features :**
    - **Provides CCD control signals for 2 CDD**
    - **Drives the Analog Front End**
    - **Acquires the digital video in streaming (120 Mbps)**
    - **Provides an UART Rx interface for parameters (9600 baud)**

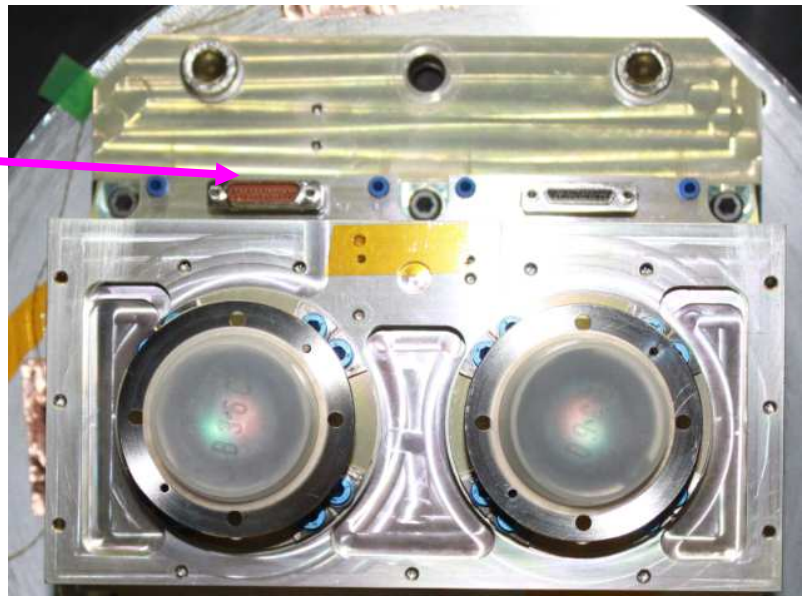
    - **Target : MicroSemi RT3PE3000L (ProASIC3)**
    - **IO pads = 77%**
    - **Core cells (versatile) = 6%**
    - **Max frequency = 46 MHz, requirement = 20 MHz**
    - **SRAM = 14 %**



FPGA in TARANIS µ-Camera

- **The programming interface (JTAG) is available on an external connector.**
- **Advantages of this solution :**
  - **Reprogrammble FPGA are easy to use and improve flexibility**
  - **Late updates can be easily implemented (after assembling)**
  - **The programming frequency can be slow down => no constraint on the I/F**
- **Drawbacks :**
  - **Dedicated pins on the connector for programming (JTAG and power supply)**
  - **Necessary to power up the whole instrument**
  - **Need to add a power supply for the flashpro probe (the probe expected to be powered by the FM)**

Dedicated pins for external programming



FPGA in TARANIS µ-Camera

- **Design is validated with success.**
- **First choice of TARANIS project was to use an ATF280 FPGA (Atmel).**
- **The ATF280 was abandoned :**
  - **The Camera is a high integrated module**
    - => very tight place for the electronics,
  - **high inrush current at start up necessary for the FPGA (~6A)**
    - => need to solder too many capacitors
  - **A low cost and fast solution was expected by the project**
- **ATF280 has been replaced by the RT3PE3000L**
- **Advantages :**
  - **No PROM for configuration**
  - **Less capacitors for start up**
  - **No programming connector (we use the external connector)**

FPGA in ATLID BSA Project

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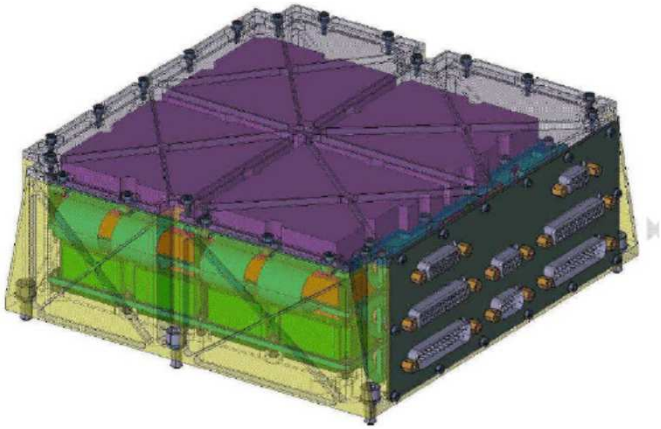
FPGA in ATLID BSA

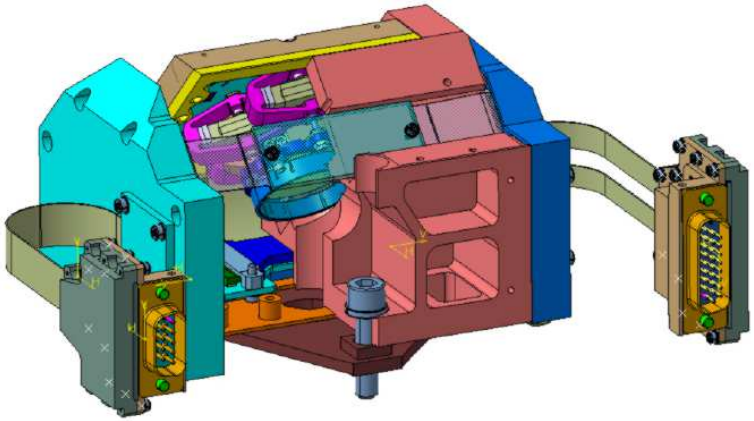
- EarthCARE satellite (ESA program with JAXA cooperation)
- Mission: to determine the Earth radiation budget by providing global observations of clouds and aerosol vertical profiles
- Launch: early 2018
- Inside, one of the 4 instruments is the ATmospheric LIDar (ATLID)
- Sodern is developing two sub-assemblies of ATLID : EBEX and BSA

FPGA in ATLID BSA

- **Two sub-assemblies developed by Sodern :**
  - **The Emission Beam EXpander (EBEX): expands the laser beam to a larger diameter**
  - **The Beam Steering Assembly (BSA):**
    - A 2 axis pointing mechanism, aimed to maximize the detection of the LIDAR echo signal
    - => piezo mechanism is handling the emission mirror
    - BSA is composed of two parts :
      - The BSME (on a panel): main electronics (including FPGA) which drives the mechanism
      - The BSMFE (inside the Power Laser Head): piezo mechanism + front end electronics (proximity electronics)



BSME

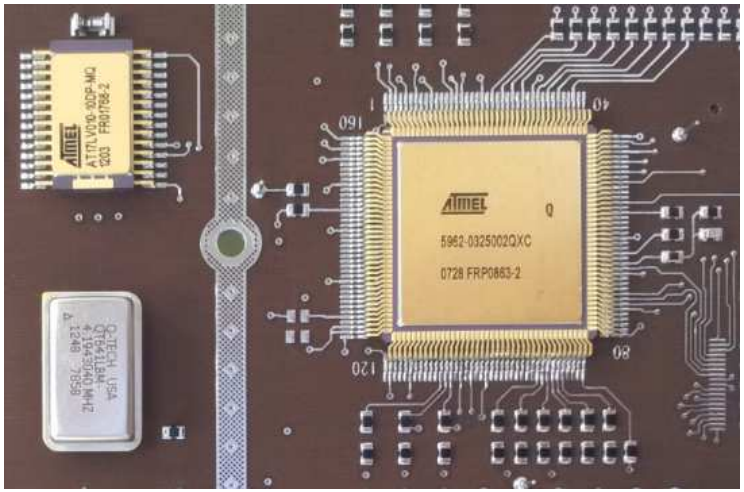


BSMFE

FPGA in ATLID BSA

- **BSA FPGA : a simple design**
  - **Features :**
    - Manages the digital TC/TM interface thanks to dual ASCS16 link
    - Controls ADCs and acquires data, manages offset compensation, collects housekeeping telemetries
  - **Target: Atmel AT40K (SRAM based)**
    - IO pads = 69%
    - Core cells = 62%
    - Max frequency= 8 MHz, requirement = 4 MHz
    - RAM not used on this project (but already used in another project)

EEPROM

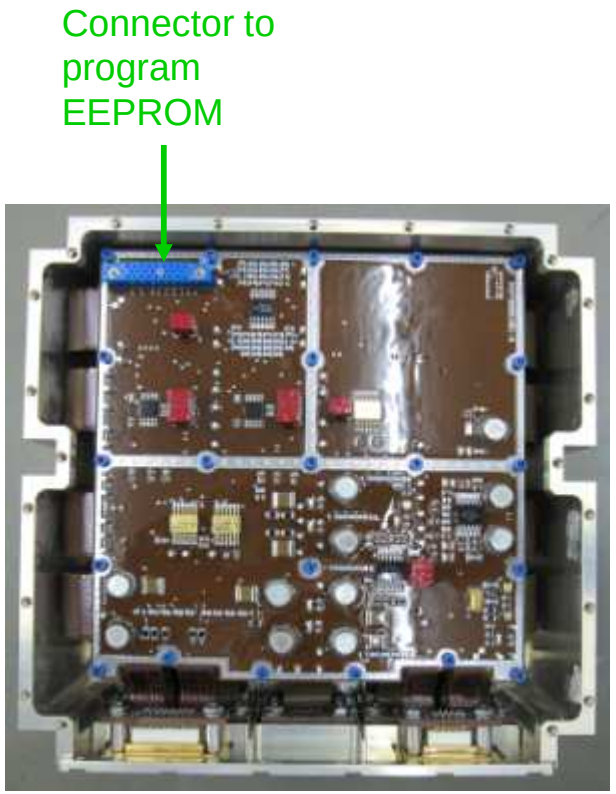


FPGA

Oscillator

FPGA in ATLID BSA

- **Connector on the board dedicated to program the EEPROM : programming is possible until the top cover is screwed**
  - **Advantages:**
    - Reprogrammable FPGA : easy to use and improves flexibility
    - Later updates can be implemented, but only during the tests of the prototype
    - No additional connector on the interface
      - not sufficient IO pins on the external conenctor
      - BSA is a high integrated instrument
  - **Drawbacks:**
    - Design updates are no more accessible after assembling



BSME after integration

FPGA in ATLID BSA

- **AT40K feedback on BSA**
  - **After MEGHA-TROPIQUES and PHARAO, this is the 3rd time Sodern uses AT40K with success**
  - **RAM block were used in PHARAO => saves a SRAM (one component)**

- **Advantages :**
  - SEE hardened cells and RAM blocks => no need to implement rad hard mitigation techniques (no TMR nor EDAC)
  - Only one single supply voltage (3,3 V), and Inputs are 5V tolerant => less regulators, less transceivers to implement
  - Small and easy package (Flat Plack 160)
  - Atmel technical support was very helpful
  - Affordable price (as compared to other FPGA)

- **Drawbacks:**
  - Limited number of gates (46k ASIC gates) and RAM bits (18 kb)
  - Flip-flops in IO pads not supported (=> less Flip-flops than expected)
  - some routing contention when more than 60% of cells are used (with this FPGA, it is better to develop a design form strach and without any IP)
  - High inrush current at start up (1A), now under control in Sodern (as far as space is available)
  - Max frequency is about 10 MHz in practice (30 MHz is possible if no more than one Logic Cell)
  - No problem with only one single clock (derivated clocks were not supported a few years ago)
  - Time consuming for the first time (several calls to Atmel support…)
  - Place and Route Tool (IDS) was not so friendly

FPGA in Sodern

- **Thank you for your attention**
- **Any question ?**
- **www.sodern.fr**