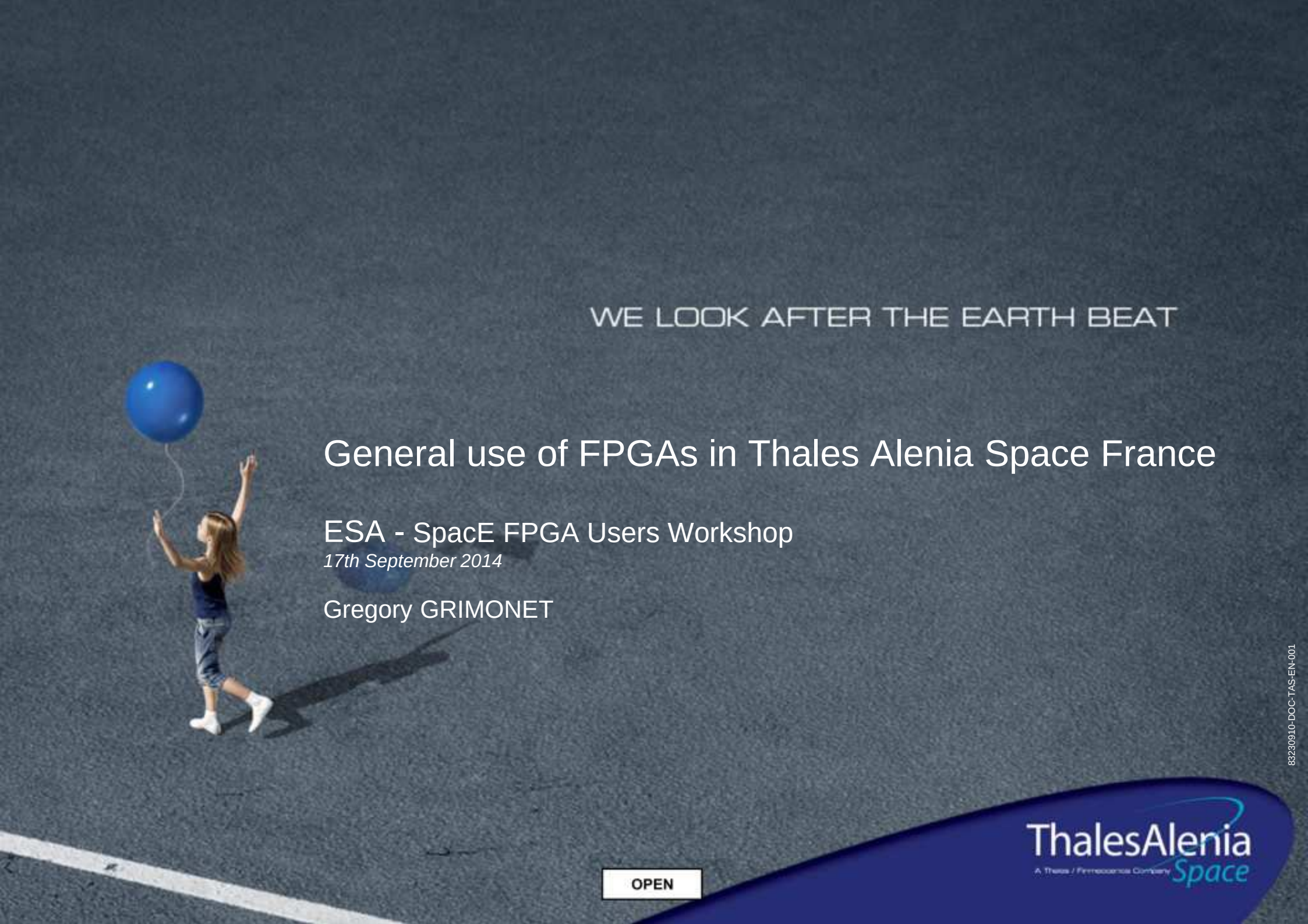

General use of FPGAs in Thales Alenia Space France

ESA - SpacE FPGA Users Workshop

17th September 2014

Gregory GRIMONET

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83230910-DOC-TAS-EN-001

Summary

- FPGAs used in TAS
- TAS Flow
- How choose a FPGA ?
- Problems encountered
- Conclusion / Our need

FPGAs used in TAS-F : MICROSEMI

Family	Device	Package	Since
RTSX-S/SU	RTSX32S/SU	CQFP 256	2003
RTSX-S/SU	RTSX72S/SU	CQFP 256	2004
RTAX-S/SL	RTAX250SL	CQFP 352	2013
RTAX-S/SL	RTAX1000SL	CQFP 352	2013
RTAX-S/SL	RTAX2000SL	CQFP 352	2008

- Antifuse technology (OTP)
- Up to 100% of the cells could be used
- Complete family

FPGAs used in TAS : ATMEL ATF280

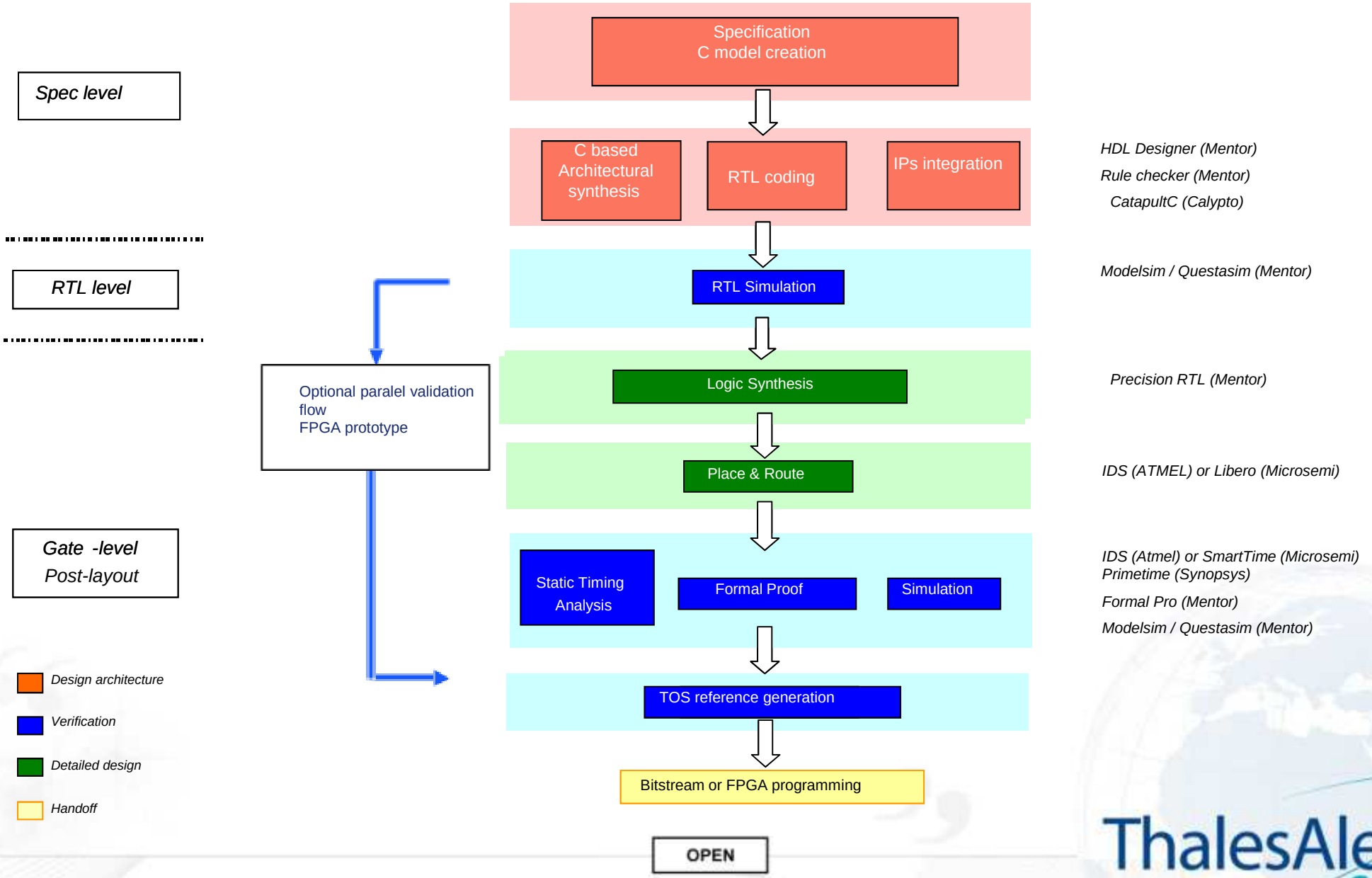
- Evaluation on breadboard since 2010
- Used as Flight model since 2011
- Packages CQFP256 & CQFP352
- Advantages :
  - Full European solution
  - Reprogrammable
- Drawbacks :
  - Performance (~10MHz maximum frequency) and poor area usage (< 50%)
  - 2 to 3 chips on the board (1 to 2 EEPROMs and 1 ATF280)
  - Tools maturity

FPGAs used in TAS : XILINX

- Large use of the Virtex family for ASIC and OTP FPGA prototyping
  - High capacity
  - Timing performances
  - Reprogrammable

- Interest in SIRF component
  - Same advantages as the commercial part
  - But some functions sensitive to radiation
  - But high power consumption ! (static mainly)

TAS flow for FPGA flight model



TAS flow : formal proof

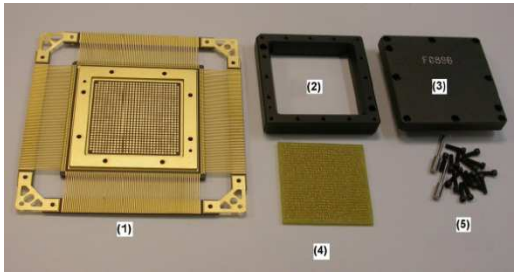
- Formal proof verifies RTL versus layout tool output netlist
- Flow built with Mentor help
- Description
  - Use of FVI flow : constraints file generated by Precision RTL
  - Mentor tool create Formalpro setup file from the constraints file
  - Run Formalpro
- Results
  - 100% of the MICROSEMI designs are equivalent
  - Only one ATMEL FPGA hasn't be verified because it contains RAMs (limitation in the constraint file, and also "Formalpro unfriendly" with VHDL coding style)

TAS flow : STA

- Vendor tool
  - ATMEL => IDS
  - MICROSEMI => SmartTime
  - XILINX => Timing Analyzer
- Primetime flow
  - Possible with ATMEL ATF280 and MICROSEMI FPGAs
  - STA can be done with “standard” scripts, ie used for ASIC verification
  - ATMEL tool IDS2PT generates a netlist compatible with PrimeTime
- => But PrimeTime has not the same behaviour !
  - Problem with library (ATMEL) and SDF (MICROSEMI)
  - So currently TAS-F sign off flow is IDS based or SmartTime based

TAS flow : MICROSEMI prototyping for RTAX-CQFP352

AX-CQFP352	AX-FG896 CQFP to FBGA Adapter Sockets	ProASIC3E ALDEC Prototyping Adaptor



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TAS flow : Post programming sequence (MICROSEMI)

- Before 2014
  - TOS creation (TAS designer)
  - Post programming/pre-BI tests (static parameters + Go/NoGo functional test, at 3 temperatures & 3 supply voltages)
  - Burn In whatever the quality level (B-flow, E-flow, QML-V)
  - Post Burn-In tests, same as pre-BI, + drift calculation

  ⇒ Post Programming Burn-In sequence (PPBI) has been applied to FPGAs in TAS-F, since the beginning of FPGAs use

- Since 2014 :
  - Publication of the ECSS-Q-ST-60C Rev.2 (21 October 2013)
  - Burn In is no longer performed by TAS-F
  - Post programming tests (static parameters + Go/NoGo functional test, at 3 temperatures & 3 supply voltages) are maintained by TAS-F

TAS strategy

- On the last 13 years, we develop an average of 18 circuits per year
  - 4 digital ASICs
  - 1 analog and mixed ASIC
  - 13 FPGAs including 6 Flight Models

Total	
25	SX32/16
28	SX72S
8	SX32S
1	RTAX250
2	RTAX1000
9	RTAX2000
7	Virtex
27	Virtex 2
25	Virtex 4
21	Virtex 5
5	ATF280

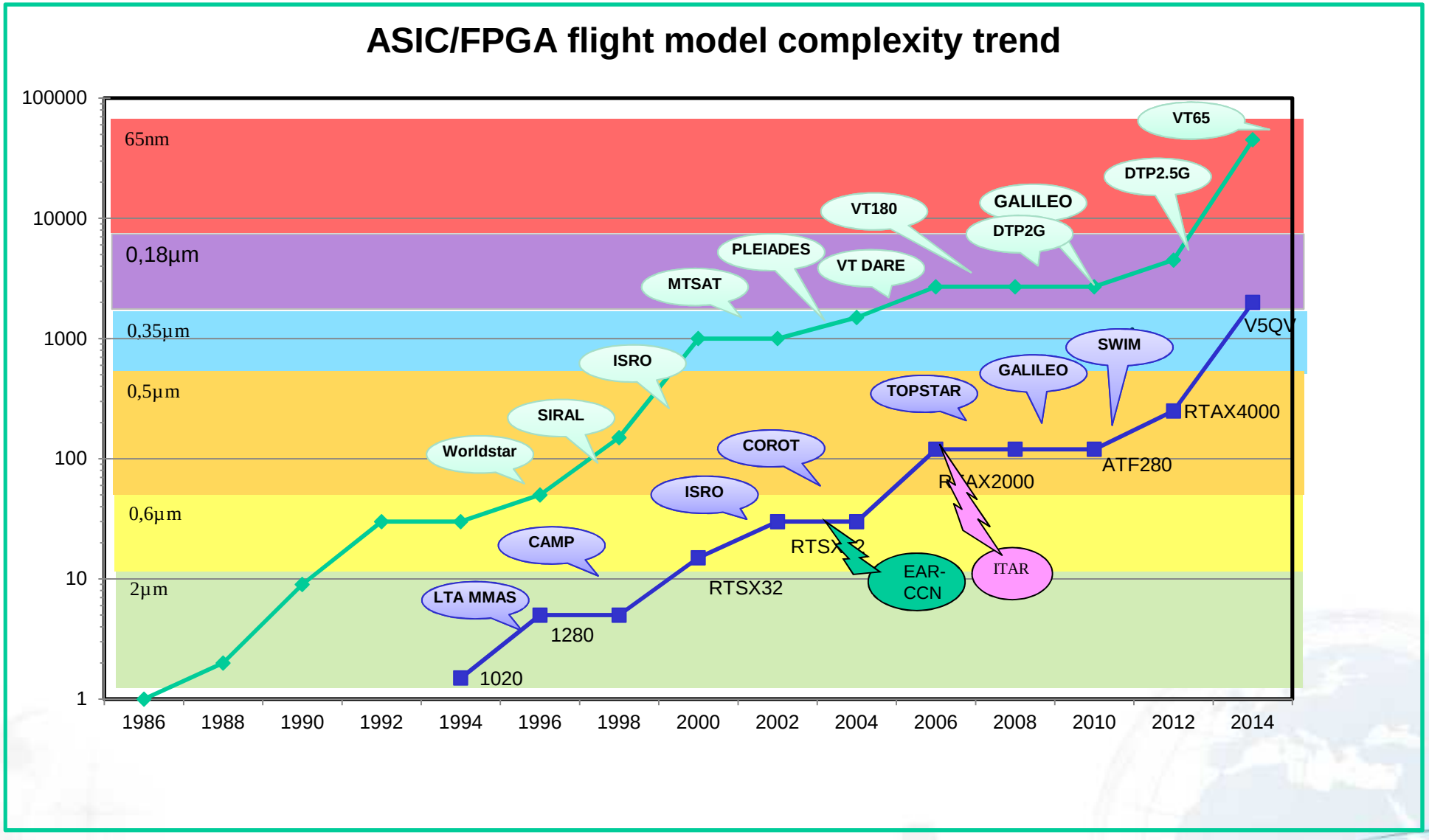
- FPGA are a large part of our business and it will increase in number of design. In parallel, the ASIC complexity will also increase drastically following technologies capability (ex ST 65nm)

Why choose a FPGA ?

	FPGA	ASIC
Integration / Complexity	--	++
Maximum frequency	--	++
Power consumption	--	++
Prototyping	++	--
Flexibility	++	--
Risks	++	--
Confidentiality	--	++
Development cost	++	--
Unitary cost	--	++
Development cycle	++	--
Fast redesign	++	--

- Different advantages and drawbacks but don't oppose these 2 solutions, there are complementary
- TAS-F have the capacity to do these 2 activities

ASIC/FPGA evolution



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How choose a FPGA

- Depending on performances (timing, area, power, hard blocks, …)

	MICROSEMI RTSX		MICROSEMI RTAX						XILINX	ATMEL
Type	SX32SU	SX72SU	250S	1000S	2000S	4000S	2000D	4000D	SIRF	ATF280
Combinatory Slices	1 800	4 024	2 816	12 096	21 504	40 320	19 712	36 960	81 920	28 800
Registers	1 080	2 012	1 408	6 048	10 752	20 160	9 856	18 480	81920	14400
Eq gate ASIC (Kgates)	16	32	25	109	194	363	177	333	1 311	259
DSP / MAC	0		0	0	0	0	64	120	320	0
Total memory (Kbits)	0		55	166	295	553	295	553	10728	115
DCMs / PLLS	No		Yes						Yes	No
SERDES	No		No						Yes	No
Max user IO	227	360	248	418	684	840	684	840	836	308
Process	0.25 um		0.15 um						65 nm	180 nm

- Depending on applications

- Complete ASIC offer since the EOL of the MG2RT and MH1RT technologies

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Tools : problems / limitations / wishes

MICROSEMI

Issue	
#1	Slack value is different, depending on the command used: • `report -type "timer"` command in a script file • `Maximum delay Analysis` in the graphical view
#2	SmartTime does not performs a correct STA on inter-clock domain analysis (between the main clock and a clock generated on the falling edge of the main clock)
#3	Resources reported by Designer are different, depending on the command used: • `report -type "global_usage"` • `report -type flipflop -fmt summary`

Tools : problems / limitations / wishes

- ATMEL
  - #1 Only one reset which is accessible from an input pin
  - #2 PDL cannot be generated on some designs due to memory limitation (IDS crash)
  - #3 IDS supports now correctly falling edge DFF (since spring 12)

- XILINX SIRF / MICROSEMI RT4G
  - Due to ITAR restriction, Precision RTL can’t have “space” libraries in order to perform a logic synthesis

Conclusion

- ASIC and FPGA are complementary and must not be opposed. The usage of FPGA in TAS-F product will increase. Nevertheless, an ASIC solution is still mandatory for critical products (huge processing capability, low power, low recurrent cost)

- TAS-F is interested in reprogrammable FPGA (ATMEL, XILINX SIRF, MICROSEMI RT4G, New European FPGA) for future products

- A large FPGA with reasonable power consumption and price is expected at short term