ECSS-Q-HB-60-02

"Techniques for Radiation Effects Mitigation in ASICs and FPGAs"

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Microelectronics Section
ESTEC
17/09/2014

outline

- Handbook goals & scope
- ECSS context
- History of this Handbook
- General structure:
- walk through the contents
- The Working Group review and status

ECSS-Q-HB-60-02 scope and goals

compilation of

techniques to mitigate effects of radiation in integrated circuits (ICs), ASICs & FPGAs

Handbook intended users

Engineers doing selection, use or development of ASIC/FPGA to be used in radiation environment.

techniques **grouped** according to the different stages (levels) of an IC development flow

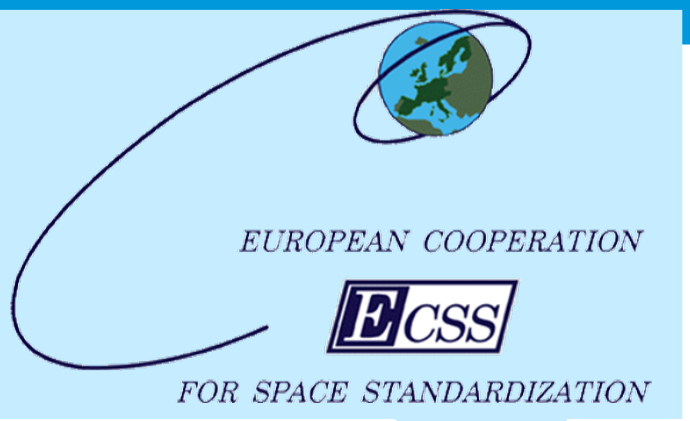
manufacturing processes
transistor-level design and layout
standard logic-cell libraries
rad hard memory cells
analogue, digital or mixed-signal IC / SoC designs
SW and off-chip HW mitigations

In addition,

overview of the space radiation environment and its effects in semiconductor devices
how to validate the mitigation techniques
general guidelines for selecting techniques, examples of typical scenarios

Guidelines and references, not requirements

Deciphering the handbook coded name



Space product assurance (branch “Q”)

ECSS-Q-HB-60-02

Handbook

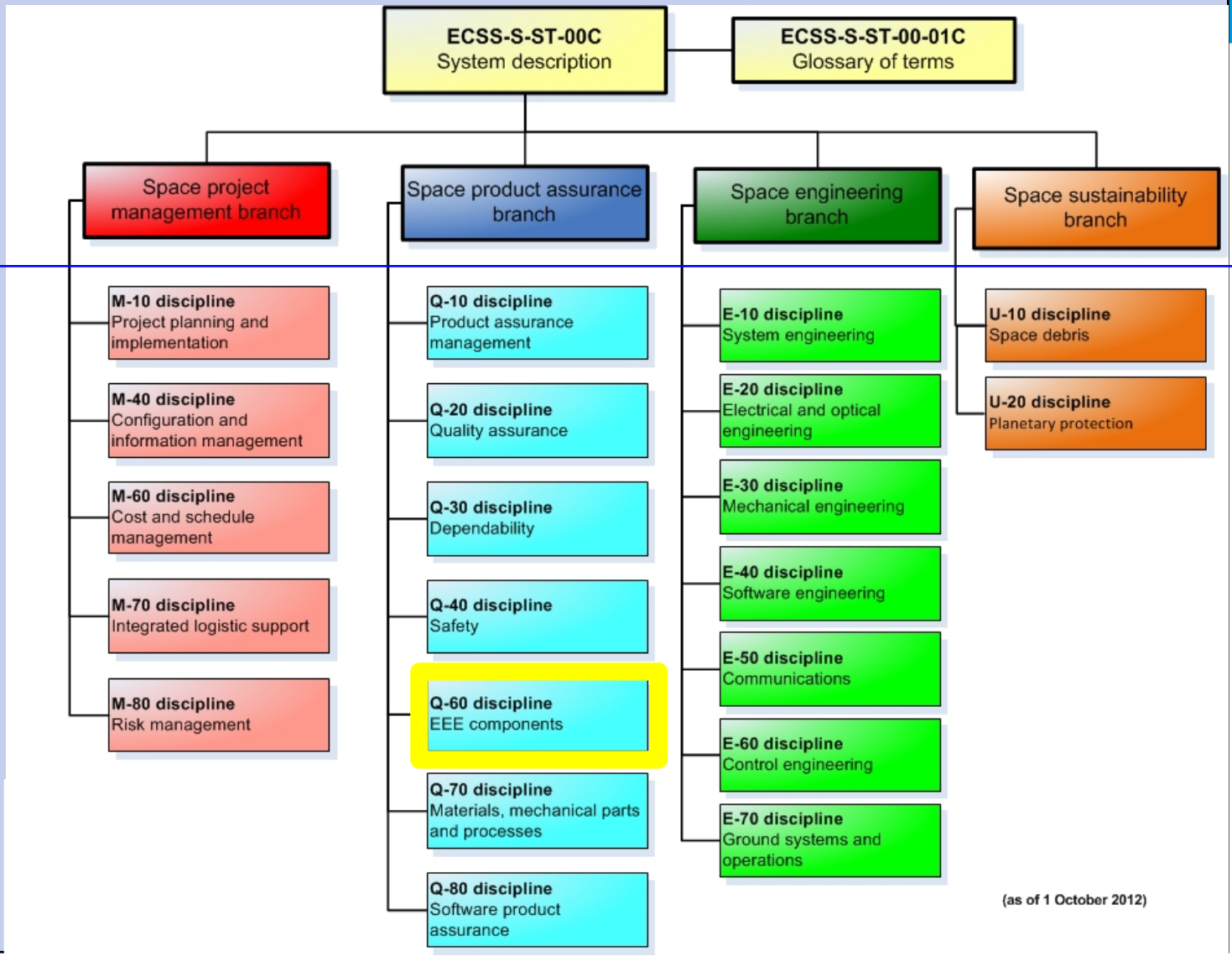
EEE Components (discipline “60”)

“Techniques for Radiation Effects Mitigation in ASICs and FPGAs”

ECSS documentation structure

Branches

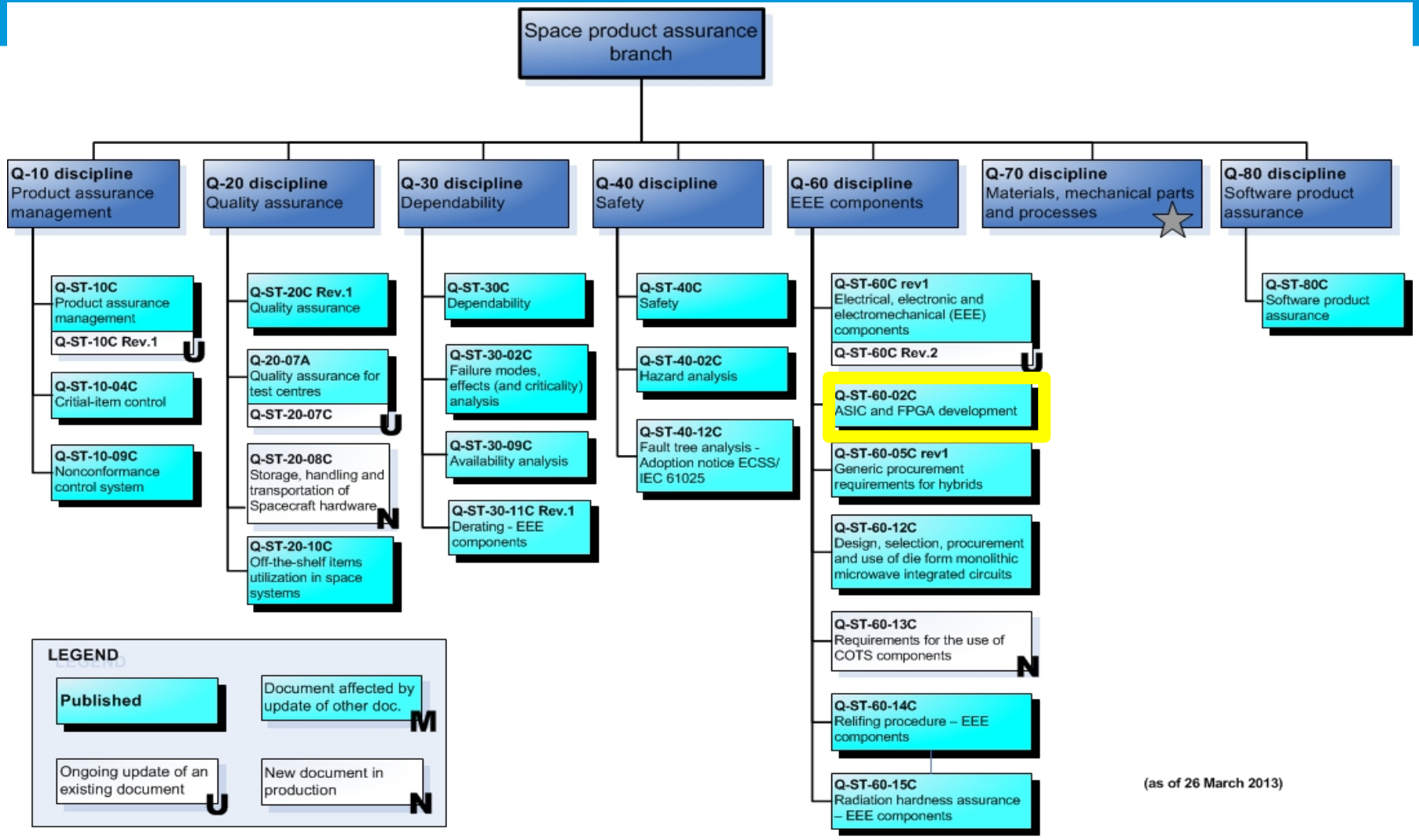
Disciplines



ECSS types of documents

standards	**for direct use in invitation to tender and business agreements**
handbooks	**non-normative documents providing guidelines and/or collection of data**
technical memoranda	**non-normative documents providing useful info or data not yet mature for a standard or handbook**

ECSS Q branch available standards



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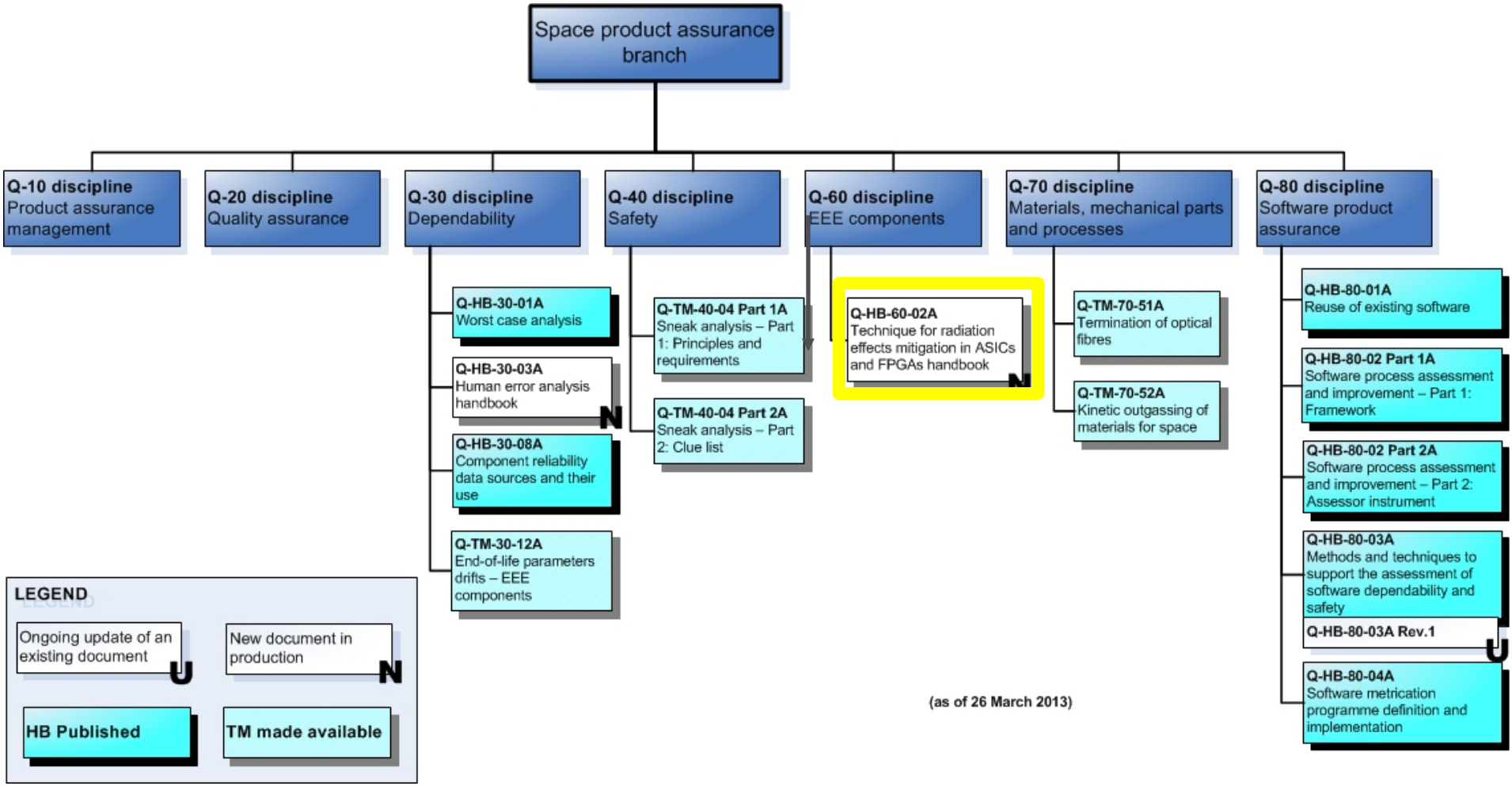
ECSS Q branch available Handbooks and Technical Memoranda



History of ECSS-Q-HB-60-02

1998 : first contract to prepare an ECSS Std for ASIC development (TESAT(D))

2007/07: ECSS-Q-60-02: "ASIC and FPGA development" **standard** released

2008/07: ECSS-Q-**ST**-60-02: "ASIC and FPGA development" name changed

2010/03: contract KO to develop 1st ECSS-Q-**HB**-60-02 draft : "Techniques for Radiation Effects Mitigation in ASICs and FPGAs" by **TIMA**(F) et al.

2010/09: workshop on the topic at ESTEC

2011/12: Final presentation (version 6 of the HB draft) with training at ESTEC

2012/02: Final revision to the HB (version 7), with inputs from TIMA & ESTEC

2013/10: "ECSS Working Group" KO to improve the 1st HB draft for future ECSS public review

Future of ECSS-Q-HB-60-02

2014 : ECSS Working Group preparing a new, improved HB draft for …

2015/03: ECSS-Q-HB-60-02 release for ECSS "**public review**"

2015/Q3: ECSS-Q-HB-60-02 **final release** as a new ECSS handbook

Who worked in the ECSS-Q-HB-60-02 ?

First HB draft put together by **TIMA (F)**, under **ESA** contract, with inputs from:

- M. Alles, **University of Vanderbilt (USA)**(process and layout level)
- D. Loveless, University of Vanderbilt (analogue & mixed-signal circuits)
- M. Nicolaidis, **TIMA(F)** laboratory (digital circuits)
- F. L. Kastensmidt, **Universidade Federal do Rio Grande do Sul(Brazil)** (digital circuits & FPGAs)
- M. Violante, **Politecnico di Torino(I)** (embedded software)
- M. Pignol, **CNES(F)** (system architecture)

Final HB version (expected for 2015 Q3) by the ECSS WG will include inputs/corrections from experts in **ESA, Thales, AirbusDS, RUAG, OHB, CNES(F), CERN(CH) and IMEC(B)**

Over 300 citations of industry, academia, vendors and agencies worldwide

Handbook table of contents

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7 Technology selection and process level mitigation
8 Layout
9 Analogue circuits
10 Digital circuits
11 Mixed-signal circuits
12 Field Programmable Gate Arrays
13 Embedded memories
14 Embedded software
15 System architecture
15 pages
16 Validation methods
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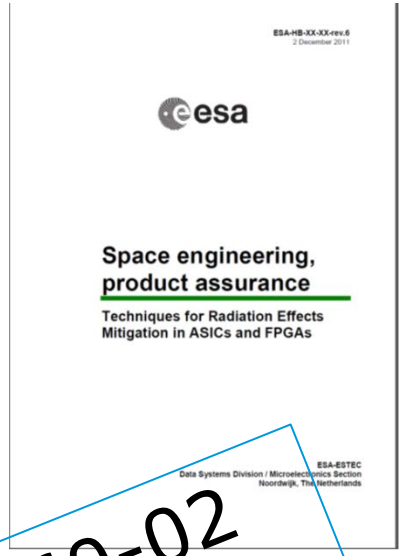

ECSS-Q-HB-60-02
Version 7
(Feb 2012)

Common structure of the chapters

a. Scope
b. Table of Mit. Techniques vs. Rad Effects they
c. Mitigation techniques concept descriptions, how to implement it
d. Examples, Figures
e. Available Test Data (simulations, radiation testing, in-flight)
f. Added value (efficiency)
g. Known issues (Weaknesses, elements to be considered)
h. ID card
   - IC family
   - Abstraction level
   - Pros
   - Cons
   - Mitigated effects
   - Validation Methods
   - Automation tools
   - Vendor solutions

ECSS-Q-HB-60-02: the first chapters

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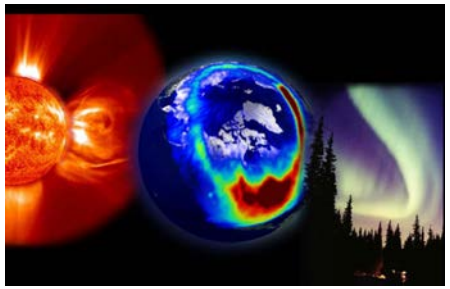
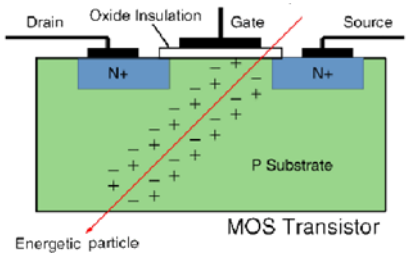
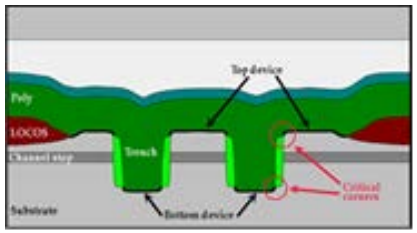


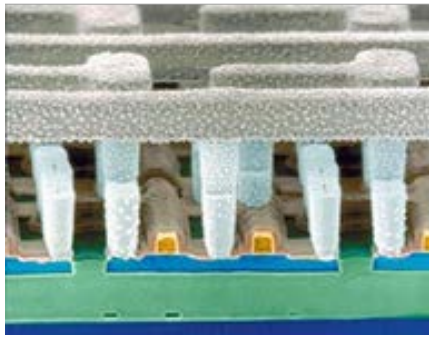


Overview of ECSS-Q-HB-60-02 contents

7 Technology selection and process level mitigation

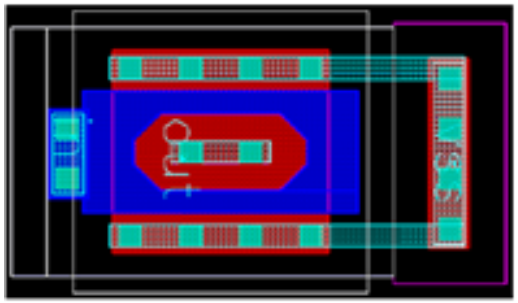
7.1 Scope
7.2 Table of effects vs mitigation techniques
7.3 Mitigation techniques
7.3.1 Epitaxial layers
7.3.2 Silicon On Insulator
7.3.3 Triple wells
7.3.4 Buried layers
7.3.5 Dry thermal oxidation
7.3.6 Implantation into oxides
7.4 Technology scaling and radiation effects
7.4.1 Effects of technology scaling on TID sensitivity
7.4.2 Effects of technology scaling on SEE sensitivity



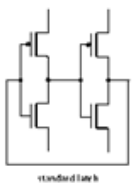


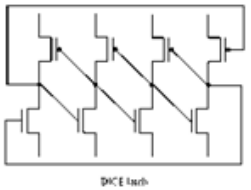
Overview of ECSS-Q-HB-60-02 contents

8 Layout



8.1 Scope
8.2 Table of effects vs mitigation techniques
8.3 Mitigation techniques
8.3.1 Enclosed Layout Transistor
8.3.2 Contacts and guard rings
8.4 Radiation-hardened libraries





8.4.1 IMEC Design Against Radiation Effects library
8.4.2 CERN 0.24 µm radiation hardened library
8.4.3 BAE 0.15 µm radiation hardened library
8.4.4 Ramon Chips 0.18 µm and 0.13 µm radiation hardened libraries
8.4.5 Aeroflex 600, 250, 130 and 90 nm radiation hardened libraries
8.4.6 Atmel MH1RT 0.35 µm and ATC18RHA 0.18 µm CMOS radiation hardened libraries
8.4.7 ATK 0.35 µm radiation hardened cell library
8.4.8 ST Microelectronics radiation hardened library

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9 Analogue circuits

9.1 Scope

9.2 Table of effects vs mitigation techniques

9.3 Mitigation techniques

9.3.1 Node Separation and Interdigitation

9.3.2 Analog Redundancy (Averaging)

9.3.3 Resistive Decoupling

9.3.4 Filtering

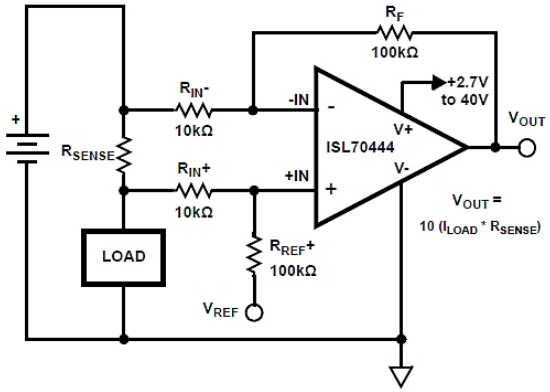
9.3.5 Modifications in Bandwidth, Gain, Operating Speed, and Current Drive

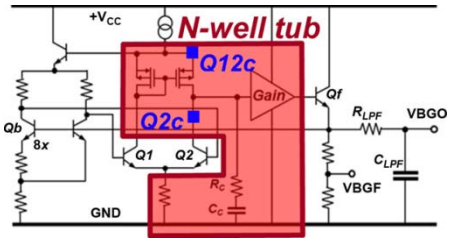
9.3.6 Reduction of Window of Vulnerability

9.3.7 Reduction of High Impedance Nodes

9.3.8 Differential Design

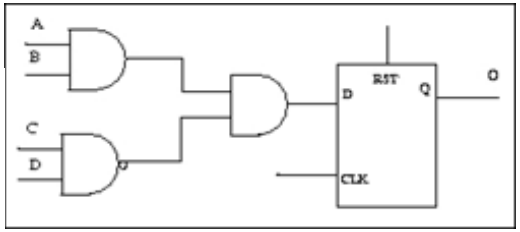
9.3.9 Dual Path Hardening





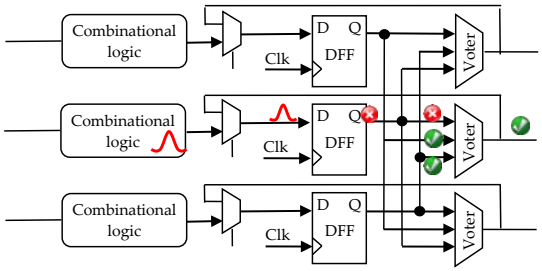
Overview of ECSS-Q-HB-60-02 contents

10 Digital circuits



10.3.1 **Spatial redundancy**
10.3.1.1 Duplex architectures
10.3.1.2 TMR architectures
10.3.1.2.1 Full, global, functional, large-grain TMR
10.3.1.2.2 Block, local TMR
10.3.2 **Temporal redundancy**
10.3.2.1 Triple Temporal Redundancy combined with spatial redundancy
10.3.2.2 Minimal level sensitive latch
10.3.2.3 Dual Temporal Redundancy
10.3.3 **Fail-Safe Finite State Machines**
10.3.4 **Memory Block mitigation** (bit interleaving, EDAC)
10.3.5 **Error Correction Codes**
10.3.5.1 Parity check
10.3.5.2 M-of-N code
10.3.5.3 Cyclic Redundancy Check
10.3.5.4 BCH codes
10.3.5.5 Hamming codes
10.3.5.6 SEC-DED codes
10.3.5.7 Reed-Solomon codes
10.3.5.8 Arithmetic codes
10.3.6 **Selective use of logic cells available in the vendor-provided library**
10.3.6.1 Rad Hard Flip-Flops
10.3.6.2 High drive (larger transistors) cells
10.3.7 **Buffers to filter SET pulses in data paths**
10.3.8 **Watchdog timers**
10.3.9 **Mitigation of FFT and FIR filters**

b)

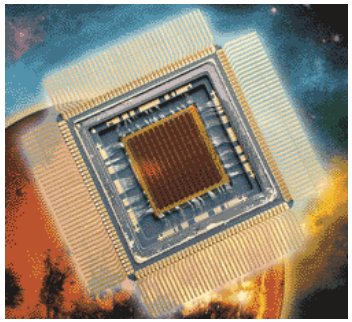


Overview of ECSS-Q-HB-60-02 contents

12 Field Programmable Gate Arrays

12.1 Scope
12.2 Table of effects vs mitigation techniques
12.3 Mitigation techniques
12.3.1 Reliability-Oriented Place and Route Algorithms
12.3.2 Scrubbing
12.3.3 Additional voters in TMR datapaths (domain crossing events)
12.3.4 FPGA TMR specific tools: Xilinx XTMR

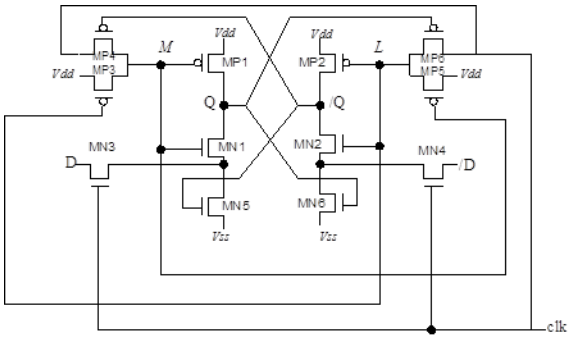
1. The rad-hard version of the Virtex-5QV FPGA has been qualified for high-radiation, deep-space applications.

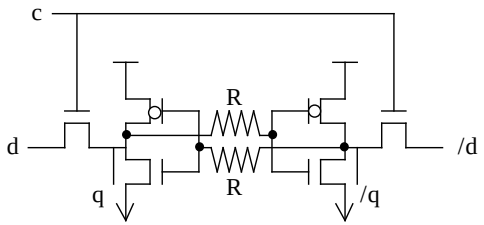


+ all techniques explained in Chapter 10 (Digital designs)

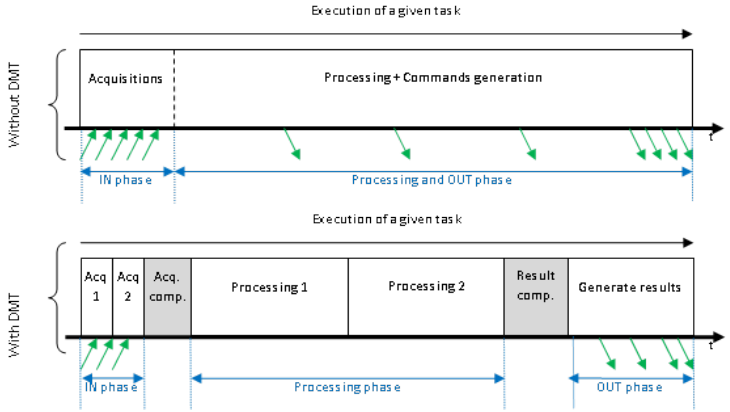
13 Embedded memories

13.1 Scope
13.2 Table of effects vs mitigation techniques
13.3 Mitigation techniques
13.3.1 Resistive hardening
13.3.2 Capacitive hardening
13.3.3 IBM hardened memory cell
13.3.4 HIT hardened memory cell
13.3.5 DICE hardened memory cell
13.3.6 NASA-Whitaker hardened memory cell
13.3.7 NASA-Liu hardened memory cell
13.3.8 Data scrambling





Overview of ECSS-Q-HB-60-02 contents



14 Embedded software

14.1 Scope

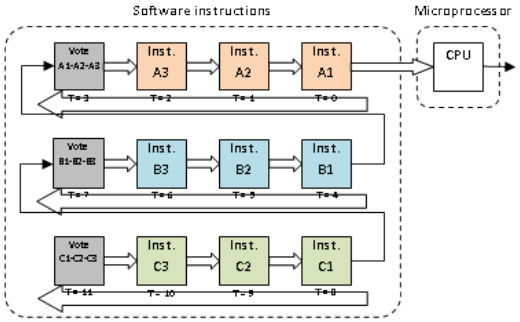
14.2 Table of effects vs mitigation techniques

14.3 Mitigation techniques

14.3.1 Redundancy at instruction level

14.3.2 Redundancy at task level

14.3.3 Redundancy at application level



Overview of ECSS-Q-HB-60-02 contents

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15.3.2 Watchdog timers
15.3.3 Latching current limiters
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15.3.6 Error Correcting Codes
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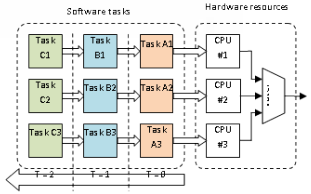
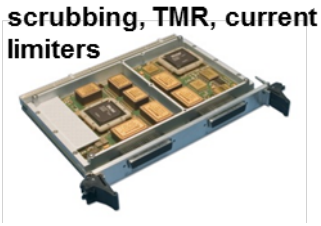
15.4 Commercial solutions
15.4.1 Space Micro Proton platform
15.4.2 Maxwell SCS750
15.5 Examples of adopted architectures on-board satellites
15.5.1 Architecture for the MYRIADE satellite
15.5.2 Architecture for the REIMEI (INDEX) satellite
15.5.3 Architecture for the CALIPSO satellite





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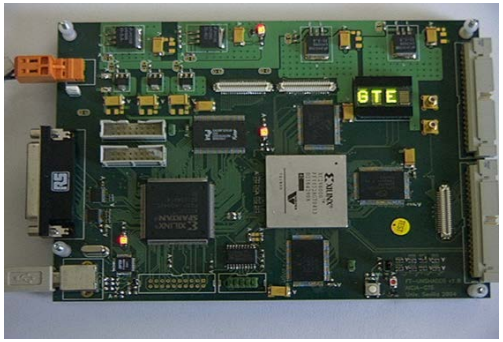
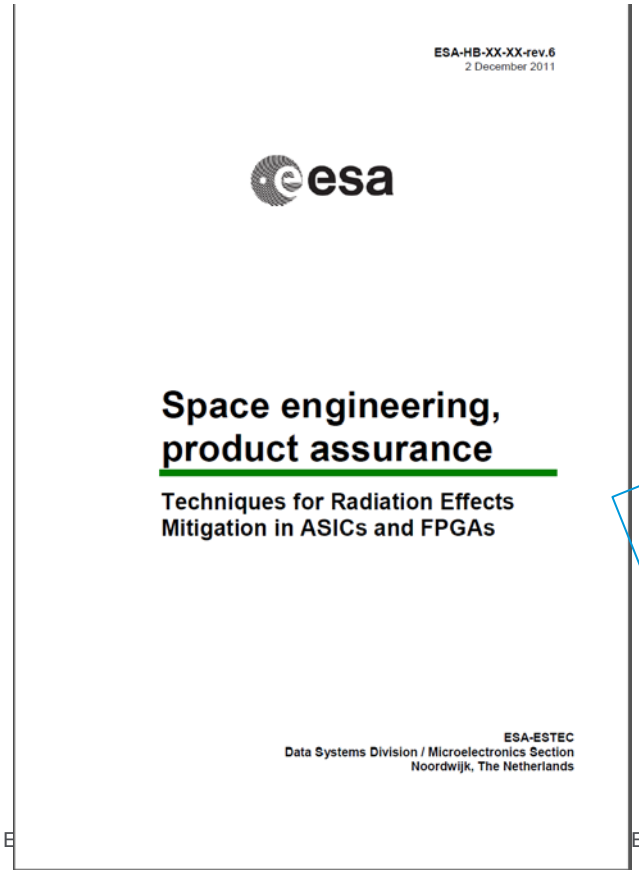
16.4.2 Test methodologies
16.4.3 Test facilities
16.4.4 Practical constraints
16.4.5 DUT preparation
16.5 Fault injection
16.5.1 Fault injection at transistor level
16.5.2 Fault injection at gate level
16.5.3 Fault injection at device level
16.5.4 Fault injection at system level
16.6 Analytical methods



ECSS-Q-HB-60-02 : the first draft

02-Dec-2011 presented at ESTEC, and distributed on-line as .pdf and as a book:

http://microelectronics.esa.int/handbook/HB_Radiation_Hardening_2011-12-02.pdf



Version 6

ECSS HB Working Group starting point:

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- 2 Normative references
- 3 Definitions and acronyms
- 4 Organisation and purpose

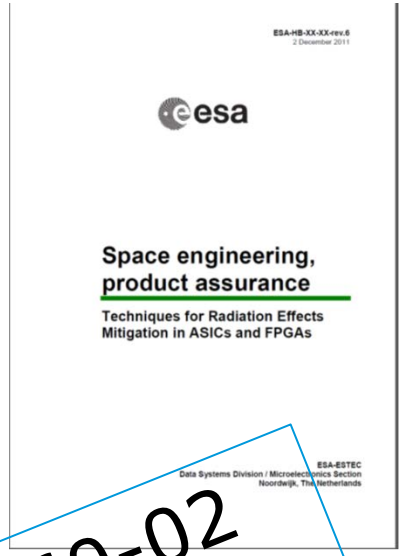
10 pages
- 5 Radiation environment and integrated circuits

1 page
- 6 Choosing a design hardening strategy

155 pages
- 7 Technology selection and process level mitigation
- 8 Layout
- 9 Analogue circuits
- 10 Digital circuits
- 11 Mixed-signal circuits
- 12 Field Programmable Gate Arrays
- 13 Embedded memories
- 14 Embedded software
- 15 System architecture

15 pages
- 16 Validation methods

Annex A References



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(Feb 2012)

HB WG review in steps: 5 BLOCKs

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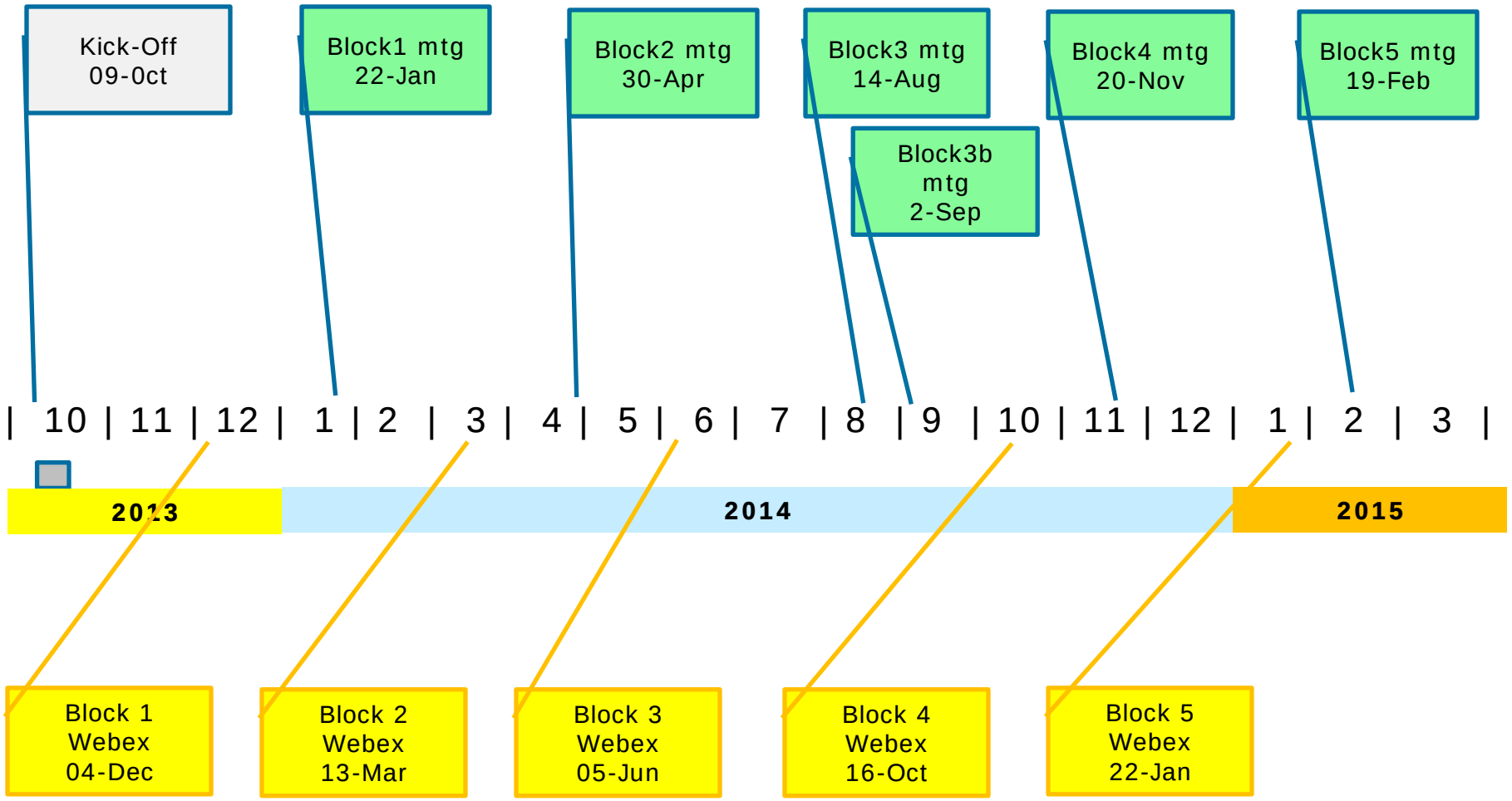
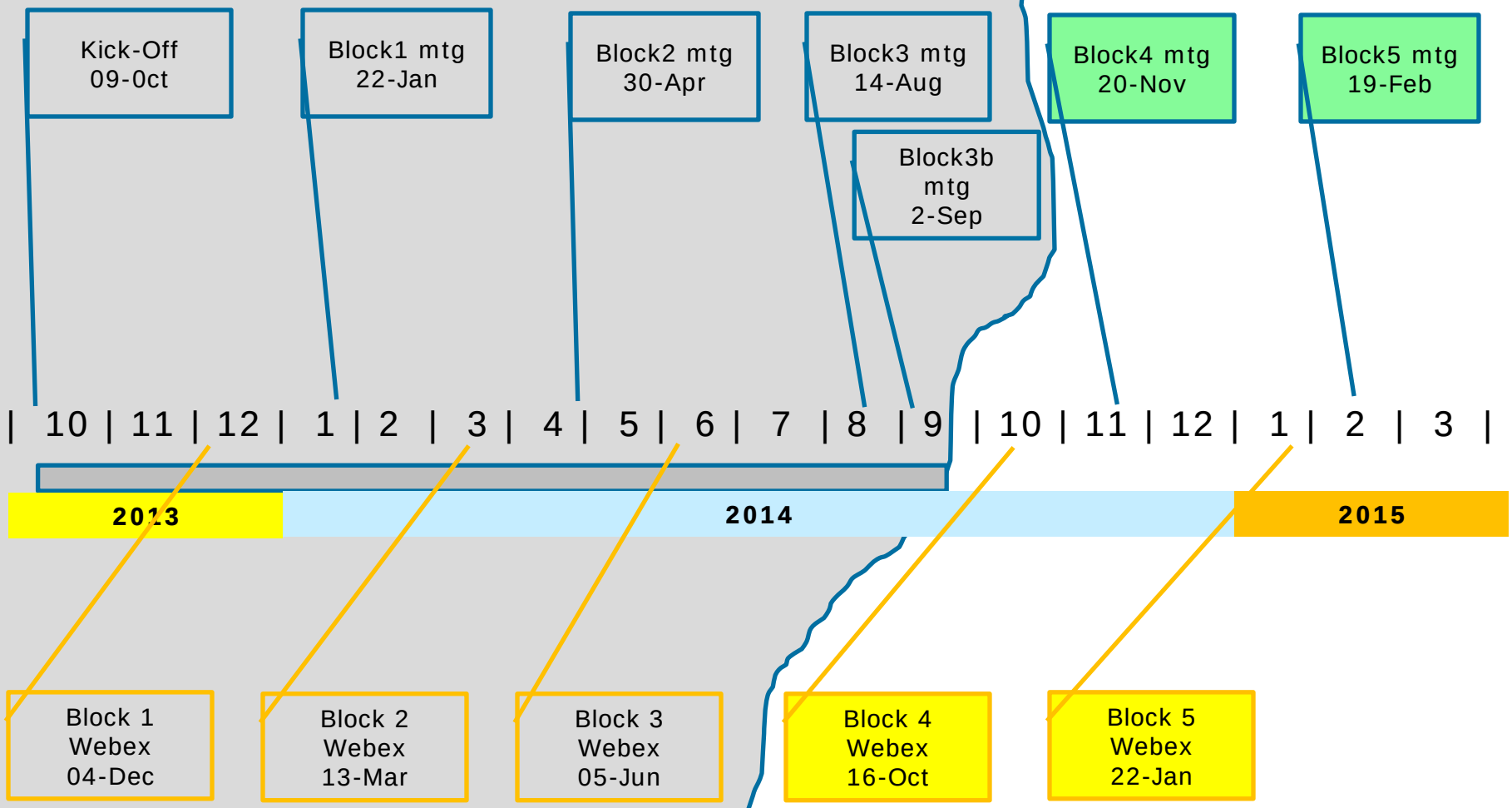
15 pages		16 Validation methods **-> Block 5**
		Annex A References **-> Block 5**

HB WG Review plan: 12 meetings, 1.5 yrs



HB WG Review plan



“requests for changes” so far by HB WG

not discussed yet	41
open*	195
closed*	200
Total	436

Future of ECSS-Q-HB-60-02

2014 : ECSS Working Group preparing a new, improved HB draft for …

➔ **Your suggestions welcome !**

2015/03: ECSS-Q-HB-60-02 release for ECSS "**public review**"

➔ **Your last opportunity to propose changes !!**

2015/Q3: ECSS-Q-HB-60-02 **final release** as a new ECSS handbook

THANKS, Questions? Suggestions?

ECSS-Q-HB-60-02

“Techniques for Radiation Effects Mitigation in ASICs and FPGAs”