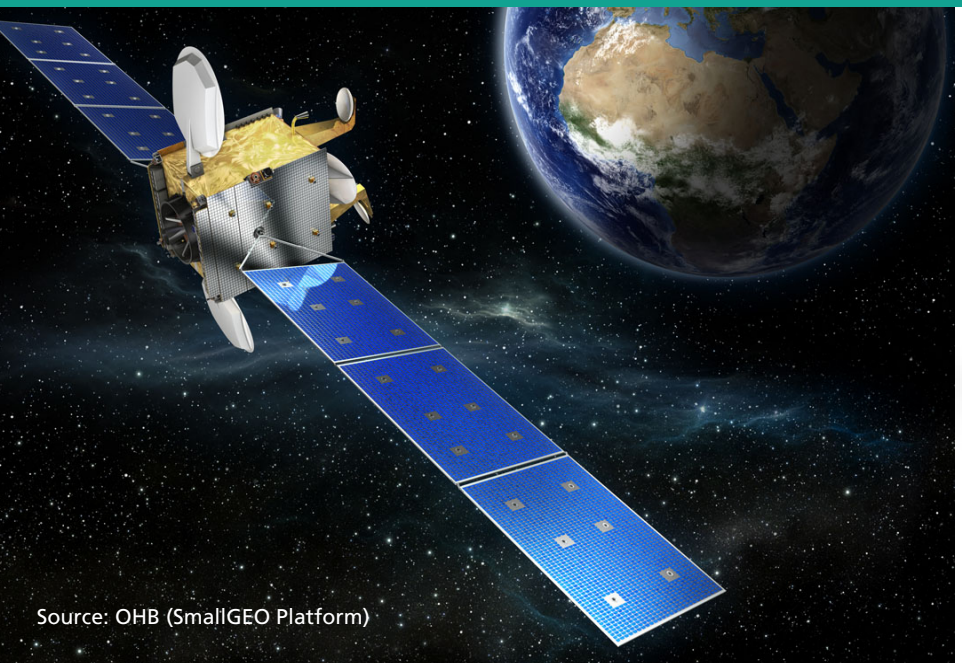
BRAM RADIATION SENSOR FOR A SELF-ADAPTIVE SEU MITIGATION

BRAM – Block RAM
SEU - Single Event Upset

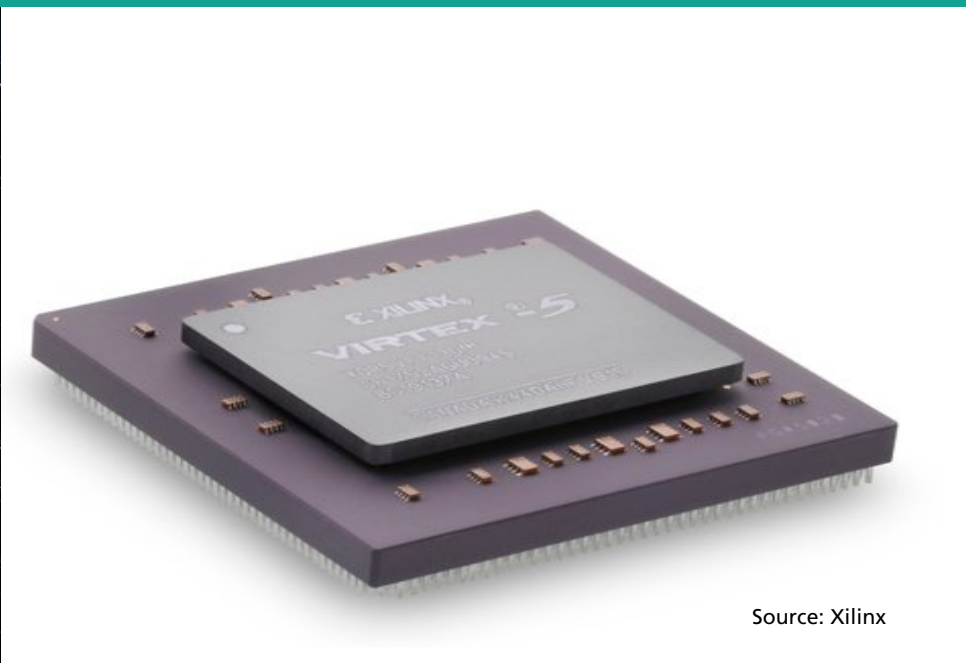
SpacE FPGA Users Workshop, 2nd Edition

Robért Glein, September 18th, 2014

Friedrich-Alexander-Universität Erlangen-Nürnberg (FAU) and Fraunhofer IIS

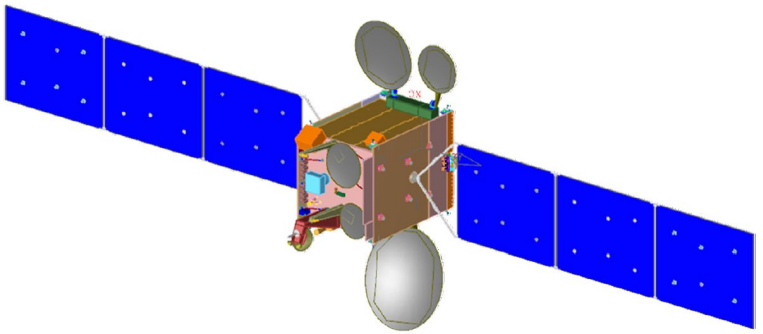


Source: OHB (SmallGEO Platform)



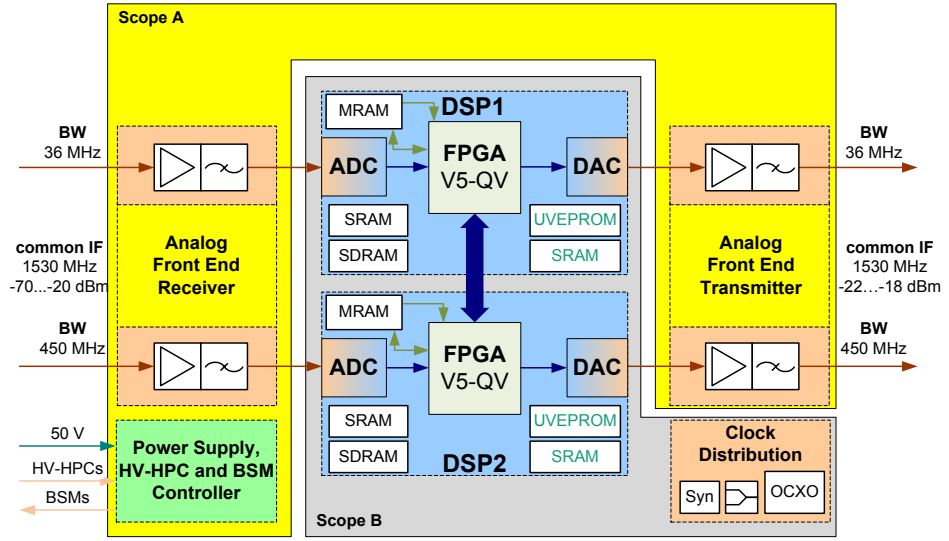
Source: Xilinx

Motivation: FOBP on the Heinrich Hertz Satellite Mission



Source: OHB (SmallGEO Platform)

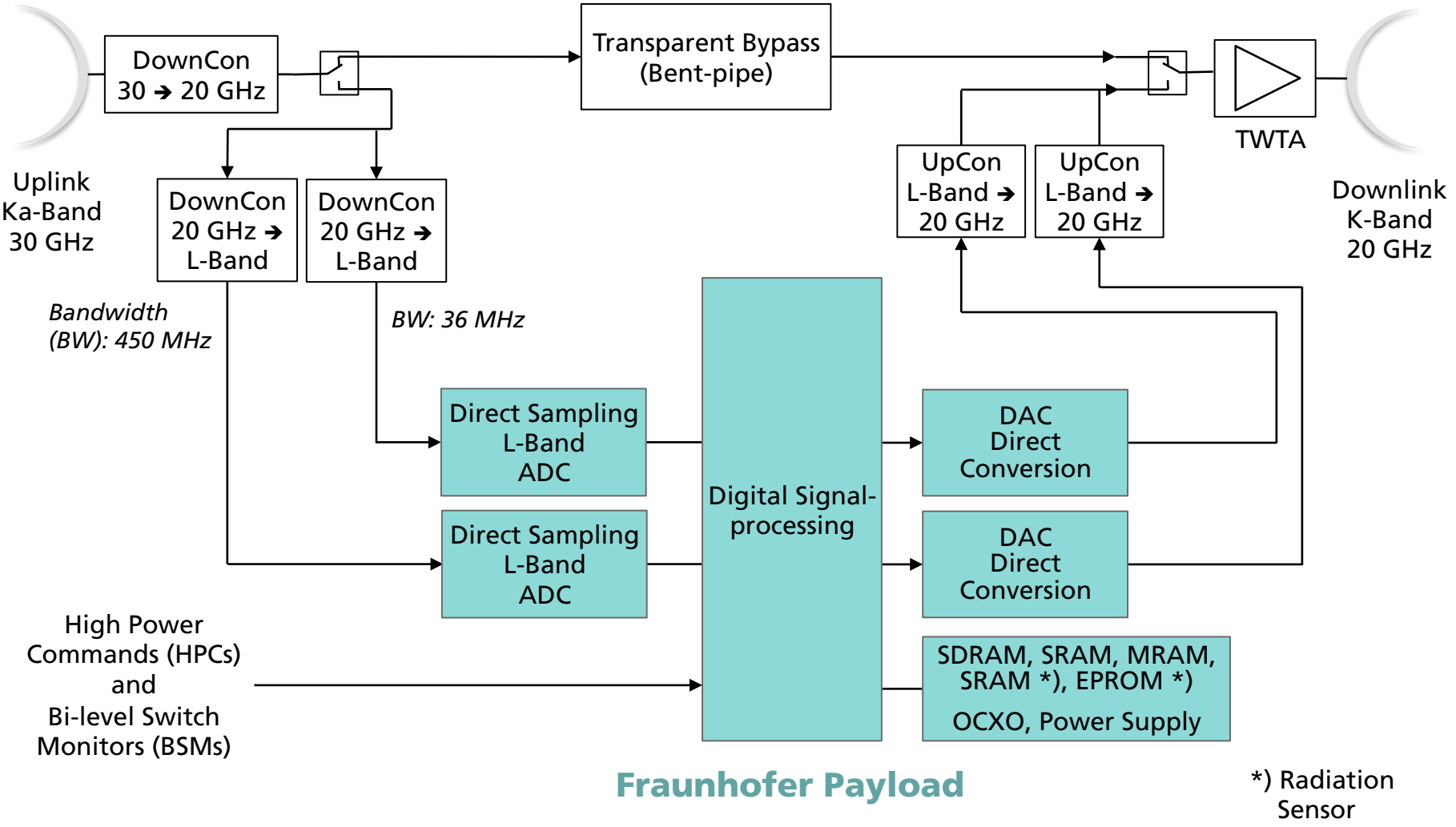
- Heinrich Hertz Satellite
  - German experimental communication satellite in GEO (35876 km)
  - Satellite will be launched in **2018/19** and located at 17.6 ° East
  - ~50 % **scientific** (experimental) payload and ~50 % military payload
- Fraunhofer On-Board Processor (**FOBP**) is part of the in-orbit verification payload
  - Regenerative Trans-ponder with **two** reconfigurable **Virtex-5QV** FPGAs
  - Channel Bandwidth:
    - Ch1: 36 MHz
    - Ch2: **450 MHz**



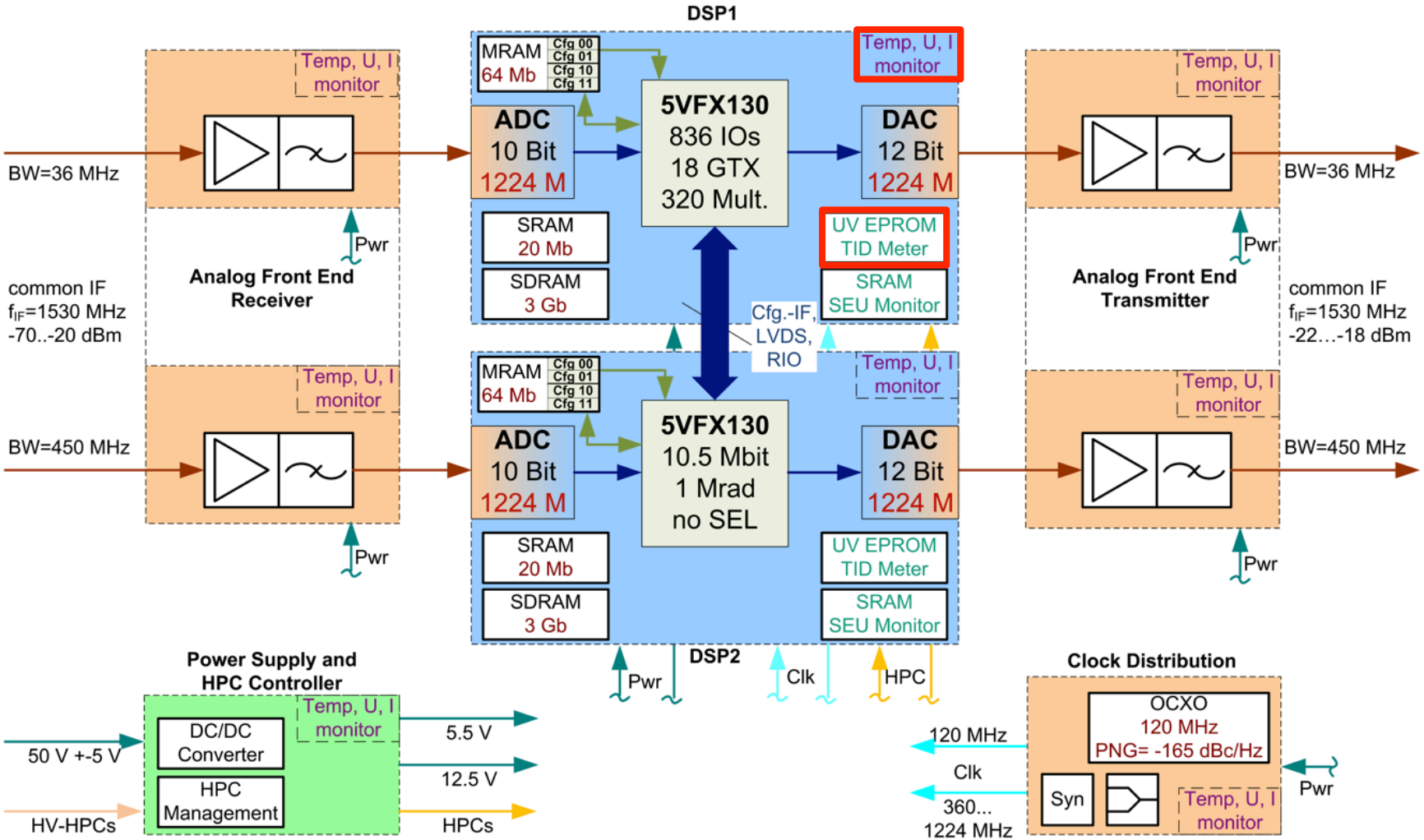
OUTLINE

- **Motivation and Project Update**
- **FPGA Configuration**
- SEU and Mitigation Problem
- FPGA Reliability Analysis
  - Device Level: Virtex-5QV Results
  - Design Level: Firmware
- Self-Adaptive SEU Mitigation System via BRAM Radiation Sensor
  - BRAM Particle Sensor
  - Measurement and Upset Rate Mapping
  - Self-Adaptive Application of Mitigation
- Outlook and Conclusion

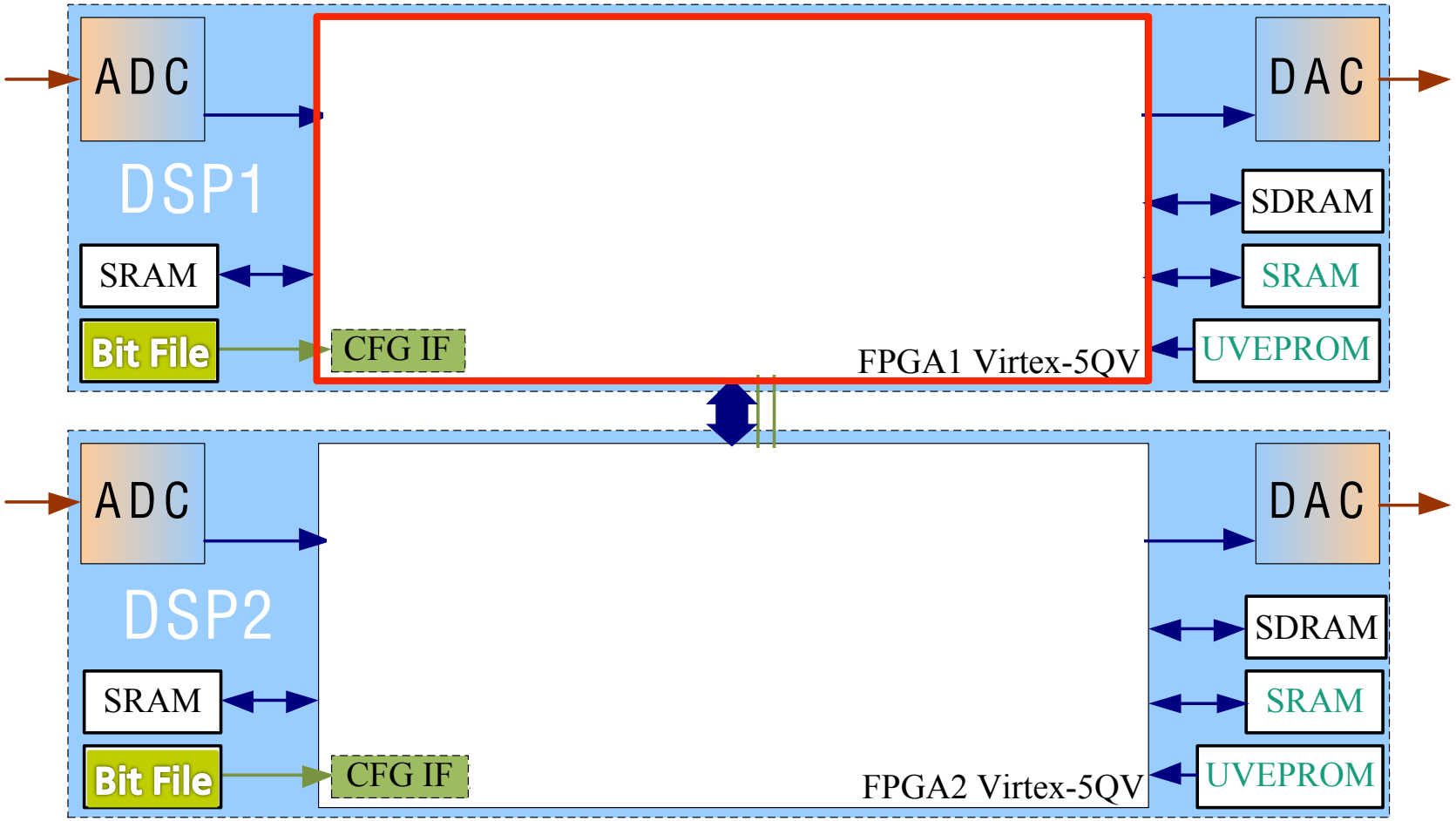
Fraunhofer On-Board Processor (FOBP) on Heinrich Hertz Fraunhofer Payload



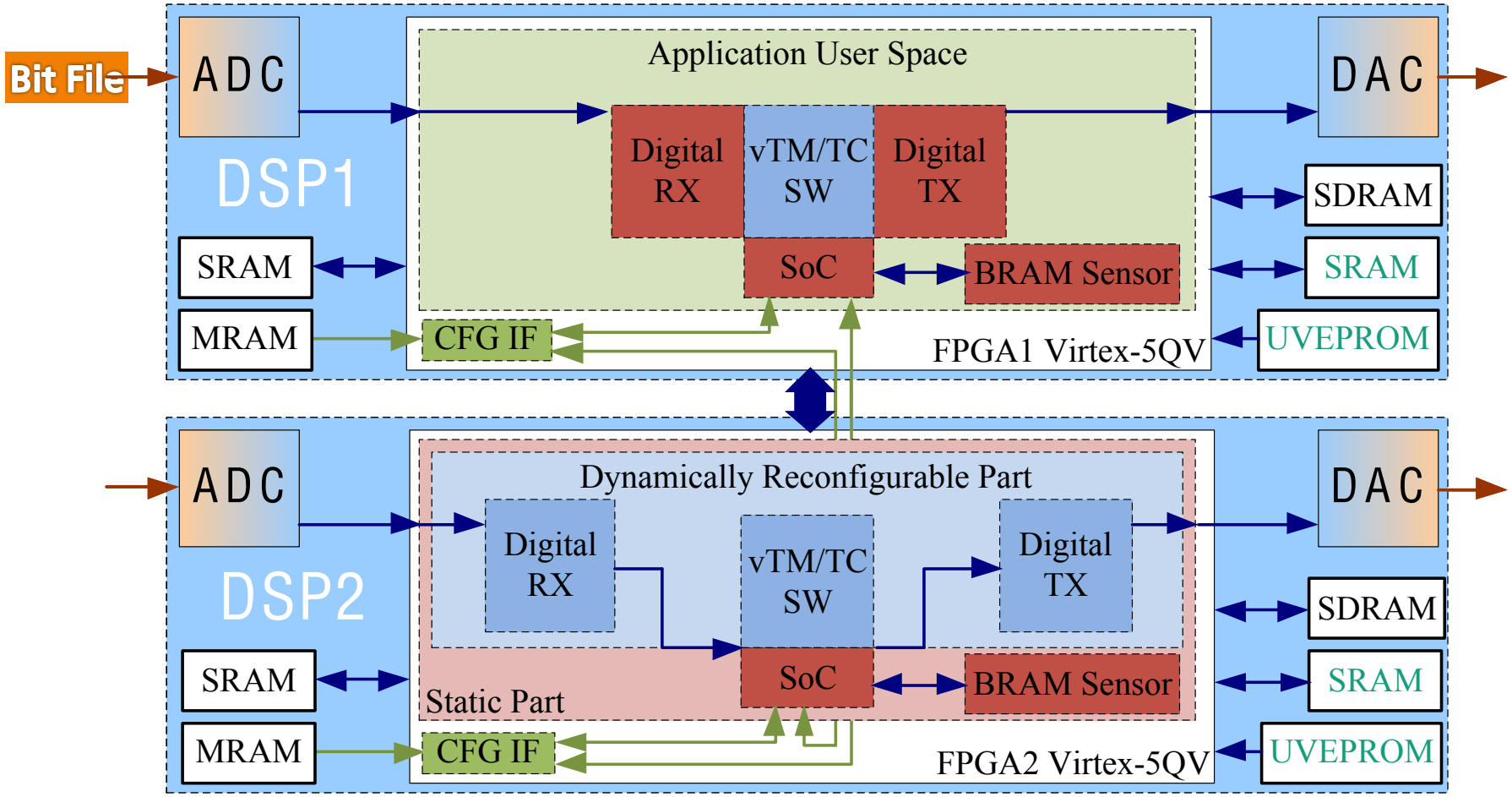
Fraunhofer On-Board Processor (FOBP) Details
Block Diagram



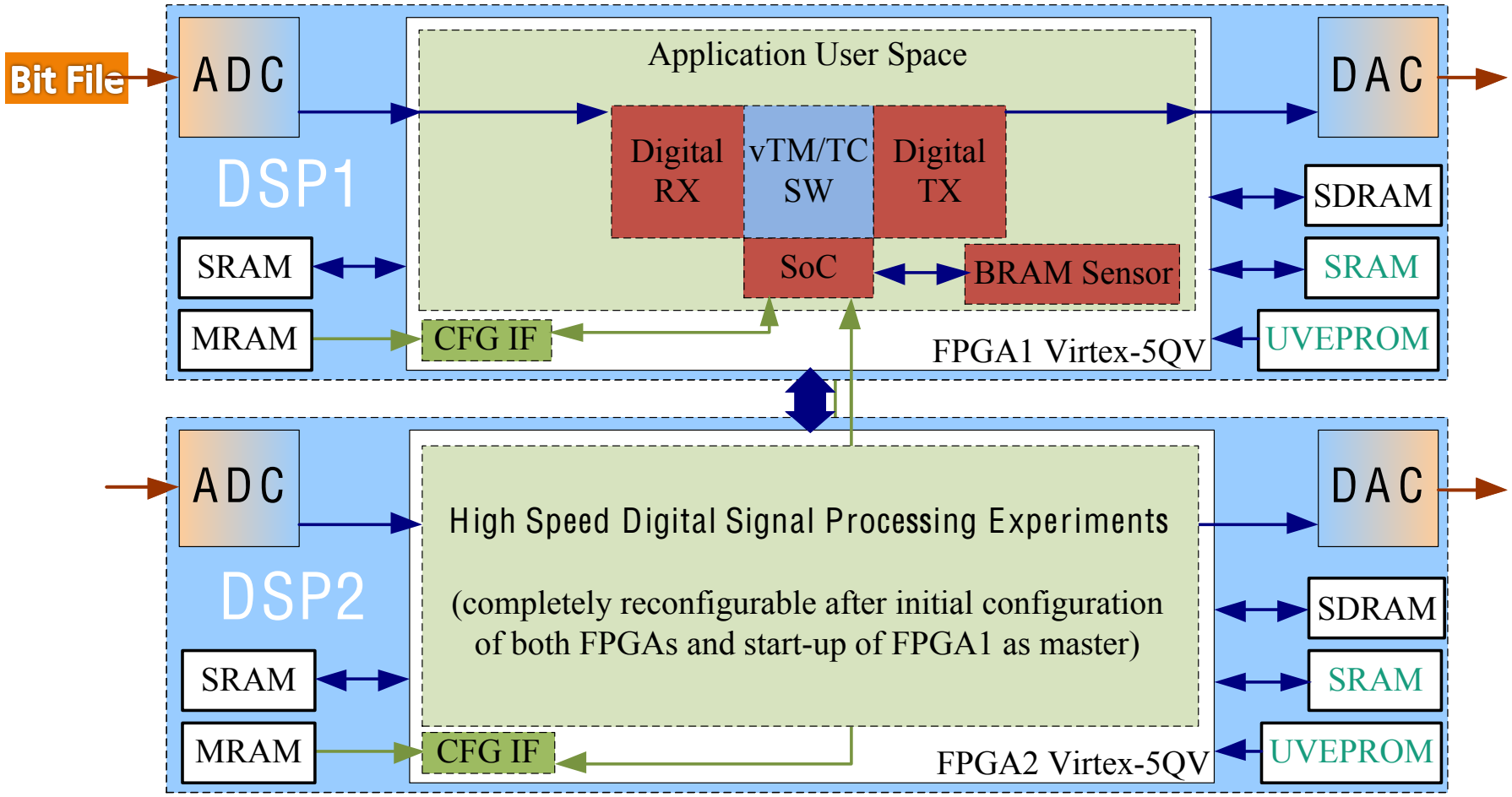
FPGA Configuration [3]
FOBP Initial State and Master Determination



FPGA Configuration
Master FPGA Reconfiguration (FOBP Control Part)



FPGA Configuration
Slave FPGA Reconfiguration (Broadband DSP Part [2])



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  - Upset Rate Mapping
  - Self-Adaptive Application of Mitigation
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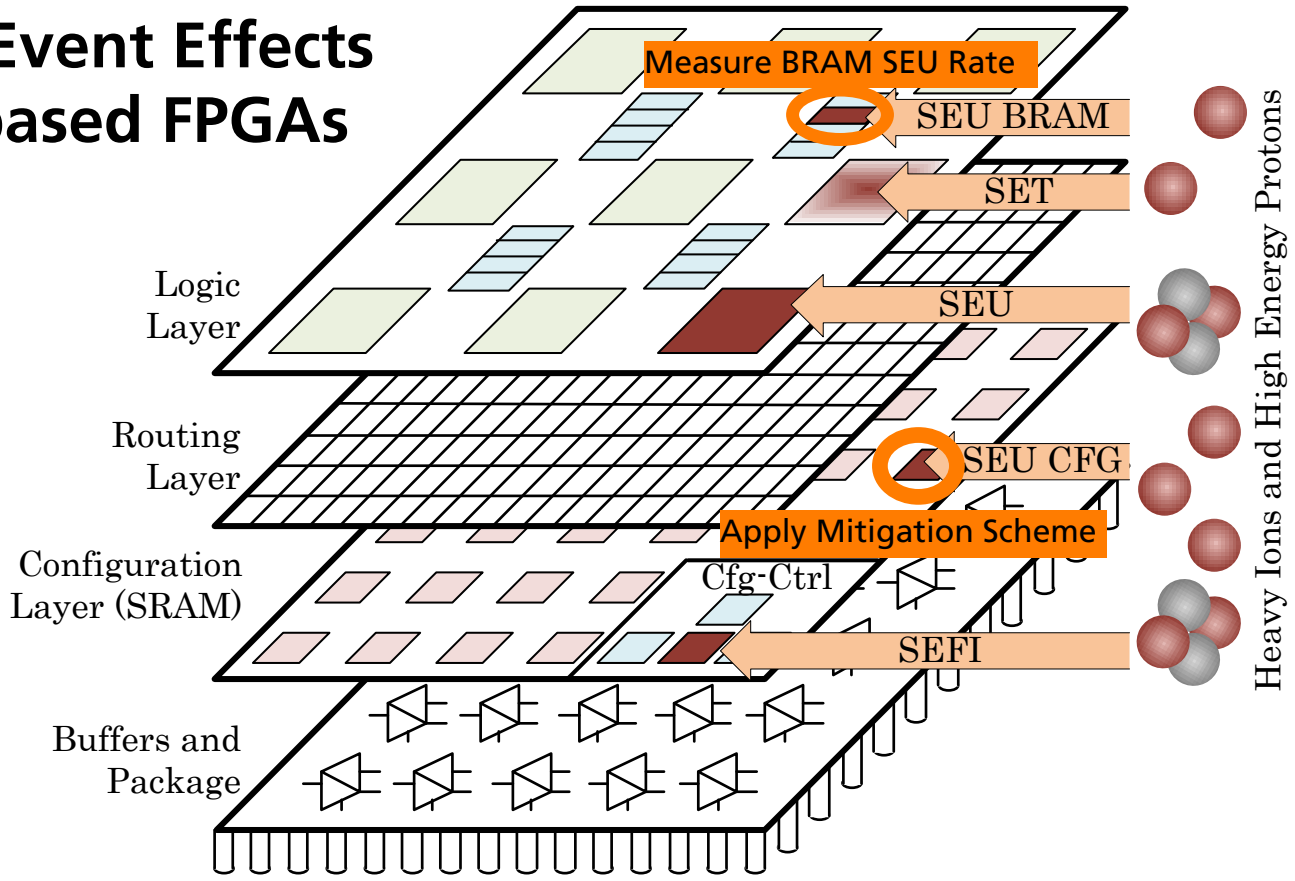
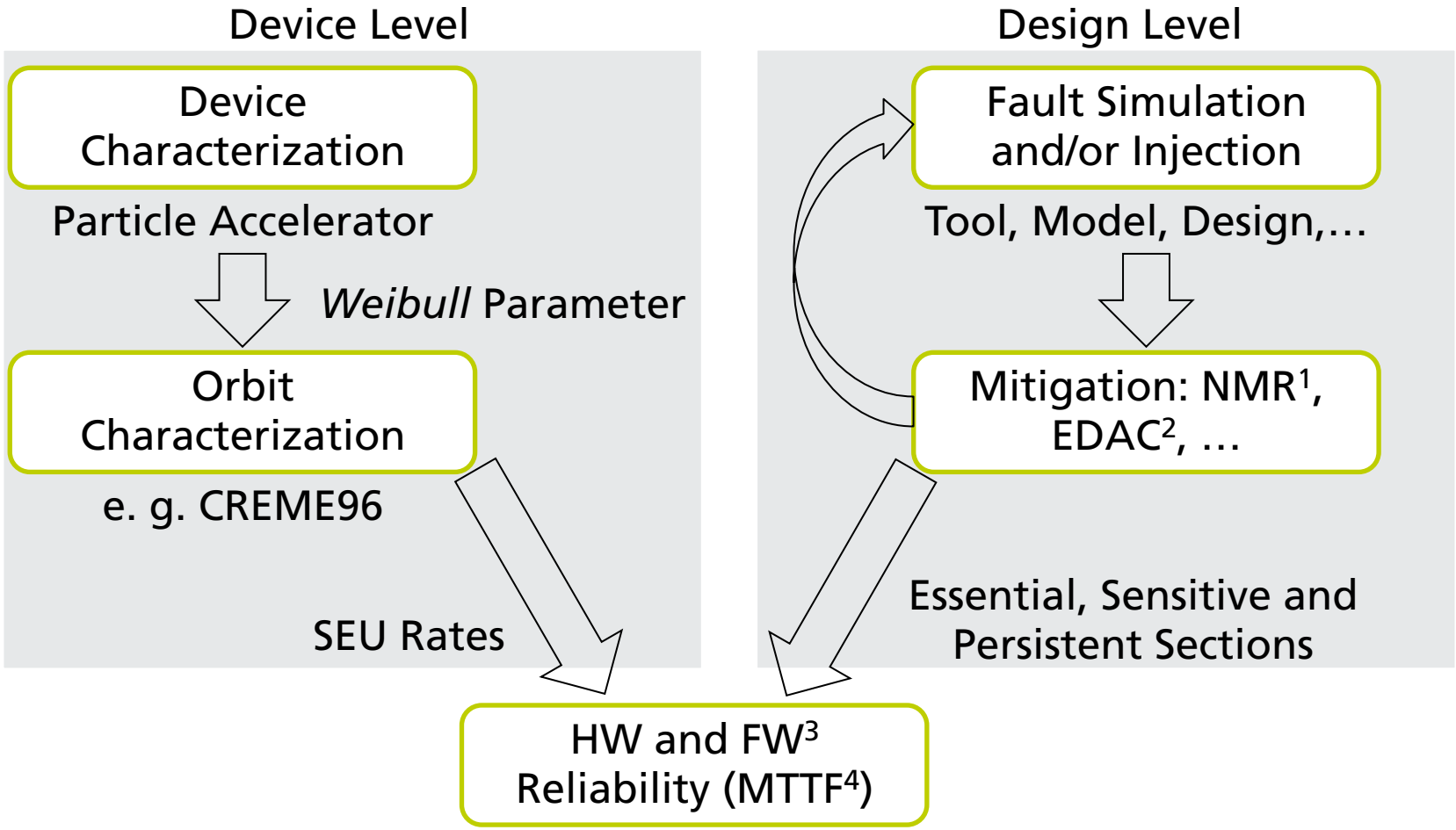
Problem: Single Event Effects (SEEs) in SRAM based FPGAs

- SEL (Single Event Latch-up) immune
- SEFI (Single Event Functional Interrupt)
- **SEU (Single Event Upset)**
  - SEU CFG (configuration)
- SET (Single Event Transient)



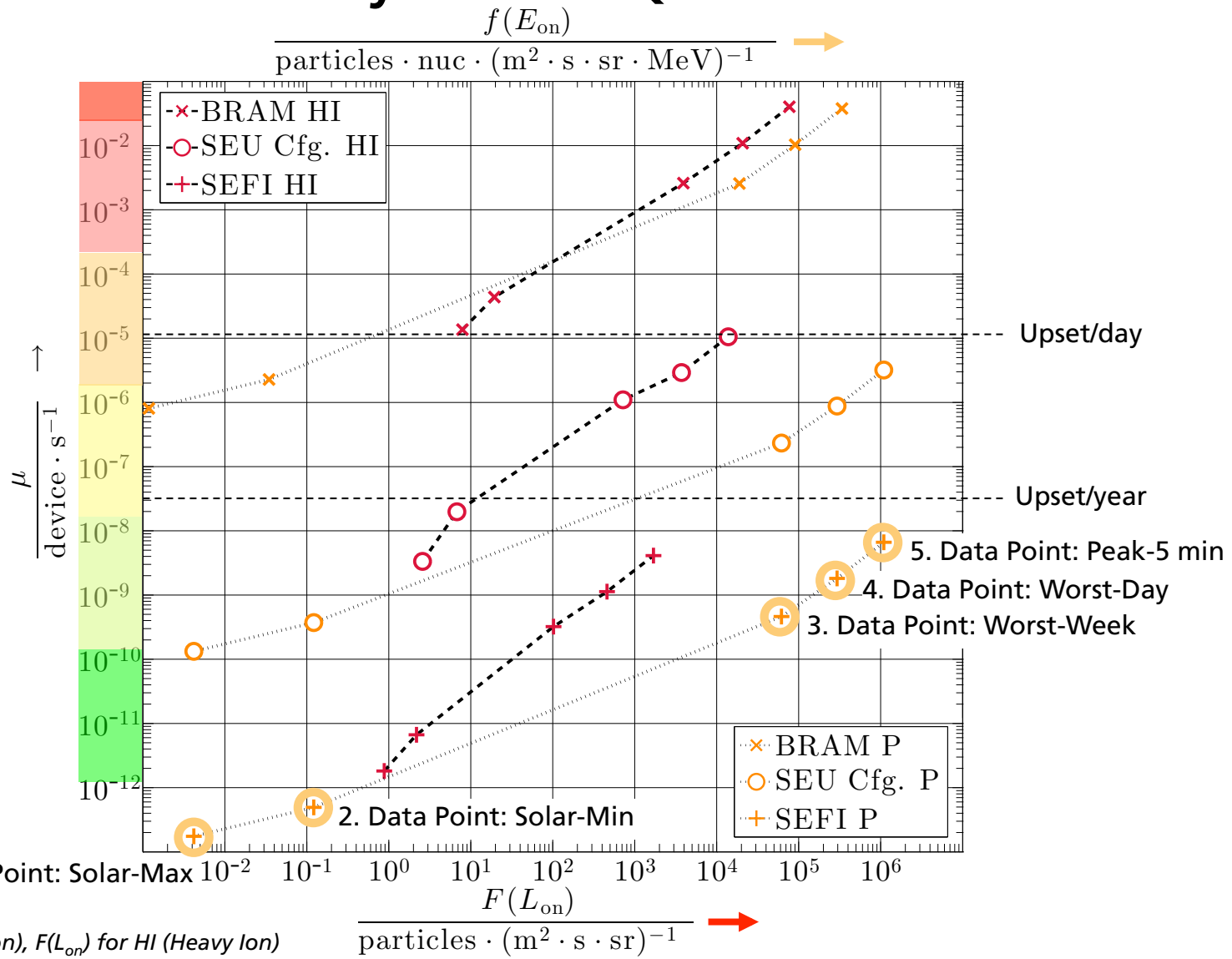
- **Resource consumption** of mitigation schemes such as
  - N-times Modular Redundancy (NMR: DMR or DWC, TMR, …)
  - Algorithm-Based Fault Tolerance (ABFT), …
- → Goal: **Adaptive Mitigation** (only use redundancy when needed)

FPGA Reliability Analysis
Device Level: Virtex-5QV



1) N-times Modular Redundancy 2) Error Detection and Correction 3) Firmware 4) Mean Time to Failure

Device Level Reliability: Virtex-5QV FPGA SEU Rate I



f(E$_{on}$) for P (Proton), F(L$_{on}$) for HI (Heavy Ion)

Device Level Reliability: Virtex-5QV FPGA SEU Rate II

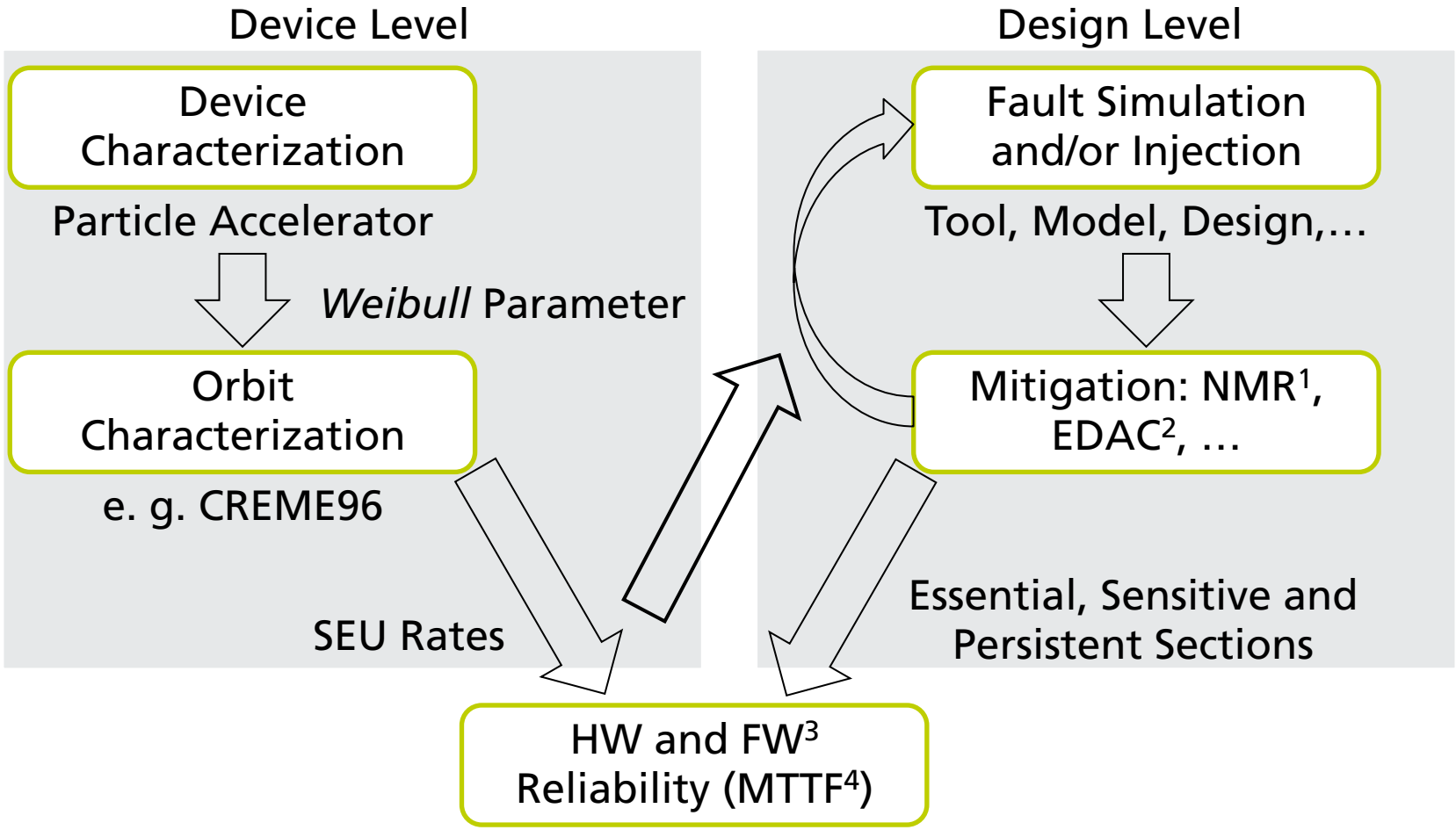
Virtex-5QV	*Solar-Minimum* Upset/day/device	Solar-Maximum Upset/day/device	*Worst-Week* Upset/day/device	Worst-Day Upset/day/device	*Peak-5* Upset/day/device
SEFI (TMR CFG Contoller + Voter)	6.167E-07	1.728E-07	6.777E-05	2.542E-04	9.279E-04
SEU CFG (CFG Memory)	1.743E-03	3.007E-04	1.149E-01	3.282E-01	1.185E+00
BRAM (Block Memory Bits)	3.968E+00	1.248E+00	4.460E+02	1.837E+03	6.743E+03
FF (Transient filter off)	3.826E-03	9.188E-04	3.056E-01	1.070E+00	3.900E+00
FF (Transient filter on)	2.734E-02	6.426E-03	1.329E+00	4.130E+00	1.501E+01
DSP (M-REG)	1.268E-01	4.497E-02	1.196E+02	4.699E+02	1.713E+03
DSP (other)	2.801E-01	9.921E-02	2.618E+02	1.027E+03	3.746E+03

Overall upset rates μ of the Virtex-5QV in GEO with 4.5 mm AL shielding

- BRAM will be mitigated via ECC[1]
- FFs and DSPs[2] criticality depends highly on the design (feedback, filter, ...)
- Analysis for CMTs[3], MGTs[4] and IOBs[5] available

[1] Error Correction Code [2] 25x18 bit Multiplier [3] Clock Management Tile [4] Multi Gigabit Transceiver [5] Input Output Buffer

FPGA Reliability Analysis
Design Level: Firmware

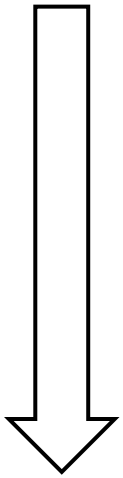


1) N-times Modular Redundancy 2) Error Detection and Correction 3) Firmware 4) Mean Time to Failure

Self-Adaptive SEU Mitigation Instrument

Goal:
Minimization of radiation caused effects in reconfigurable FPGAs

Instrument:



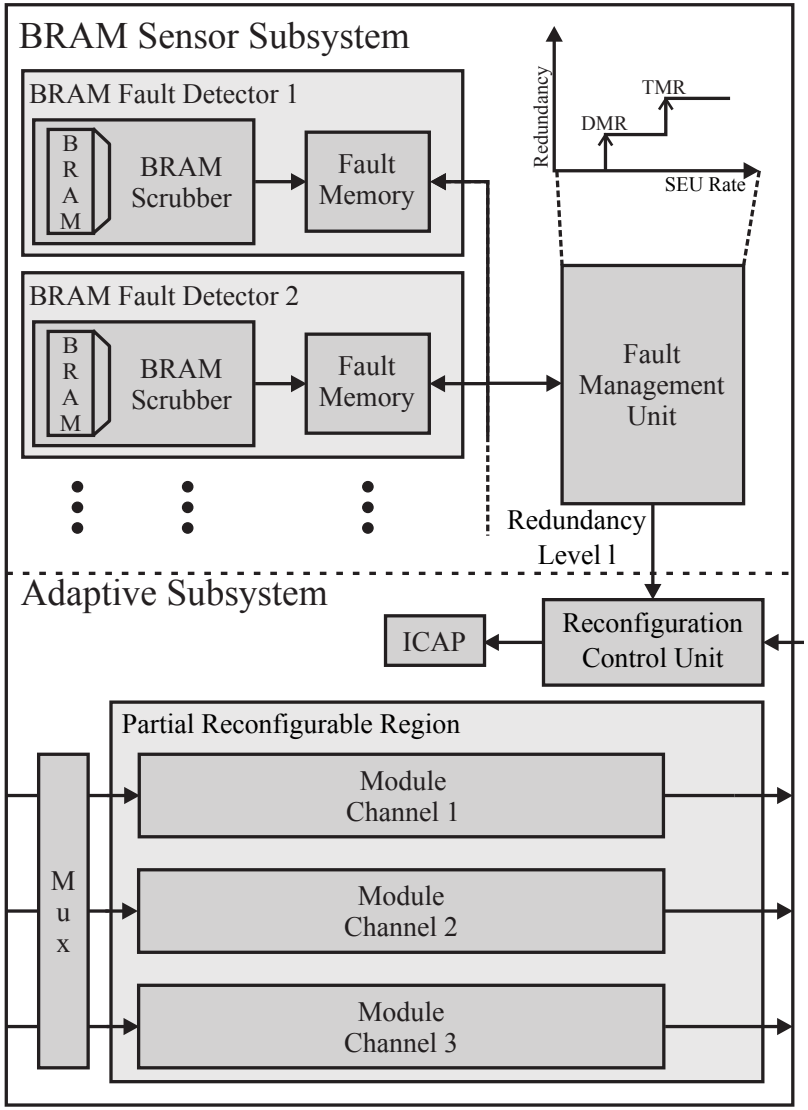
BRAM inside the FPGA

- **High radiation sensitivity**
- **No additional HW needed**
- **Point of interest**
- **Scalable by BRAM primitive count**
- **Easy access**

→ Applying an optimal redundancy at runtime

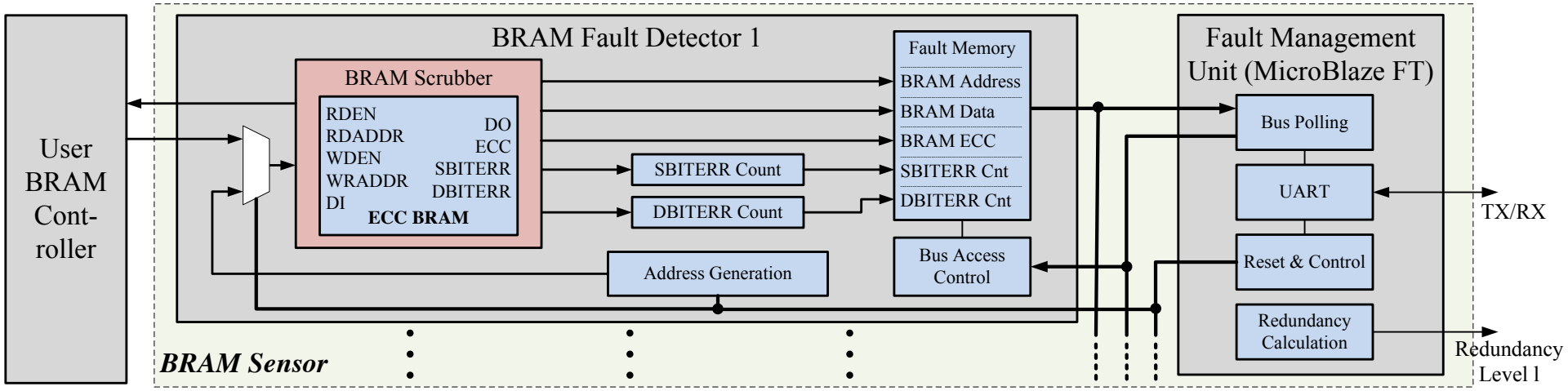
Self-Adaptive SEU Mitigation System Overview

- Self-adaptive SEU mitigation system for FPGAs (only SEU CFG)
- Enabled by an **internal block RAM (BRAM) radiation particle sensor** and dynamic partial reconfiguration
- **Triplicate** the data throughput **at the *Solar Maximum*** condition (no flares) compared to TMR[1]
- Decrease the probability of failures per hour by **$2x10^4$ at flare-enhanced** conditions compared with a non-redundant system



[1)] *Triple Modular Redundancy*

Self-Adaptive SEU Mitigation
BRAM Sensor



- BRAM fault detector is a wrapper for an BRAM primitive (512 x 72 bit) with ECC[1] (64 bit + 8 bit)
  → single bit error correction, double bit error detection
- BRAM can be **accessed by the user** (has to guarantee a reading of all addresses all few seconds) or a address counter will be instantiated
- 64 BRAMs (out 298 in the Virtex-5QV) enable one upset every minute for the *Peak 5 Minutes* (GEO with 4.5 mm AL shielding)

[1] Error Correction Code

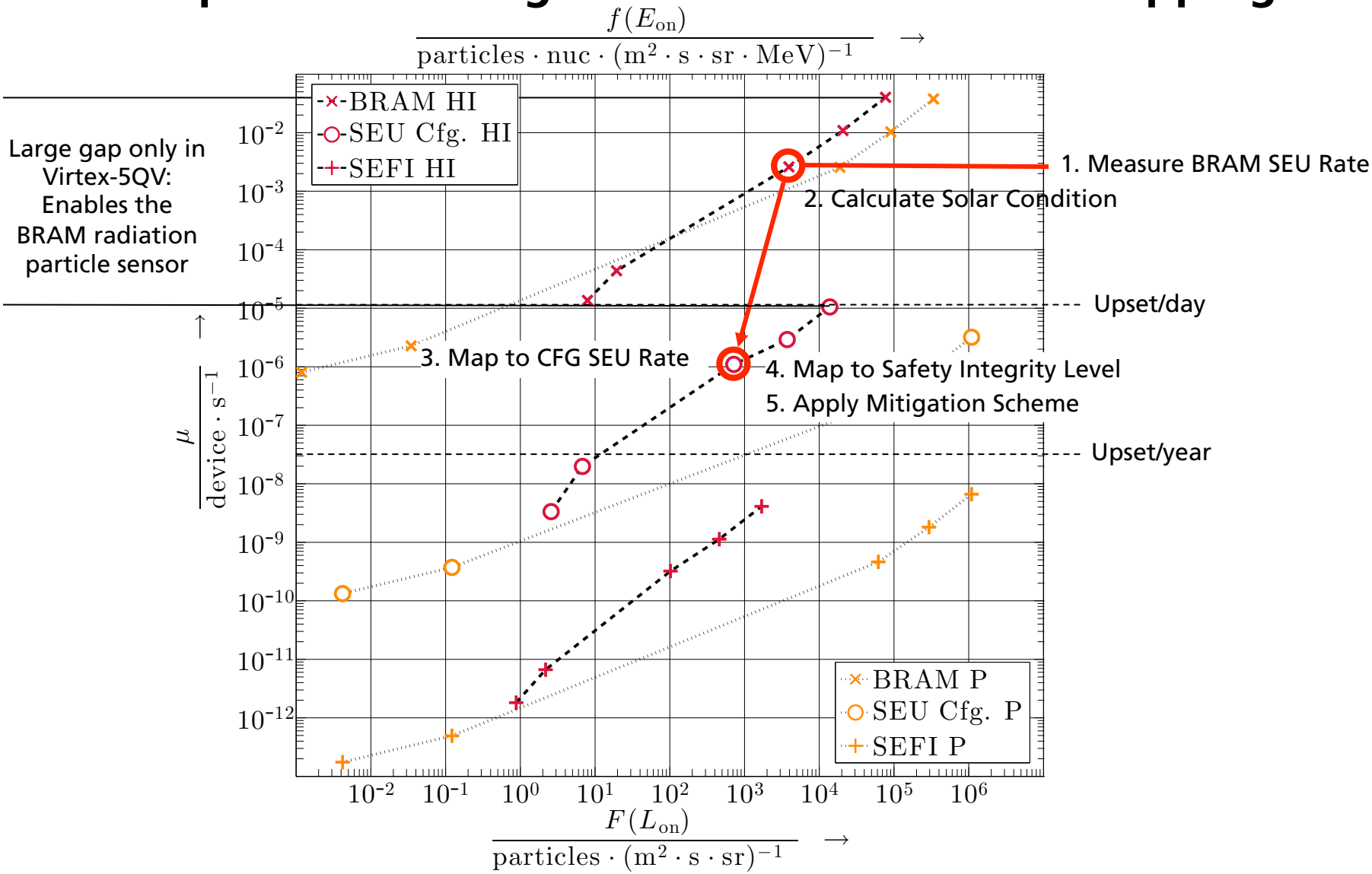
Self-Adaptive SEU Mitigation
Solar Flares Definition and Characteristic

- Definition: 3 values ≥ 10^5 particles•m^{-2}•sr^{-1}•s^{-1} of proton flux (5-minute averages) for energies >10 MeV
- Duration: 15 minutes to several days
- Measured by GOES (Geostationary Operational Environmental Satellite)
- Occurrence: 0...30 flares per year (trend follows sun cycle)
  - Rising time to the maximum flux from minutes to days
  - Reference flare (20th Oct 1989):
    Second highest proton flux 4•10^8 particles•m^{-2}•sr^{-1}•s^{-1}
  - 259 flares occurred from 1976 to now
- Heavy ion instrument planned (launch in 2016)

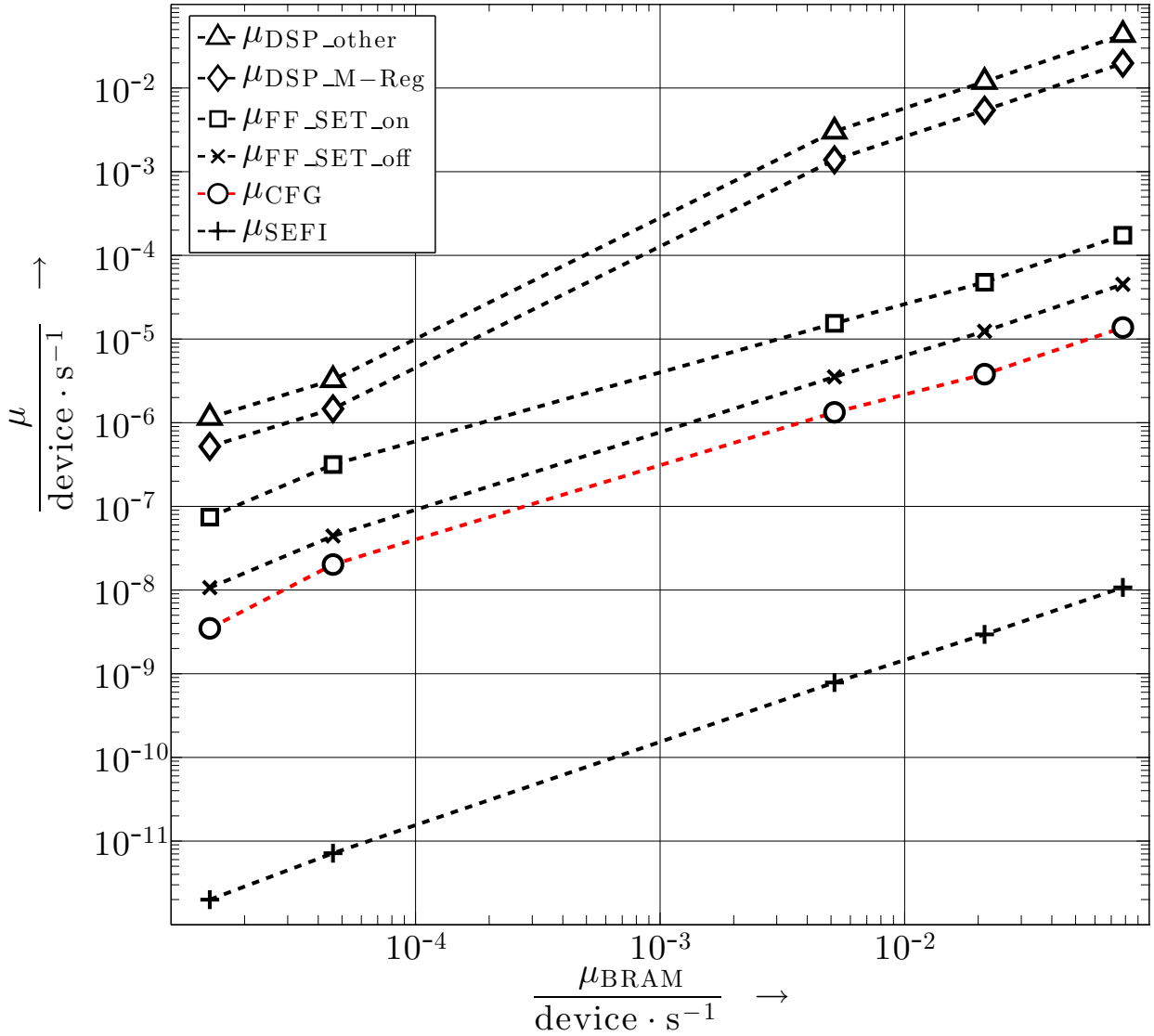
Self-Adaptive SEU Mitigation
BRAM Mean Time to Upset (MTTU) Measurement

- Measurement
  - Averaging three measured mean time to upset values
  - Windowing of the last tree BRAM SEUs
- Multiple-Bit Upset (MBU)
  - Two or more bits of one BRAM primitive are corrupted during a memory scrubbing cycle (a few seconds) → interpreted as MBU
- Promising results on modeling measurement with *Petri Nets*
  - X1 solar flare: 11/12 Sep. 2014
    - Peak flux: $4 \cdot 10^6$ particles$\cdot m^{-2} \cdot sr^{-1} \cdot s^{-1}$ (> 4 MeV ≈ E_{on} for the BRAM) which is just under the worst week condition
    - Detection in 1…2 h of this 40 h flare (probability of 95 %, depending on starting condition)

Self-Adaptive SEU Mitigation: BRAM SEU Rate Mapping

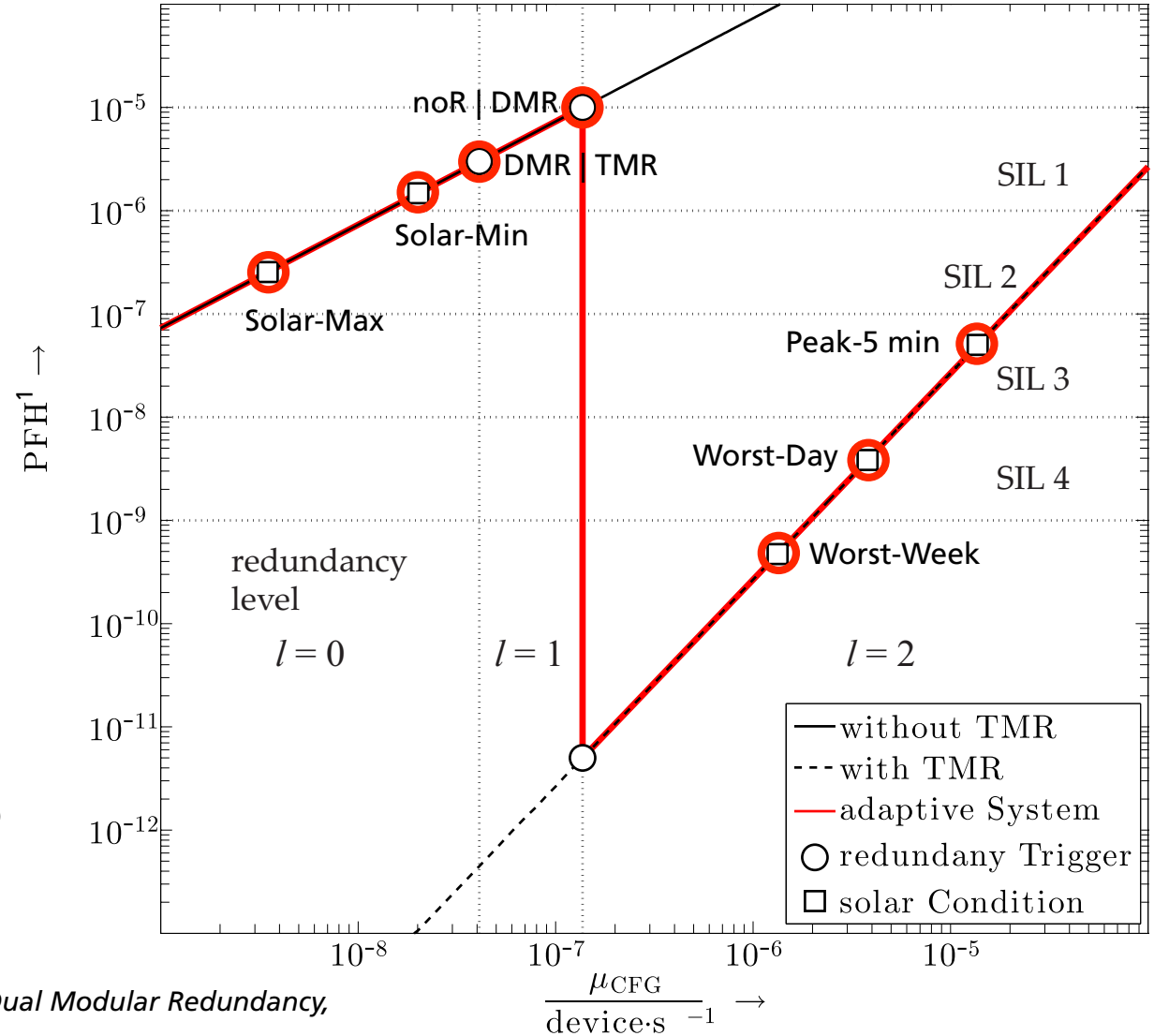


Self-Adaptive SEU Mitigation: BRAM SEU Rate Mapping II



Self-Adaptive SEU Mitigation: Case Study I

- According to the safety integrity level (SIL) the system configures with:
  l=0: noR,
  l=1: DMR[2] or
  l=2: TMR[3]
- DMR only for fault detection
- TMR increases the reliability dramatically due to scrubbing (60 s)



[1] Probability of Failures per Hour, [2] Dual Modular Redundancy, [3] Triple Modular Redundancy

Self-Adaptive SEU Mitigation: Case Study II

a
$$\lambda_m = \mu_{CFG} \cdot \frac{n_{e,m}}{n_{FPGA}}$$

b
$$R_m(t) = e^{-\lambda_m \cdot t}$$

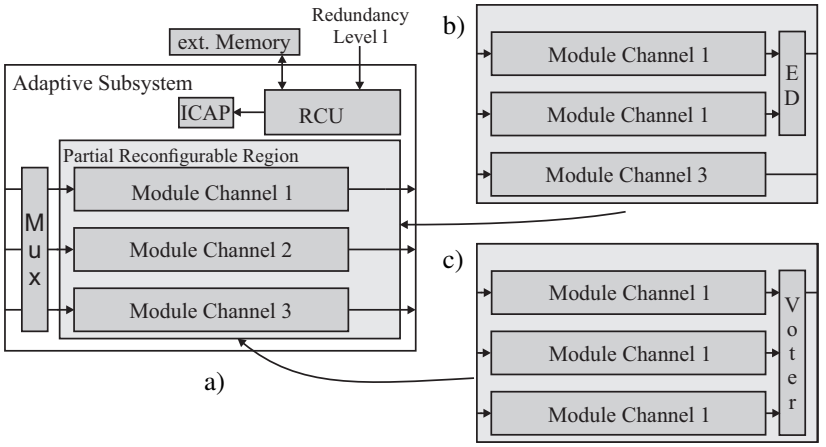
$$PFH = 1 - R_m(T_h) \text{ with } T_h = 3600s$$

c
$$R_m^{TMR}(t) = 3R_m(t)^2 - 2R_m(t)^3$$

$$\lambda_m^{TMR,s} = \frac{1 - R_m^{TMR}(t)}{t_s} \quad \text{(approximation)}$$

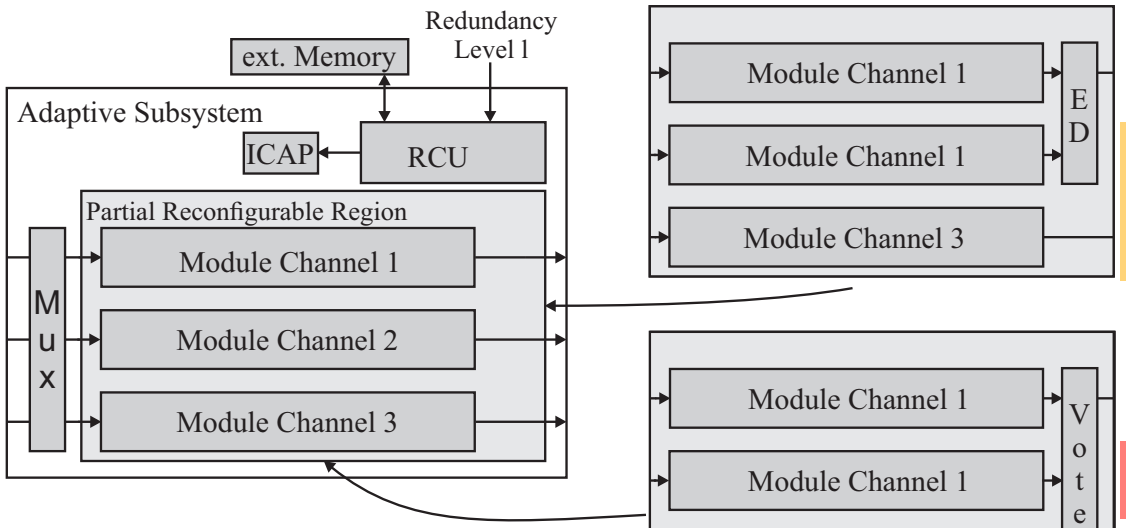
$$R_m^{TMR,s}(t) = e^{-\lambda_m^{TMR,s} \cdot t}$$

$$PFH_m^{TMR,s} = 1 - R_m^{TMR,s}(T_h) \text{ with } T_h = 3600s$$



λ	: Failure rate
μ	: Upset rate
n	: Number of bits
R	: Reliability
PFH	: Probability of Failures per Hour
$\{\}_m$	: Module
$\{\}_{CFG}$	: Configuration
$\{\}_e$	: Essential
$\{\}^{TMR}$	: Triple Modular Redundancy
$\{\}^s$	: Scrubbing (cyclical rewrite of CFG)

Self-Adaptive SEU Mitigation: Case Study II



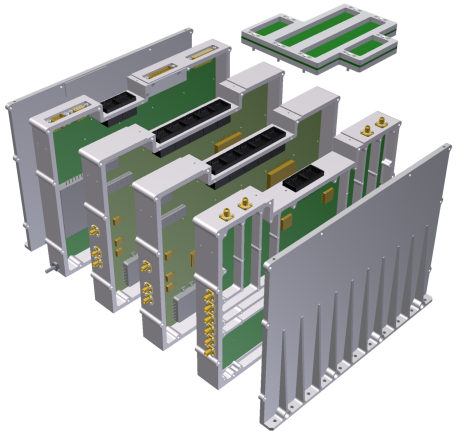
Improved by 99.999 %

> 90 % of the time no TMR overhead

Improved by 99.995 %

	Module	LUTs	FFs	DSP48	n_e	PFH$_m$ *Solar Min.*	PFH$_m$ *Solar Max.*	PFH$_m$ *Worst Week*	PFH$_m$ *Worst Day*	PFH$_m$ *Peak 5 Min.*
0	demod1	4,176	3,735	69	691,354	1.47×10^{-6}	2.54×10^{-7}	9.71×10^{-5}	2.77×10^{-4}	1.00×10^{-3}
	demod2	4,176	3,735	69	673,732	1.44×10^{-6}	2.48×10^{-7}	9.50×10^{-5}	2.70×10^{-4}	9.75×10^{-4}
1	demod3	4,176	3,735	69	757,174	1.61×10^{-6}	2.78×10^{-7}	1.06×10^{-4}	3.04×10^{-4}	1.10×10^{-3}
	demod1 (DMR)	8,352	7,470	138	1,382,708	1.47×10^{-6}	2.54×10^{-7}	9.71×10^{-5}	2.77×10^{-4}	1.00×10^{-3}
2	demod1 (TMR)	12,528	11,205	207	2,074,062	1.07×10^{-13}	3.23×10^{-15}	4.72×10^{-10}	3.85×10^{-9}	5.01×10^{-8}

Outlook



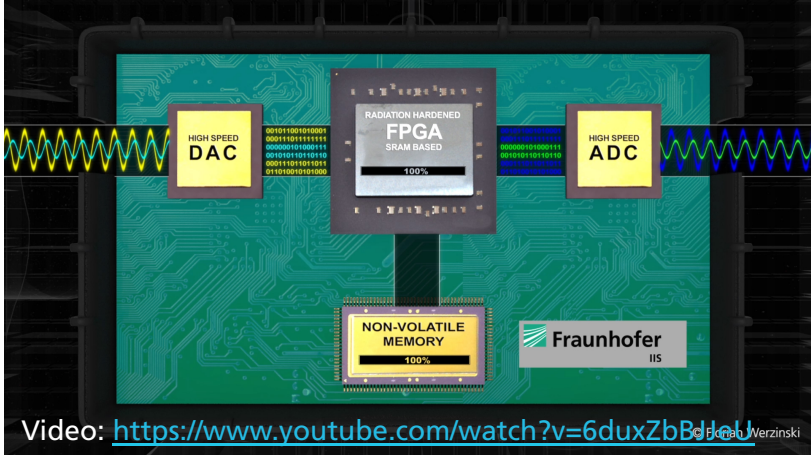
- FPGA Reliability Analysis
  - SEU mapping of all other used resources (primitives) in the FW design
- BRAM particle sensor
  - Optimize the estimation model and measurement of the MTTU
  - Take all SEUs of the FPGA into account → FPGA particle sensor
    - FFs and DSP with NMR, CFG memory (scrubber), …
  - SDRAM: low error rate (3D capacitor → Q_{crit} ↑ and junction collection ↓)
- Self-Adaptive SEU Mitigation
  - Generalization to enable a large set of apps → scalable mitigation (NMR, ABFT, scrubbing time, …)
- Firmware Framework: FMU integration in a LEON3 FT with RTEMS[1]

[1)] Real-Time Executive for Multiprocessor Systems

Conclusion I

- Problem: SEE in FPGAs and the resulting mitigation resource overhead
- Solution: Self-adaptive SEU mitigation system for FPGAs
  - Dynamic partial reconfiguration for optimal redundancy at runtime
- **BRAM radiation particle sensor** inside the FPGA
  - Integrated at point of interests, sensitive and scalable
  - The sensor BRAMs can be accessed by the user
    - Low overhead (realize FMU as FSM)
    - Just the ECC bits are analyzed
  - Can be integrated in almost every scalable mitigation

Conclusion II



Video: https://www.youtube.com/watch?v=6duxZbBJdeU

- Results
  - **Triplicate** the data **throughput at no flare** condition (*Solar Maximum and Solar Minimum*) compared to TMR → **no redundancy "over 90 %" of the time**
  - **Decrease the PFH** (probability of failures per hour) **by 2x10^4 at flare-enhanced** conditions (*Worst Week*, *Worst Day* and *Peak 5 Minutes*) compared with a non-redundant system
- Latest publications:
  - [1] FCCM'14: A Self-Adaptive SEU Mitigation System for FPGAs with an Internal Block RAM Radiation Particle Sensor
  - [2] AHS'14: Broadband FPGA Payload Processing in a Harsh Radiation Environment (upset rate typo in Chapter VI)
  - [3] Xcell 84: Ensuring FPGA Reconfiguration in Space