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Static Design-Dependent SEE rates on SRAM-based FPGAs: a designer flow

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3. University of Sevilla Team (FT-UNSHADES/2)
4. INAF Team (Milano) (FLIPPER)
5. Airbus Space and Defense (Janus design)
6. ESA colleagues

Outline

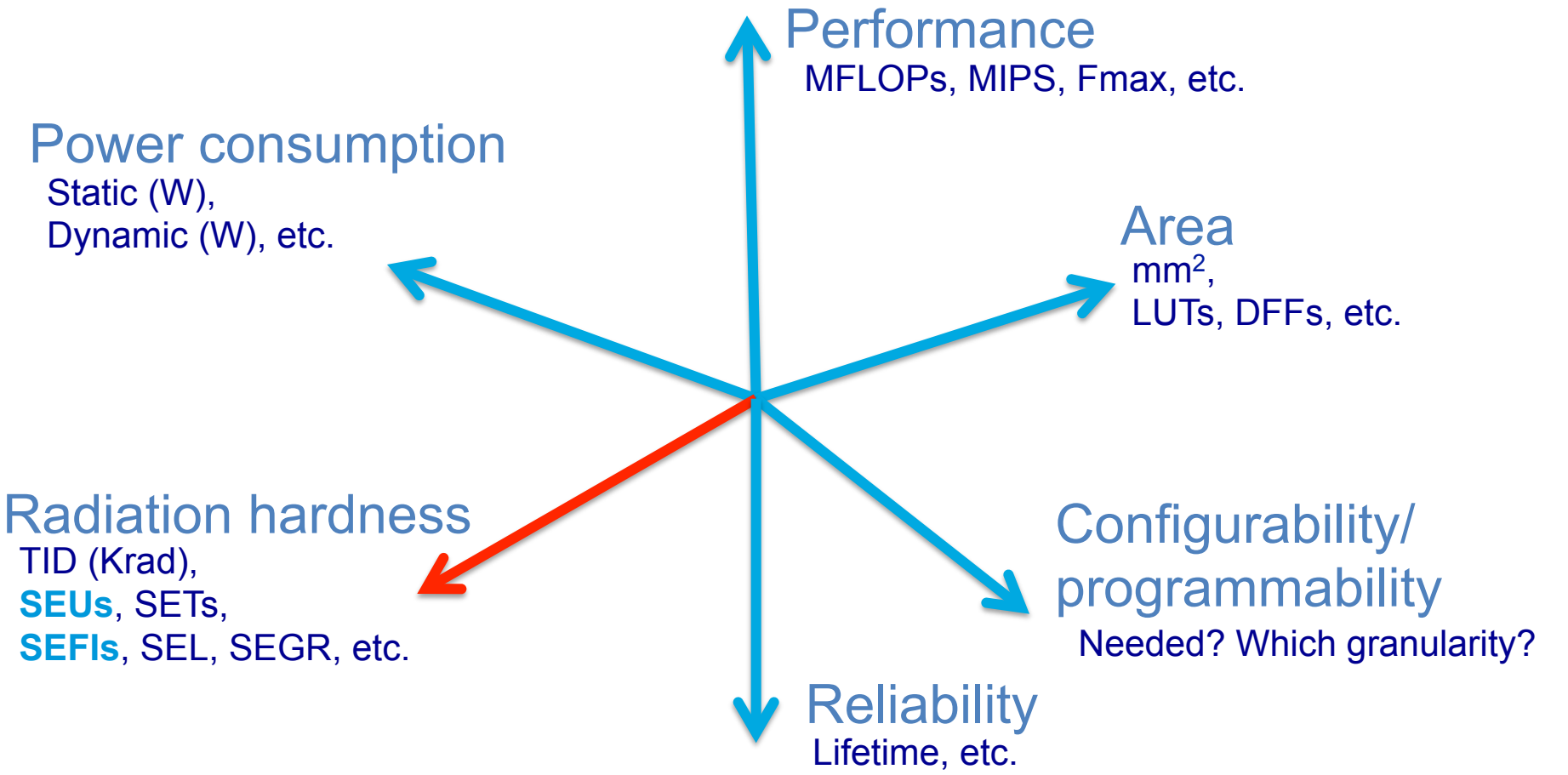
1. Motivation
    a. UKube example
2. Designer Flow overview
    a. Device specific
    b. Application specific
3. Results and Future work

Motivation

1. FPGA SEE rate prediction, information to be considered:
    a. Space Environment
        - Orbit information, CREME96
    b. FPGA components:
        - Accelerated radiation testing. Provides radiation cross sections of the FPGA architectural elements
    c. Mitigation techniques
        - FPGA designer can implement several mitigation techniques that will change the final SEE rate

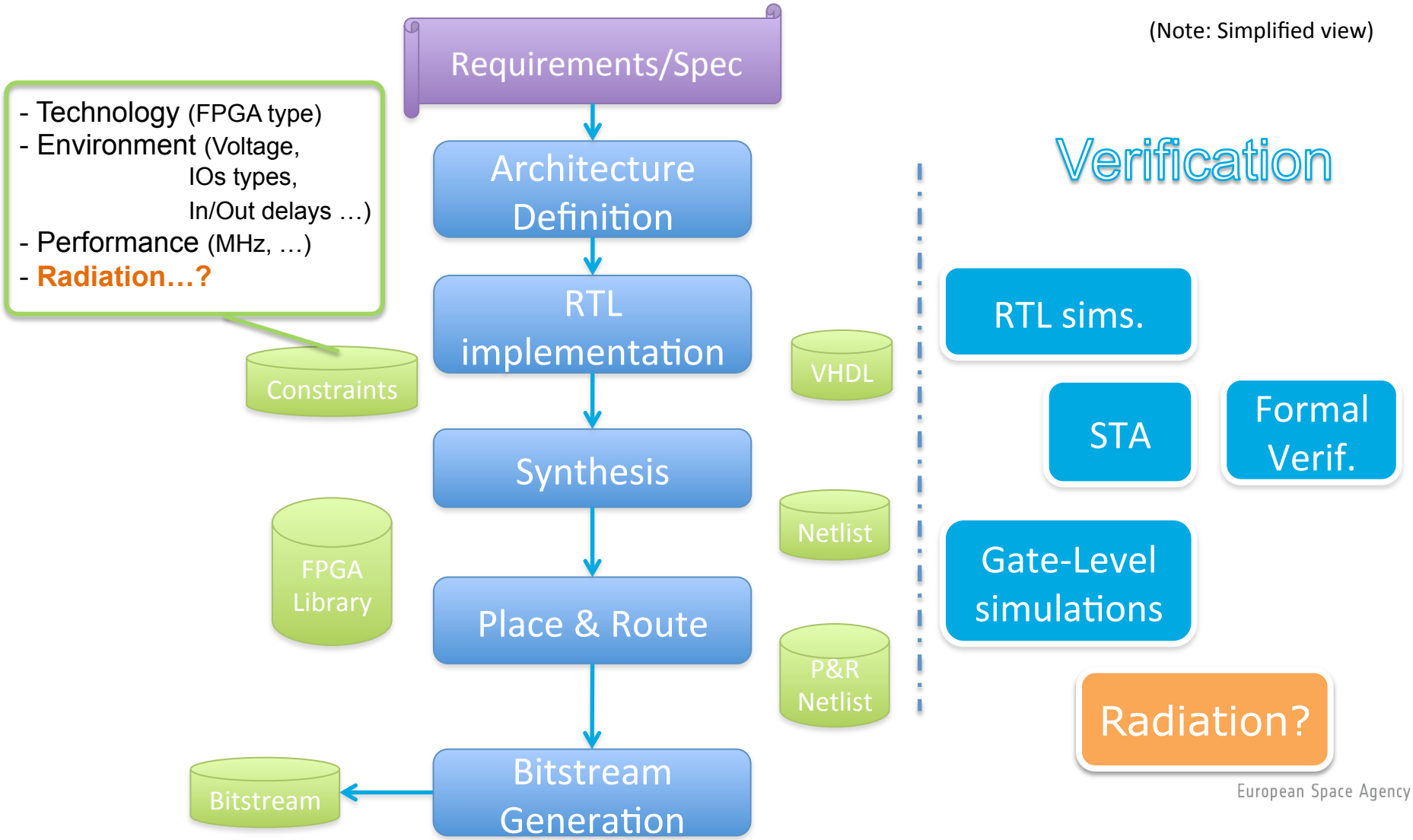
Can the FPGA designer predict the SEE rate of the Application (Place & Routed) in the FPGA?

Motivation, FPGA designer trade-offs: radiation hardness is included



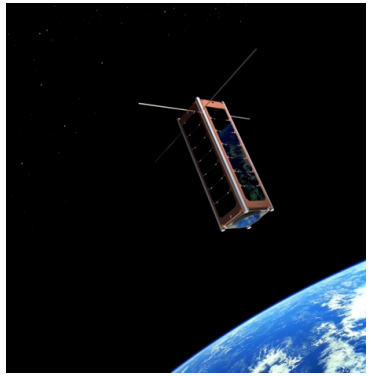
Also VERY important: Quality, Packaging, Mounting, ITAR, Price …

Motivation: How does Radiation fit in the FPGA Designer Flow?



Design Example used in the presentation: Janus UKube payload

1. UKube is a Nanosatelite
    a. Janus payload
    b. The FPGA has a design without mitigation (the goal is to get events, not to mitigate them)
2. FPGA: Virtex 4 XQR4VSX55 [9]
    a. UMC 90nm copper
    b. CF1140 ceramic flip-chip
    c. 55296 Logic Cells
    d. 5760 Kb BRAM
    e. 8 DCMs



Janus Design resources:

	Number	%
Slices Flip-Flops	41,000	83
4-input LUTs	120	83
IOs	320	18
RAMB16s	320	100
GCLKs	18	56
DCM	8	100

[9] Xilinx, Space-Grade Virtex-4QV Family Overview, DS653 (v2.0) April 12, 2010.

XQR4VSX55 architectural elements

1. Architectural Elements, as described in [4]:

Acronym	Description	XQR4VSX55
CFG	Configuration Bits	15,713,449
BRAM	Block Memory Bits	5,898,240
FFs	User Flip Flops	55,296

2. SEFIs considered for XQR4VSX55 ([4]):

Acronym	SEFI Description
POR	*Power-on-Reset.* This is a SEFI that results in global reset of all internal storage cells
SMAP	*SelectMap Interface*. Loss of read/ write capabilities through SelectMAP port. It is observed by acquiring meaningless data or inability to refresh data.
GSIG	*Global Signal*. This includes Global Set/Reset, Global Write enable and Global drive high signals

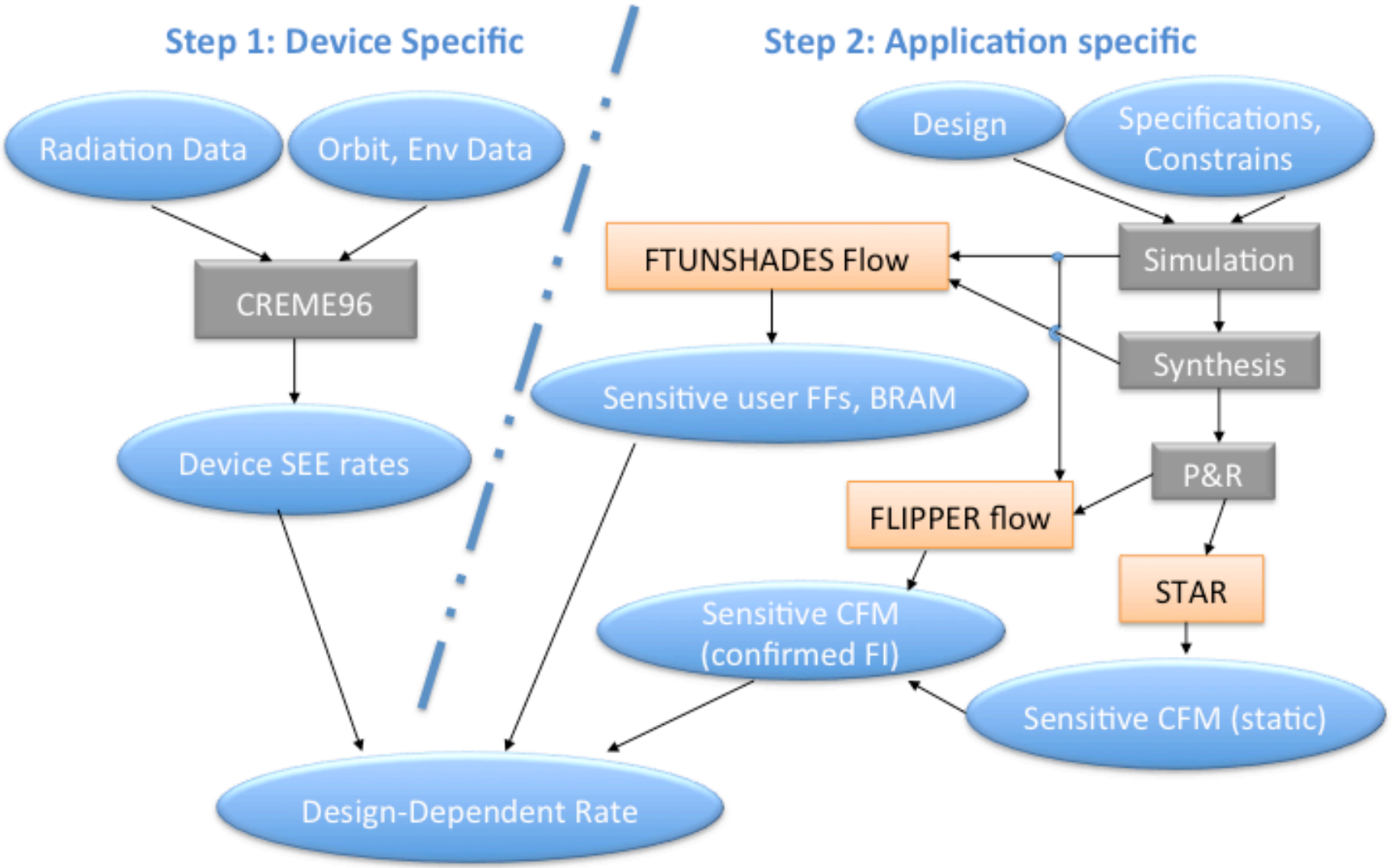
[4] Gregory Allen, Gary Swift, Carl Carmichael, "VIRTEX-4QV static SEU characterization summary" Jet Propulsion Laboratory California Institute of Technology Pasadena, California.

Overview of the flow (1/2)

1. Design-dependent static SEE rate of an application implemented in an FPGA, 2 steps:
    a. **Step 1**: **Device Specific**
        - Computes the SEE rate for each FPGA architectural blocks according to the specific mission conditions (i.e. Orbit). Based on publication [5].
    b. **Step 2**: **Application Specific** (Design Specific)
        - During the Design Phase, detailed information from P&R of the design in the FPGA. Compute the SEE specific for the application … *<at least a first approximation>*

[5] Joshua D. Engel,Michael J. Wirthlin ,Keith S. Morgan,Paul S. Graham "Predicting On-Orbit Static Single Event Upset Rates in Xilinx Virtex FPGAs" 2006 Military and Aerospace Programmable Logic Devices Conference 26-28 September 2006 Washington, D.C.

Overview of the flow (2/2)

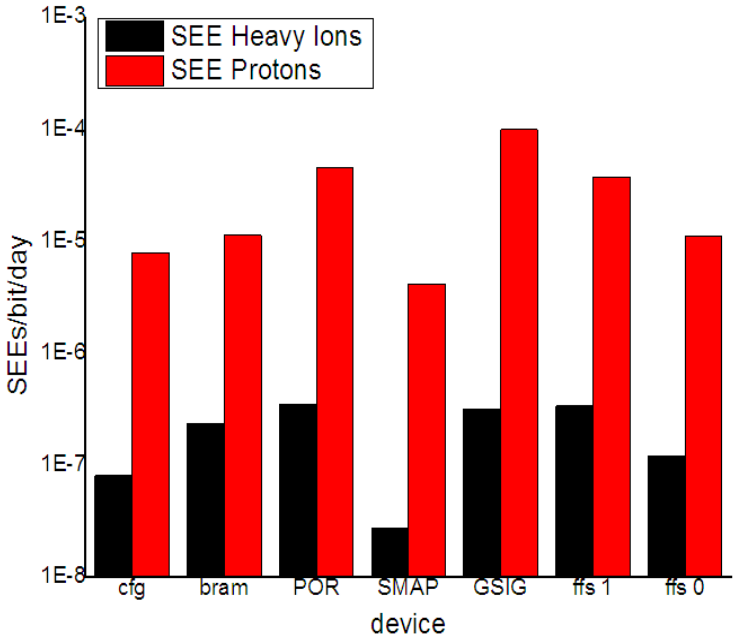


STEP 1: Device Specific

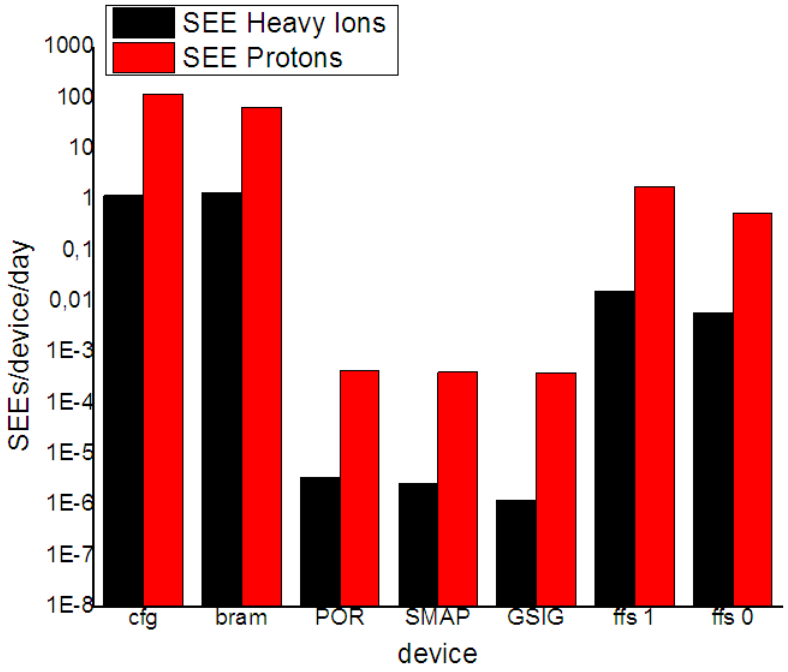
1. Static SEE rates for the FPGA architectural elements, methodology as published in [5], based on **CREME96**:
    a. Mission-dependent information (orbital and environmental information).
        – UKube case : Perigee 600km, apogee 600km and inclination 97.79 deg.
    b. Accelerator measurements [4] (using cross-section information in the form of **Weibull** distribution fitting)
2. Three cases have been studied:
    a. solar minimum, flare enhanced worse day and solar maximum

Device Specific Results, architectural elements contribution

1. Results for Solar Minimum (other cases available in the report):



SEEs/**bit**/day



SEEs/**device**/day

Configuration memory (CFG) is the biggest contributor when considering all CFG bits

Device Specific Results, "worst case", including all bits

1. Addition of all the architectural elements contribution (equivalent for SEFIs):

$$SEU_{device/day} = \sum_{k} N_k \left(SEU_{bd,k,HI} + SEU_{bd,k,\mathrm{Proton}} \right)$$

k: FPGA architectural block
N_k: Number of bits of the arch. block *k*
$SEU_{bd,k}$: SEU bits/day of arch. block *k*

	SEUs device/ day	SEFIs device/ day
SOL MIN	1,94E+002	1,28E-003
WORSE DAY	4,56E+003	1,51E-002
SOL MAX	1,30E+002	8,61E-004

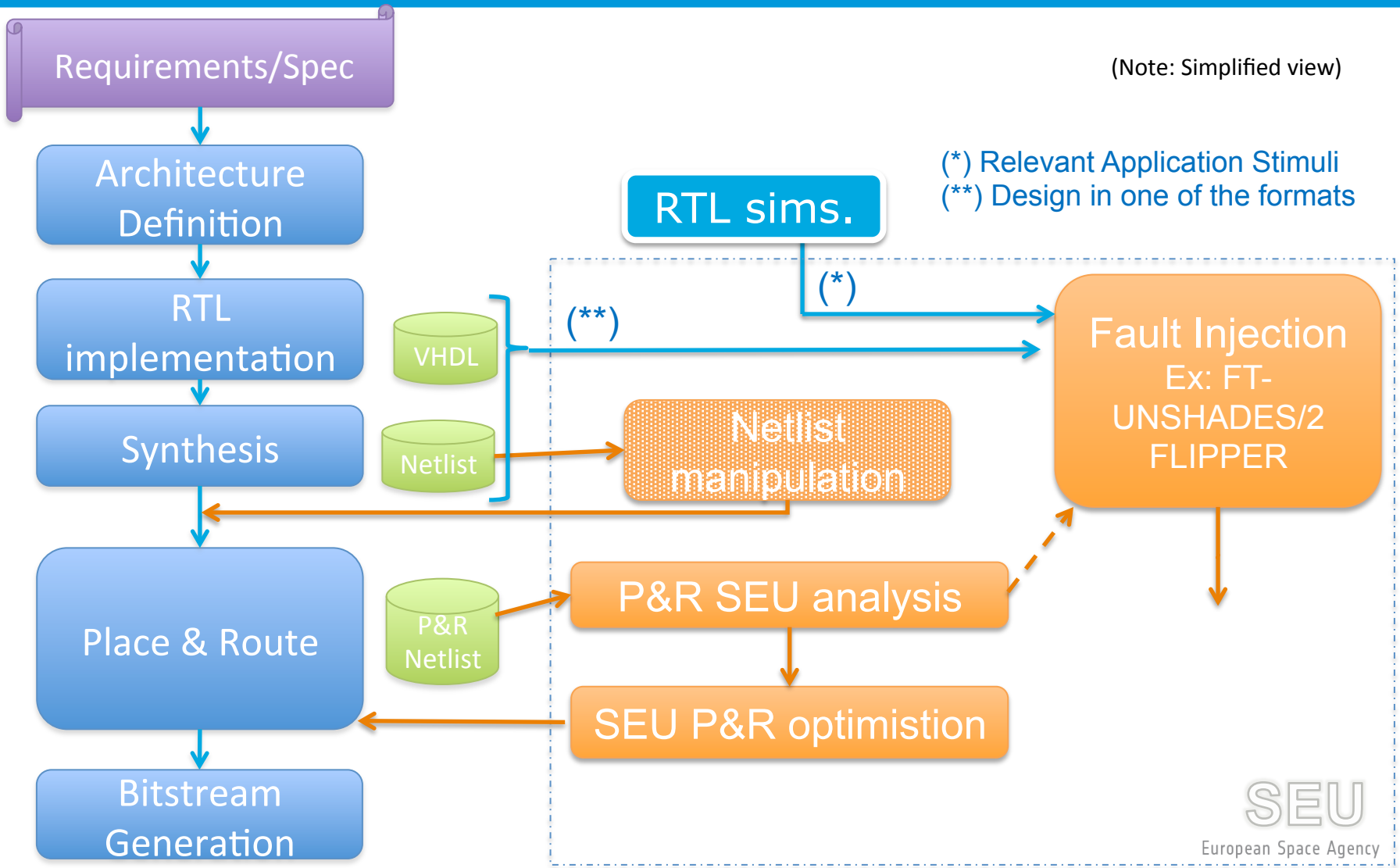
STEP 2: Application Specific

1. Application specific
    a. How many bits of each architectural feature are really relevant for a given application?

$$SEU_{device/day} = \sum_{k} N_k \left(SEU_{bd,k,HI} + SEU_{bd,k,\mathrm{Proton}} \right)$$

    b. What tools are available to get the N_k for the specific application?

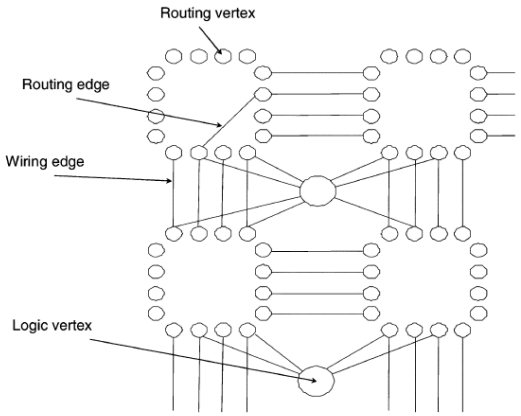
FPGA designer flow, tools to help implement and assess mitigation



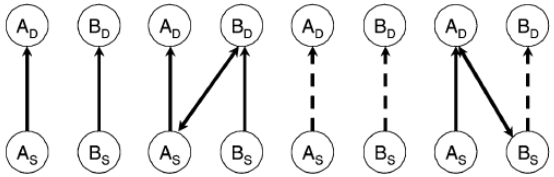
Configuration Memory: Static Analysis with STAR

1. No commercial tool available ! It is in the wish list …
2. But … the STAR tool from Politecnico di Torino [7]. Single event effects in Configuration Memory:

Goal: get the Configuration Static Critical bits (i.e. Sensitive Bits) of the application after the Place&Route



Equivalent routing graph



Effects of an SEU

The STAR tool validation is ongoing.
Needs extra correlation with more Radiation Results

[7] L. Sterpone and M. Violante, "A new analytical approach to estimate the effects of SEUs in TMR architectures implemented Through SRAM-Based FPGAs". IEEE Transactions On Nuclear Sciense, Vol. 52, No. 6, December 2005.

STAR Report

Report of Violations: Output is number of cfg memory sensitive bits

STAR Discovery Results

Total Sensitive Bits: **892060**

Bit Type
Programmed : 497104
Not Programmed : 394956

Resource Bits
LUT : 439552
MUX : 224688
CLB Config : 14122

ALONE PIP : 0
OPEN PIP : 57552
SHORT PIP : 5995
INTRASHORT PIP : 152
ANTENNA PIP : 149999

TOTAL PIP : 213698

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1 Intrashort : 152
1 Short : 5995
1 Antenna : 149999
1 Open : 57552

Total TMR Failure: 0

	Multiple Open	Short
TMR Failure	0	0
Warning One Domain	0	0
Warning Different Partition	0	0
TMR Warning Same Signal	0	0

TMR FAILURE Detailed Nets

	Multiple Open	Short
Ground (GND)	0	0
Power (VCC)	0	0
Clock (CLK)	0	0
Reset (RST)	0	0

Time to perform the analysis: 959 seconds

Reads Design after mapping
STAR reads .xdl netlist (ncd2xdl command)

```
inst "G3[6].wide_larger_shift/G1[10].larger_shift/G1[15].large_shift/q<1>" "SLICEL",placed
CLB_X13Y76 SLICE_X18Y153  ,
  cfg " BXINV::#OFF BYINV::#OFF CEINV::#OFF CLKINV::CLK COUTUSED::#OFF CY0F::#OFF
       CY0G::#OFF CYINIT::#OFF DXMUX::X DYMUX::Y F:G3[6].wide_larger_shift/
G1[10].larger_shift/G1[15].large_shift/Mxor_q_1_xor0000_Result1:#LUT:D=(A2@A1)
       F5USED::#OFF FFX:G3[6].wide_larger_shift/G1[10].larger_shift/G1[15].large_shift/q_1:#FF
       FFX_INIT_ATTR::INIT0 FFX_SR_ATTR::SRLOW FFY:G3[6].wide_larger_shift/
G1[10].larger_shift/G1[15].large_shift/q_0:#FF
       FFY_INIT_ATTR::INIT0 FFY_SR_ATTR::SRLOW FXMUX::#OFF FXUSED::#OFF
       G:G3[6].wide_larger_shift/G1[10].larger_shift/G1[15].large_shift/
Mxor_q_0_xor0000_Result1:#LUT:D=(A2@A4)
       GYMUX::#OFF REVUSED::#OFF SRINV::SR_B SYNC_ATTR::ASYNC XBUSED::#OFF
       XMUXUSED::#OFF XUSED::#OFF YBUSED::#OFF YMUXUSED::#OFF YUSED::#OFF
       "
  ;
```

"Assisted" Fault Injection

1. Fault Injection "campaign" requires (simplified; it would require a full presentation in itself):
    a. Goal and scope of the Fault Injection
    b. Inputs for the application (DUT). They must be representative !
    c. Define injection locations and time
    d. Continuous or debug modes
    e. Inject in the Design FFs/BRAMs or in the Configuration Memory (or both)
2. In our case:
    a. Inject in all the design FFs. As a simple design, injecting at any time will produce an error at the output
    b. Inject in the Configuration Memory to Confirm STAR results: PENDING (we did not have the right part at the F.I. system).

Fault Injection, FPGA Configuration Memory

1. Fault Injection for Configuration
    a. The goal is to Inject on the Configuration Bits reported by STAR as critical and confirm which ones will change the nominal outputs if flipped.
    b. Fault Injection System used: **FLIPPER**

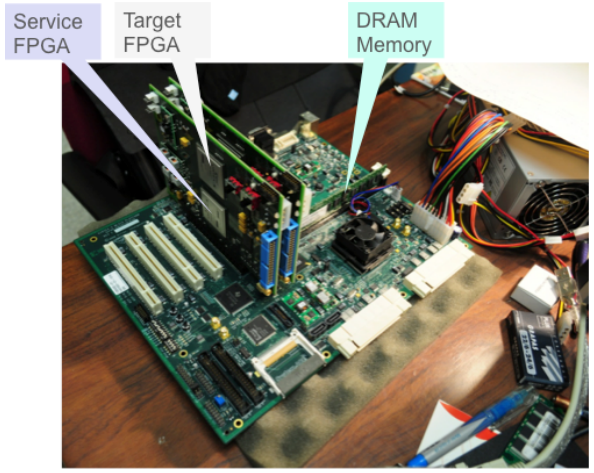
Status:

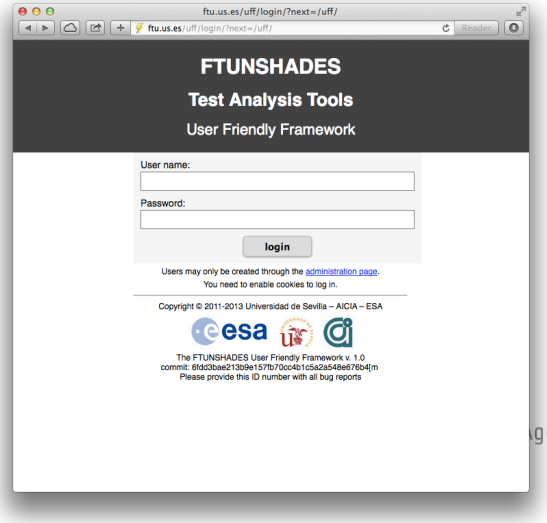
Migration to **XQR4VSX55**: in the final stage.

UKube Janus design: soon to be checked.

Fault Injection, Application FFs (and BRAMs)

1. Fault Injection for the Application Design:
    a. Target FFs: Injection to all design FFs
    b. DUT inputs: all test cases. (This is a simple case; in a general design it would be more complex)
    c. Injection time: 1 injection per *RUN*, random (in this case simple because each injection is observable at the output within the *RUN*)
    d. Results: ALL FFs are critical (as expected)
2. Fault Injection System used: FT-UNSHADES2 (FT-U2)
    a. Access to FT-U2 in Sevilla: http://ftu.us.es/uff





Results (1/2)

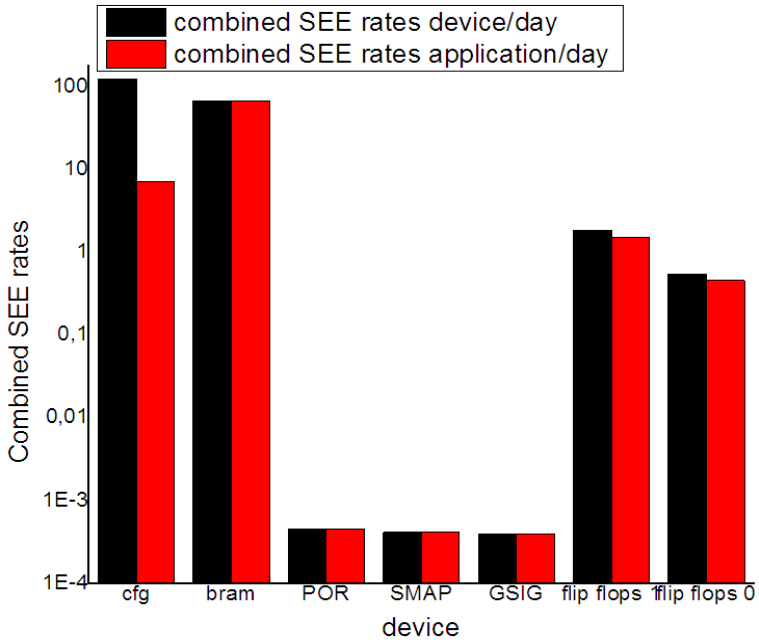
1. UKube Janus Final Application critical bits:

	Application Critical Bits	XQR4VSX55
CFG	892,060	15,713,449
BRAM	5,898,240	5,898,240
FFs0	41,000	55,296
FFs1	41,000	55,296

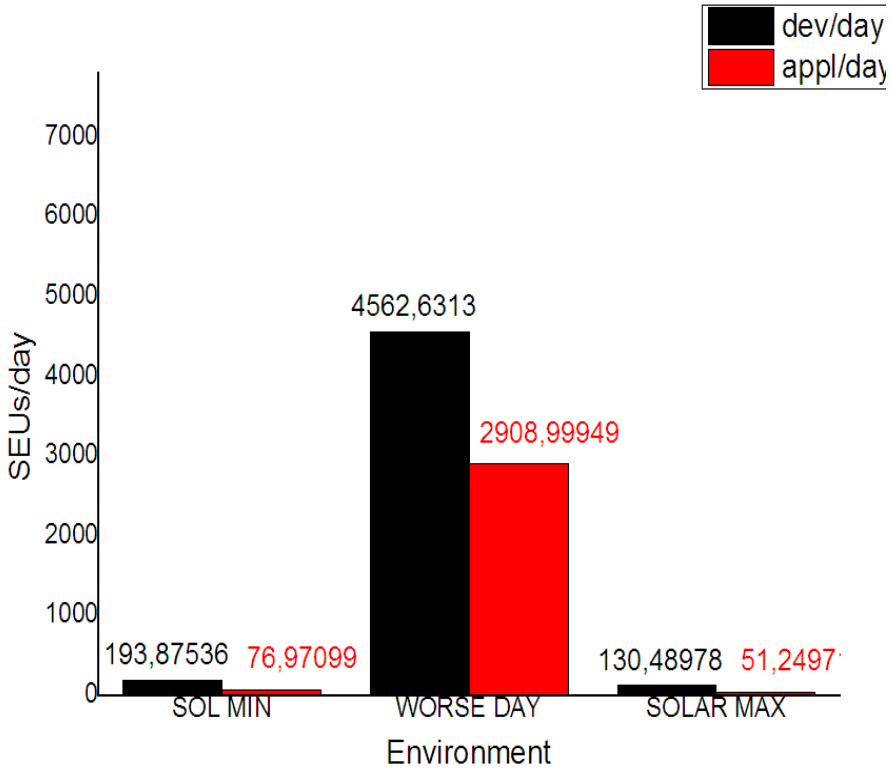
2. Consideration of this case:
    a. In this case no mitigation has been applied
    b. A design with (selective) mitigation, would have a different number of critical bits for the Application would be lower

Results (2/2)

1. UKube Janus SEE rate prediction (compared with the device SEE rate):



Combined SEEs/**device**/day for Solar Minimum



Combined SEUs/**device**/day and SEU/**appl**/day

Conclusion (1/2)

1. Need of tools to help FPGA designers to predict application-specific SEE rates
2. An approach based on 2 steps has been presented:
    a. Device specific (requires radiation acceleration test results and mission environment information, CREME96)
    b. Application specific
3. Static analysis (STAR) and Fault Injection (FT-U2 and FLIPPER) have been proposed as tools to assist in the SEE prediction

NOTE: there are other tools that will assist the FPGA designer; the list is not exhaustive

Conclusion (2/2)

1. Future work
    a. To use other applications with mixed mitigated strategies for Flip-Flops and BRAMs in order to have trade-off cases
    b. STAR (VeriPLACE): finish correlation of data with radiation experiments to prove the models
    c. Fault Injection: investigate more in detail how to implement efficient and representative experiments
    d. Extension to dynamic SEE prediction

2. Request

    a. STAR (VeriPLACE) "validation": needs more users in order to validate it. Can you contribute?
    b. Designs: do you have designs that we could use? (or would you like to use FT-U2 and VeriPLACE?)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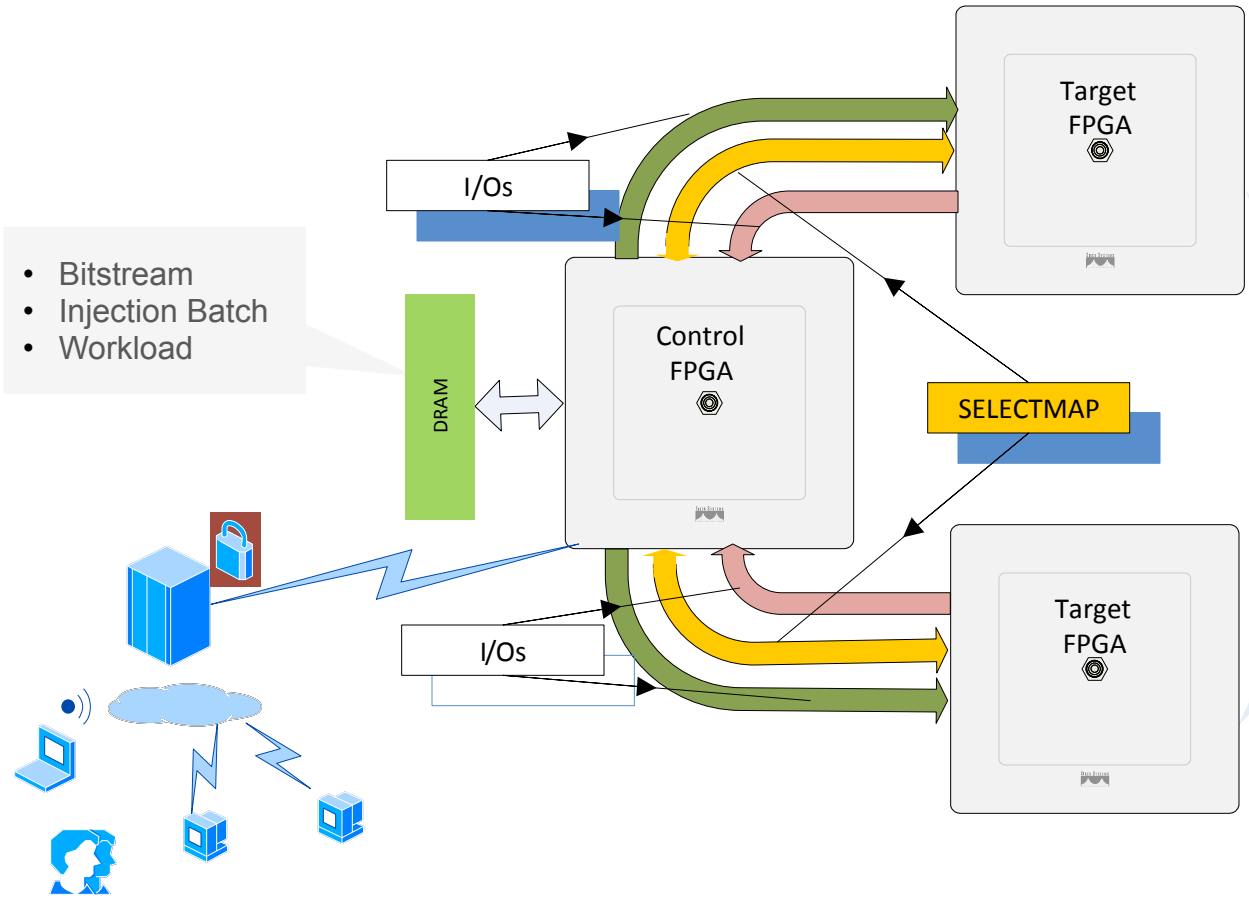
FT-UNSAHDES summary slide



- Bitstream
- Injection Batch
- Workload

Two twin FPGAs hosts two copies of the netlist. The design runs along in parallel

FPGA selection

1. FPGA selection includes several aspects (not exhaustive list):
    a. **Capacity and performance** (**frequency** and **power consumption**)
        - Related to the internal architecture and technology node used
        - Related to **Mass** and **Volume**, as it enables miniaturization
    b. **Radiation hardness**
        - Addressed at different levels:
            - Process
            - Transistor/ Standard Cell
            - Register Transfer (RTL)
            - System
    c. **Reconfigurability**
    d. **Quality, Packaging, Assembly**
    e. Others:
        - **ITAR** (International Traffic in Arms Regulations)
        - **Cost**