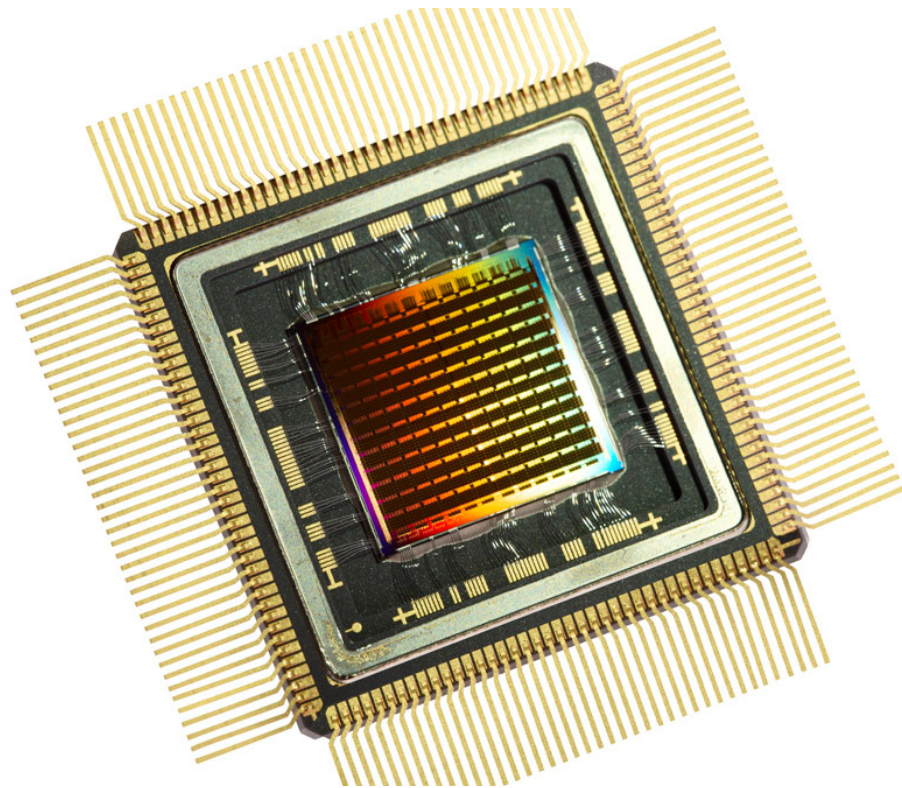




## AT40K FPGAs Platform For SPACE APPLICATIONS

SEFUW  
ESTEC, Noordwijk  
2014, Sept. 16-18<sup>th</sup>



# AT40K FPGA PLATFORM

## Alternatives with the AT40K SRAM-based FPGA series for low gate count designs requiring low-power applications

- Technology from 0.35 to 0.15µm
- **Build-in RH** product  
Radiation hardening proven – No need for radiation testing
- Unlimited **reprogramming** product
- Embedded memory blocks (freeRAM™)
- Configurations auto-checks with
  - Check of configuration download protocol
  - Check of SRAM content vs EEPROM content
  - Check of SRAM integrity in run time
- Highest level of Space qualification: ESCC and QML-V
- No ITAR restrictions apply
- ATMEL EEPROM's for FPGA configuration

*built-in SEU protection*

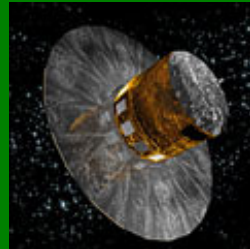
*Re-programmability*

*Configuration auto-check*

# FLIGHT HERITAGE & PLANNING TO FLY ...



Megha-tropiques  
Oct 2011



Gaia  
Dec 2013



Sentinel-1  
Apr 2014



Pharao  
In ISS in 2016



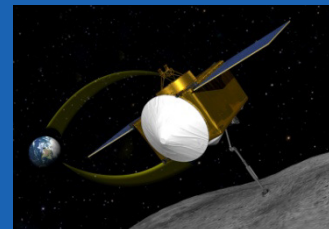
CFOSat (swim)  
2015



Ingenio/SEOSat  
2015



Svom  
2015



Osiris-Rex  
2016

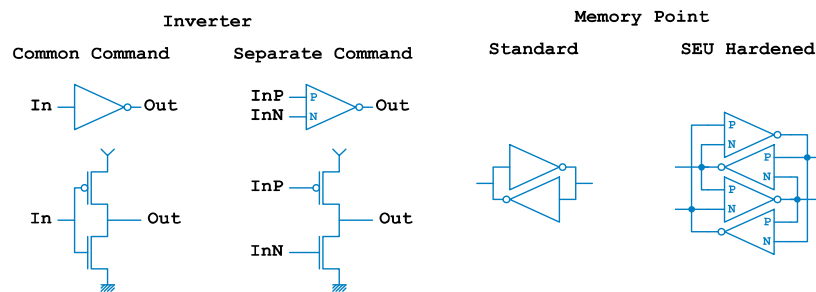


Bepi-Colombo  
2016

# ATMEL FPGA – Built-In SEU Fault-Tolerance

SEU Protection		ATMEL SRAM-Based RH FPGA
FPGA Internal Logic	Control State-Machine	<b>Built-In TMR</b>
	Configuration Memory	<b>Built-In DICE*</b>
User Design Area	D Flip-Flop	<b>Built-In DICE*</b>
	SRAM/DPRAM	<b>Built-In DICE*</b>

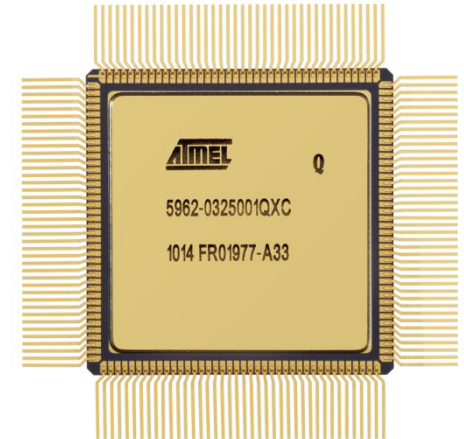
\* **DICE** (Dual Interlocked storage **CELL**),



The SEU hardened memory point can only change value if the 2 channels switch at the same time → An ion impact on a single channel cannot flip the memory point

# AT40KEL040

- **Technology**
  - 0.35µm
- **Product features**
  - 46K equivalent ASIC gates // 2 kLuts (4)
  - 20 MHz clock speed
  - 18 Kbit FreeRAM (144 modules of 32x4)
  - 3.3V Core and I/Os
  - Packages CQFP 160 & 256



## Qualification status

DLA qualified with SMD 5962-03250

ESCC qualified with ESCC DS 9304/008

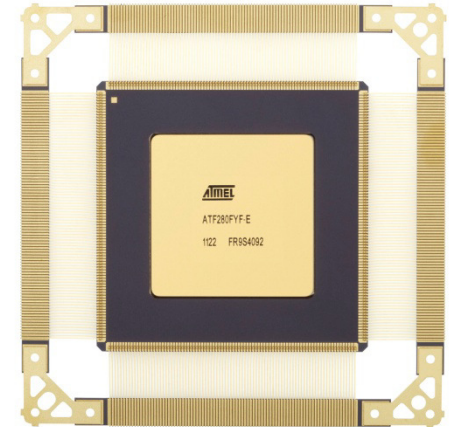


## Radiation Performances

TID Tested up to 300Krad  
SEL >70 MeV/mg/cm<sup>2</sup>

# ATF280

- **Technology**
  - 0.18 $\mu$ m
- **Product features**
  - 280K equivalent ASIC gates // 14 kLuts
  - 50 MHz clock speed
  - 115 Kbit FreeRAM (900 modules of 32x4)
  - I/O's cold sparing PCI compliant
  - 8 RX and 8TX LVDS
  - 1.8V Core and 3.3V I/Os
  - Packages CC/CLGA472 & CQFP 352 & 256



## Radiation Performances

TID Tested up to 300Krad  
SEL >70 MeV/mg/cm<sup>2</sup>

## Qualification status

DLA qualified with SMD 5962-12225  
ESCC qualified with ESCC DS 9304/xxx



# ATFS450

- **Technology**

- 0.15µm **SOI**

- **Product features**

- 450K gates equivalent ASIC gates // 21 kLuts
- 70 MHz clock speed
- 180 Kbit FreeRAM (900 modules of 32x4)
- I/O's cold sparing PCI compliant
- 8 RX and 8TX LVDS
- 1.5V Core and 3.3V I/Os
- Packages CQFP 352

A blue oval graphic tilted diagonally, containing the text "SOI Technology" in white.

## Availability

Engineering samples	now
Flight Models	15H2

## Radiation Performances Target

TID: 100Krad +  
SEE: high performances with SOI

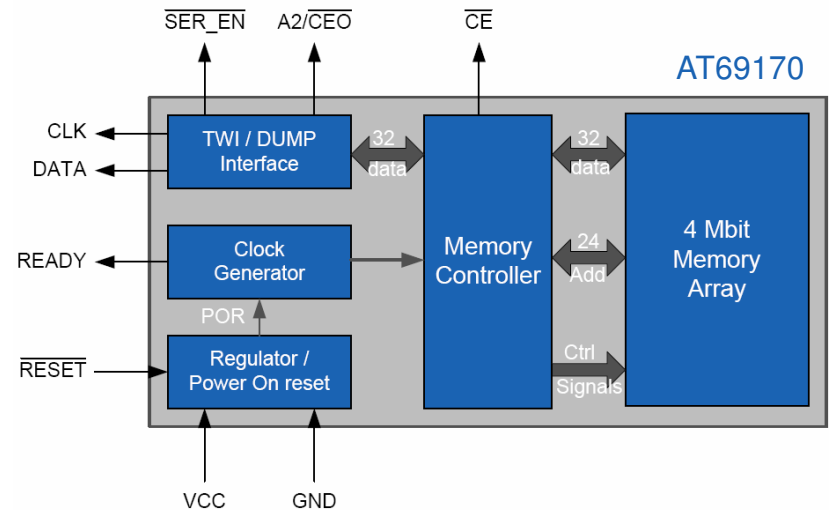
# Companion EEPROM: AT17LV010 & AT69170

## AT17LV010

- **Technology** 0.35µm
- **Product features**
  - 1 Mbit Rad Hard EEPROM
  - 3.3V Core and 3.3V I/Os
  - Packages CFP28

## AT69170

- **Technology** 0.18µm
- **Product features**
  - 4 Mbit Rad Hard EEPROM
  - 1.8V Core and 3.3V I/Os
  - Standard TWI programming interface
  - Endurance: 10K cycles
  - Data retention: >15 years at 125° C
  - TID: 60 krads(Si) in Read mode
  - Packages CFP18



### Availability

Engineering samples	now
Flight Models	now



# ATFee560

- **Technology**

- 2 ATF280 and 2 EEprom AT69170

- **Product features**

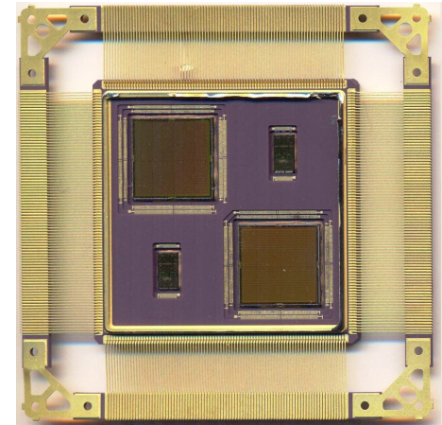
FPGA

- 2\* 280K gates equivalent ASIC gates
- 2\* 115 Kbit FreeRAM (900 modules of 32x4)
- 2\* (2 RX & 2TX) LVDS

EEPROM

- 2\* 4Mbit Rad Hard EEPROM

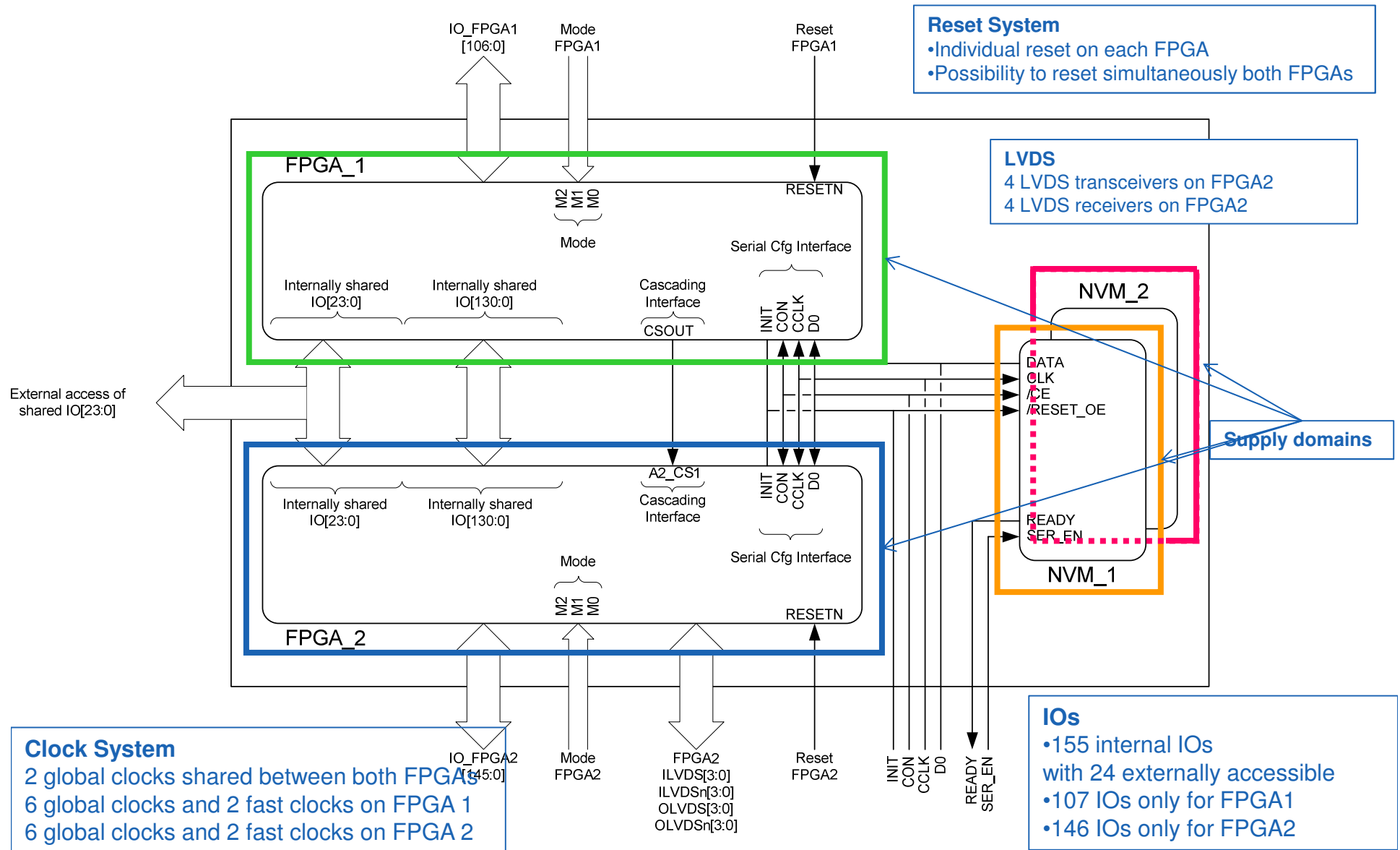
Package CQFP352



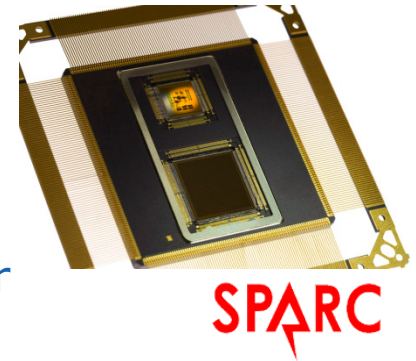
## Availability

Engineering samples	now
Flight Models	15Q1

# ATFee560 Block diagram



# ATF697



- **Technology**

- 1 ATF280 FPGA and 1 ATF697 Leon2-FT 100 MHz Processor

- **Product features**

## FPGA

- 280K gates equivalent ASIC gates
- 152\*152 core-cells (each 2 LUT + 1 DFF)
- 115 Kbit FreeRAM (900 modules of 32x4)
- 4 RX & 4 TX LVDS

## PROCESSOR

- 100 MHz – 86 Mips
- Peripheral UART
- Embedded Instruction and Data caches Icache : 32Kbytes; dcache : 16 Kbytes
- EDAC protection for ext. memories (PROM, SRAM, SDRAM)
- SDRAM memory controller up to 93MHz

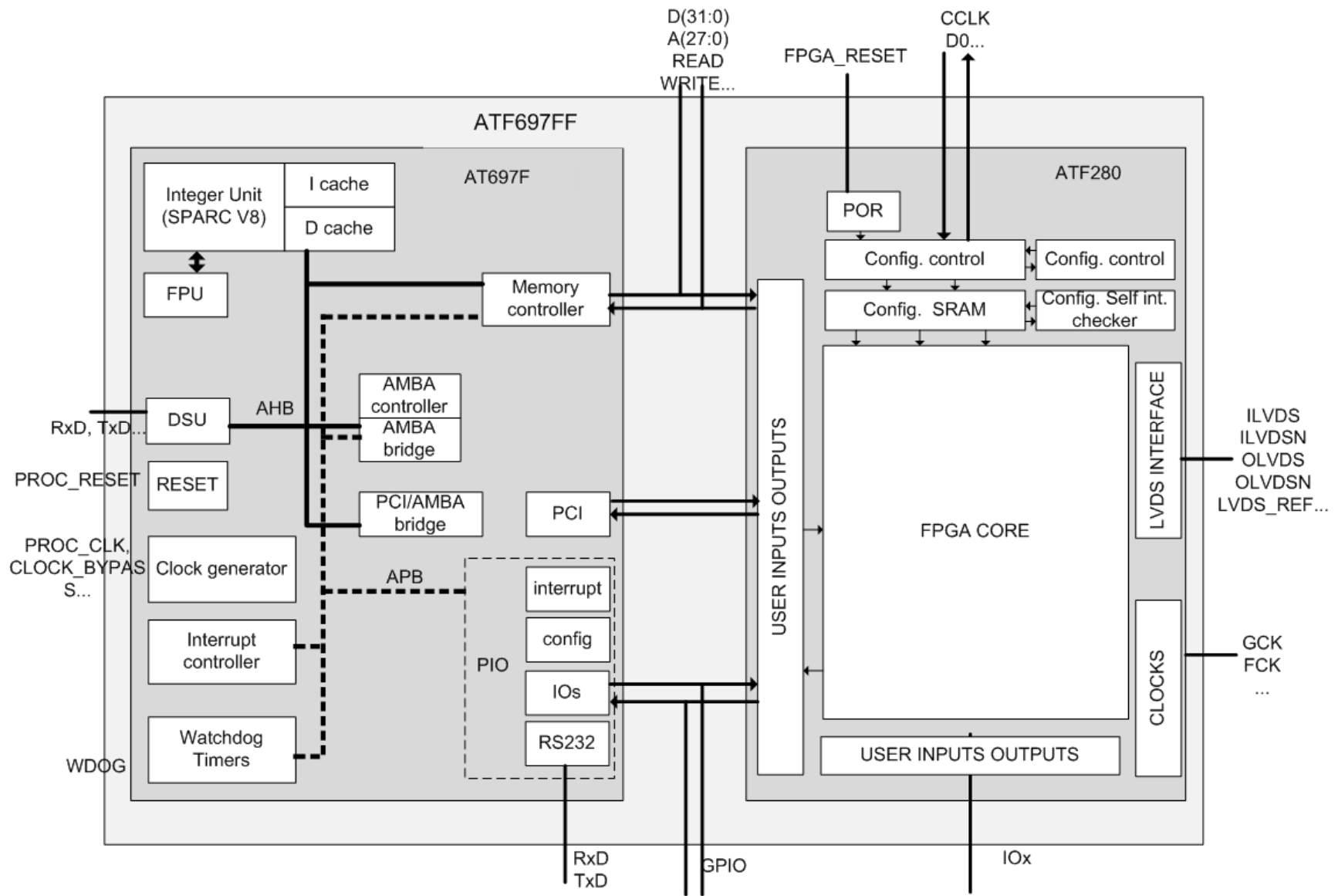
## Qualification status

DLA qualified with SMD 5962-14229  
ESCC qualification on going



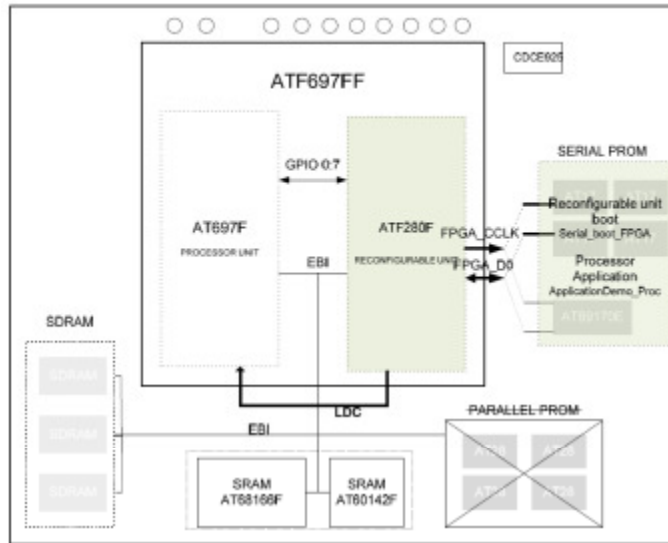
Atmel

# ATF697 Block Diagram



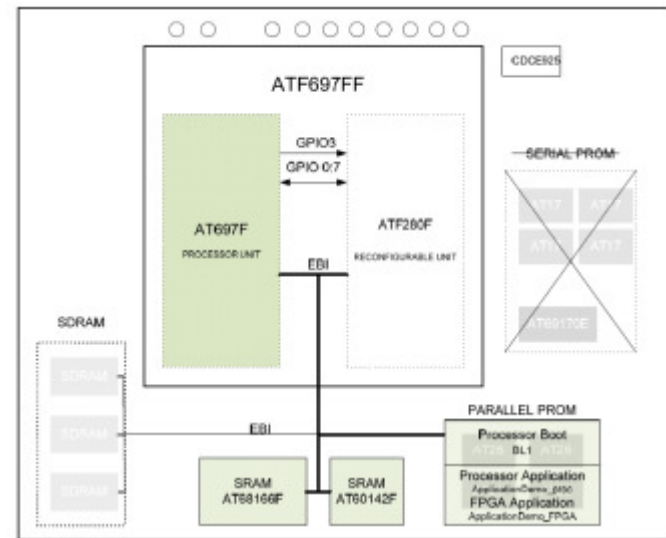
## ATF697 /ATF280 Modes

## FPGA in master mode



- All codes in FPGA NVM
- FPGA booting 1st
- FPGA controlling processor boot

## Processor in master mode

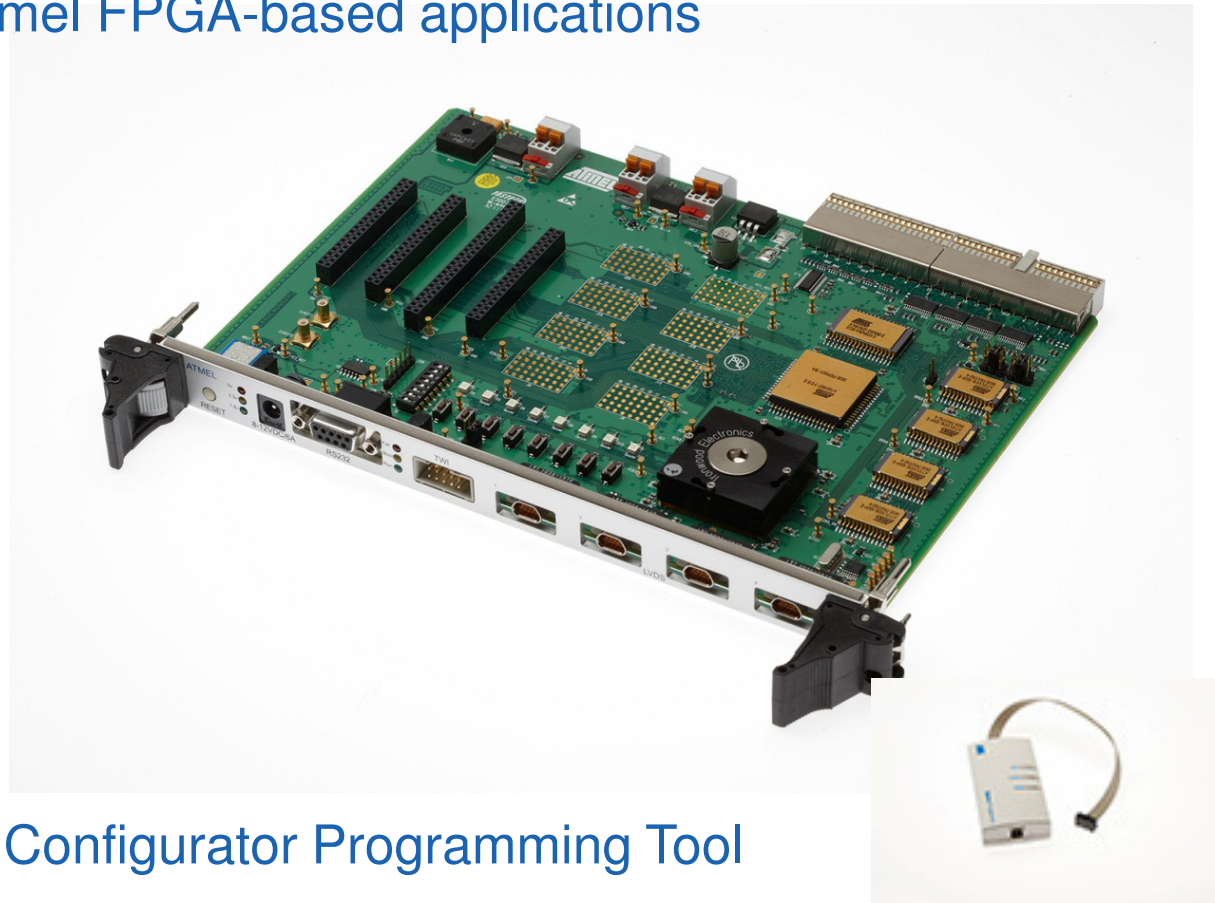


- All codes in Processor NVM
- Processor booting 1st
- Processor configuring FPGA
- On flight reprogrammable controlled by processor
- Interfaces update, bug fixes, routing dynamically

# HOW TO START WITH AT40K PLATFORM? HARDWARE

**Development kit is the main platform for**

- Evaluating the Atmel FPGA
- Developing Atmel FPGA-based applications



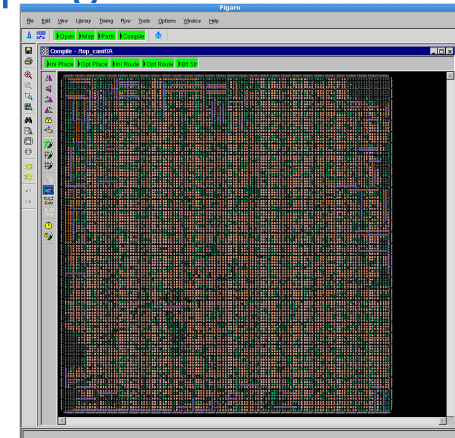
also includes the Configurator Programming Tool

# HOW TO START WITH AT40K PLATFORM? SOFTWARE

## SYNTHESIS

### MENTOR Precision

- Available from Atmel
- VHDL / Verilog entry
- Automatic IDS Macro detection and mapping

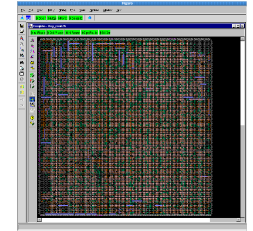


## PLACE & ROUTE

### ATMEL IDS: Automated Place & Route

- STA
- Power Estimator
- VHDL / Verilog netlist export with SDF back-annotation
- Bitstream generation

# IP's SOLUTIONS



Within IDS, the user get access to the placed&routed blocks

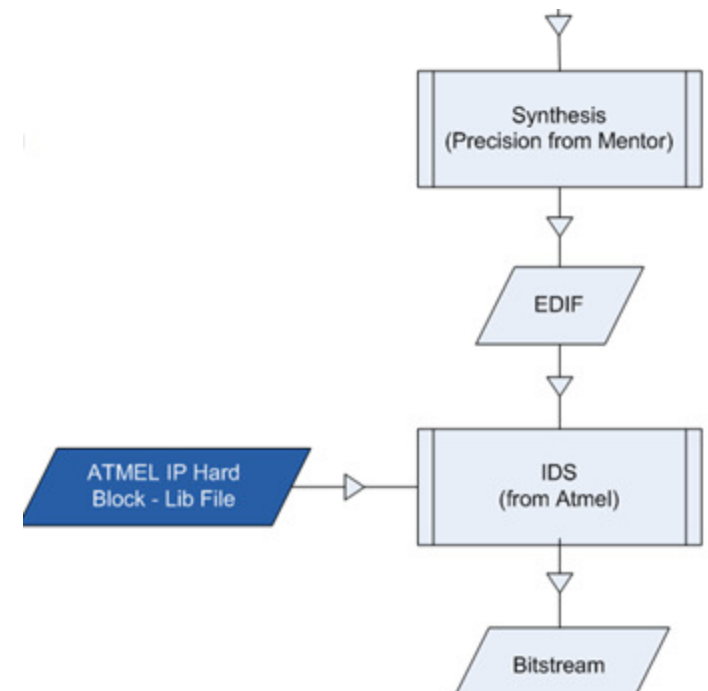
- Guaranteed performances
- Simulation files with high coverage level
- Validated on board

## Current Development (2013-2014)

- SpaceWire
- 1553
- PCI
- UART

## Next developments

- CAN
- SMCS TM/TC
- AVR8





# Contacts and Documentation

- Atmel website

[http://www.atmel.com/products/other/space\\_rad\\_hard\\_ics/default.aspx](http://www.atmel.com/products/other/space_rad_hard_ics/default.aspx)

- Datasheet
- User Guides
- Application Notes
- SMD

- Aerospace FAE manager

- [Thibaud.gaillard@atmel.com](mailto:Thibaud.gaillard@atmel.com)

- Hotlines

- SPARC Processors - [sparc-applab.hotline@nto.atmel.com](mailto:sparc-applab.hotline@nto.atmel.com)
- Communication ICs - [assp-applab.hotline@nto.atmel.com](mailto:assp-applab.hotline@nto.atmel.com)
- FPGA - [radhard-fpga@nto.atmel.com](mailto:radhard-fpga@nto.atmel.com)
- Other Products - [aerospace@nto.atmel.com](mailto:aerospace@nto.atmel.com)

- Radiation reports & Qualification data package upon request

- Secured web site AEDOS <https://www.atmel-nantes.fr/aedos/>

For FPGA's

- Access upon request to Marketing or hotline
- Place & Route tool (IDS) download
- Space Programmer documentation download
- Development kit documentation download

And also

Packages info: PPL, ibis models

...





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