SETs Broadening Tuning: a Place and Route Approach

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Goal

- Effective analysis of SET's impact on circuits mapped on Flash-based FPGAs
- Mitigation of SEEs sensitiveness
  - Optimal electrical filtering by placement
  - Selective guard gate

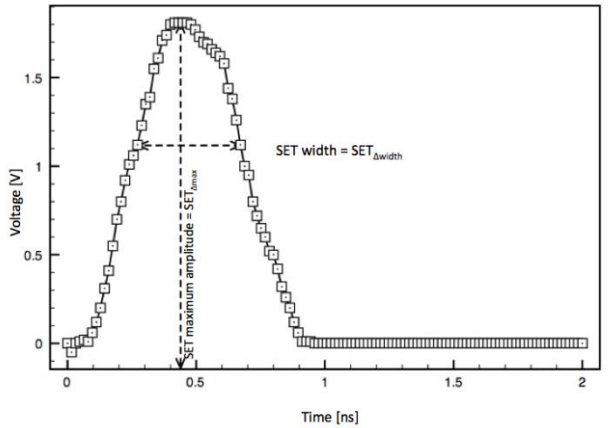
Outline

- Introduction
- Related Works
- Our Proposed Solution
  - Analysis of SET effects
  - Accurate mitigation of SEE
- Experimental Setup and Results
- Demo
- Future Works

Introduction (i)

- Generation of SET effects is due to the injunction of charge collection
  - A charged particle crosses a junction area
  - it generates an amount of current, provoking a "glitch"

SET width
SET amplitude
Rise ΔV/ΔT
Fall ΔV/ΔT

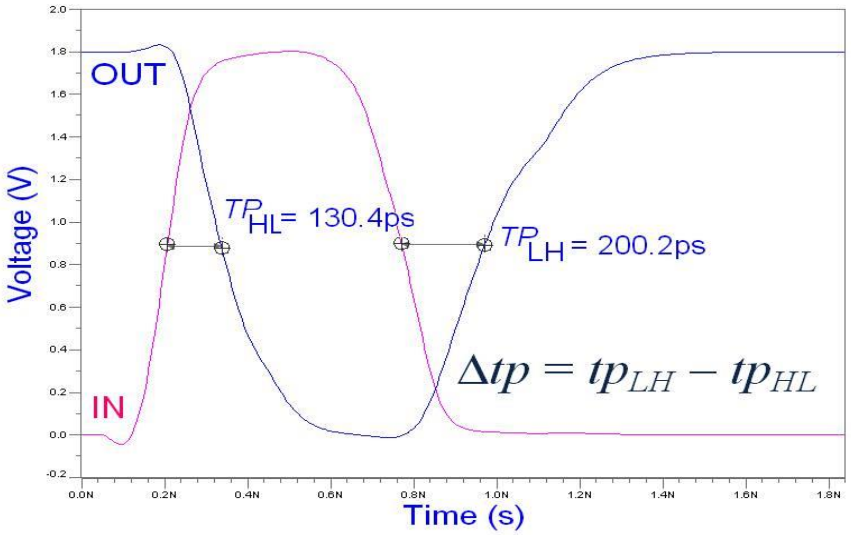


- SET can be indistinguishable from normal signal and exist for notable distances

Introduction (ii)

- Two transitions are possible: 0-1-0 or 1-0-1
- SET is generated into the sensitive area of a logic gate
  - It propagates until a sequential element is reached
  - During the propagation the SET may pass through different gates

Introduction (ii)



For a 1→0→1 transition Δtp is defined as:

$$\Delta tp = tpHL - tpLH$$

For a 0→1→0 transition Δtp is defined as:

$$\Delta tp = tpLH - tpHL$$

[Wirth et al, NSREC 2008]

Fist Region: If($\tau_n < k*tp$) then $\tau_{n+1} = 0$

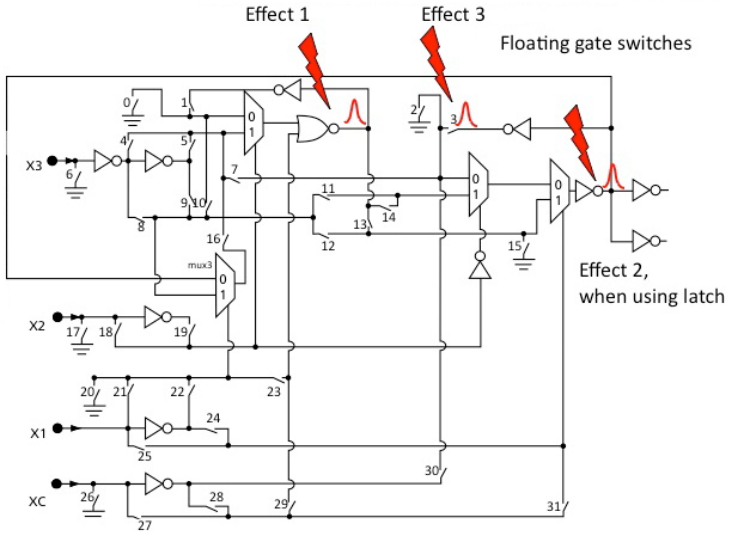
Second Region: If ($\tau_n > (k+3)*tp$) then $\tau_{n+1} = \tau_n + \Delta tp$

Third Region: If ($(k+1)*tp < \tau_n < (k+3)*tp$) then $\tau_{n+1} = (\tau_n^2 - tp^2)/\tau_n + \Delta tp$

Fourth Region: If ($k*tp < \tau_n < (k+1)*tp$) then $\tau_{n+1} = (k+1)*tp(1 - e^{(k-(\tau n / tp))}) + \Delta tp$

Introduction (iii)

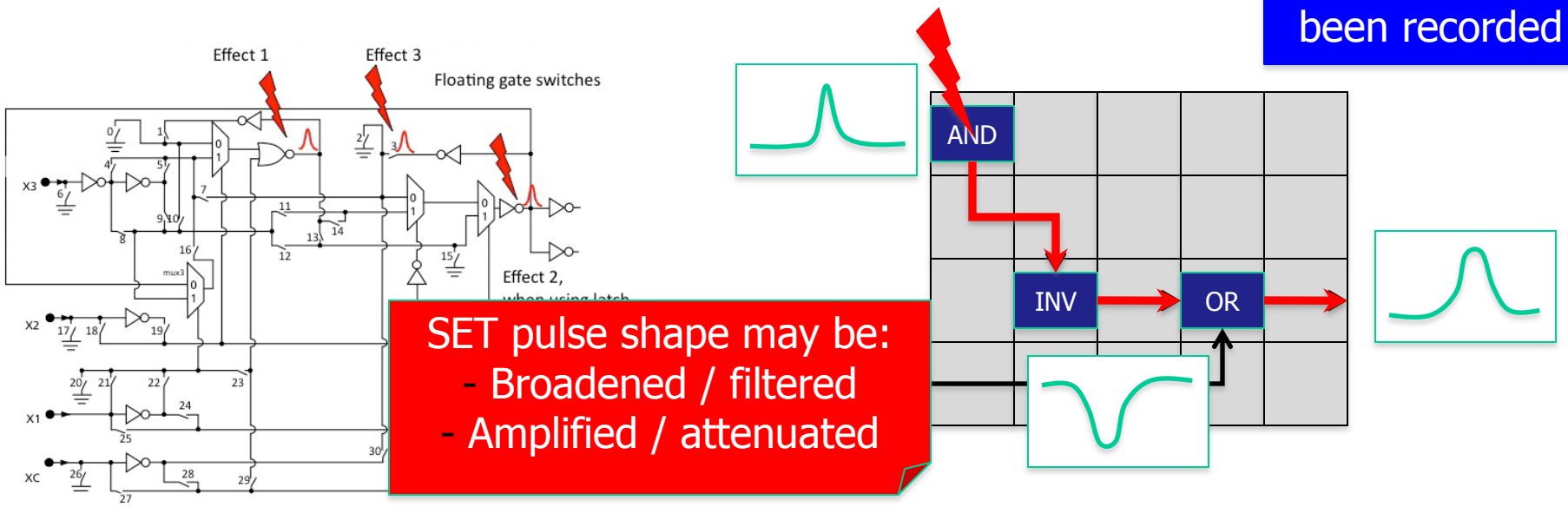
- A particle hitting the Flash-based FPGA basic block can provoke three effects:
  1. if hits a sensitive node, can induce a pulse that propagates through the logic
  2. It can affect a logic cell configured as a latch
  3. it can hit a junction in the floating gate switch



Introduction (iii)

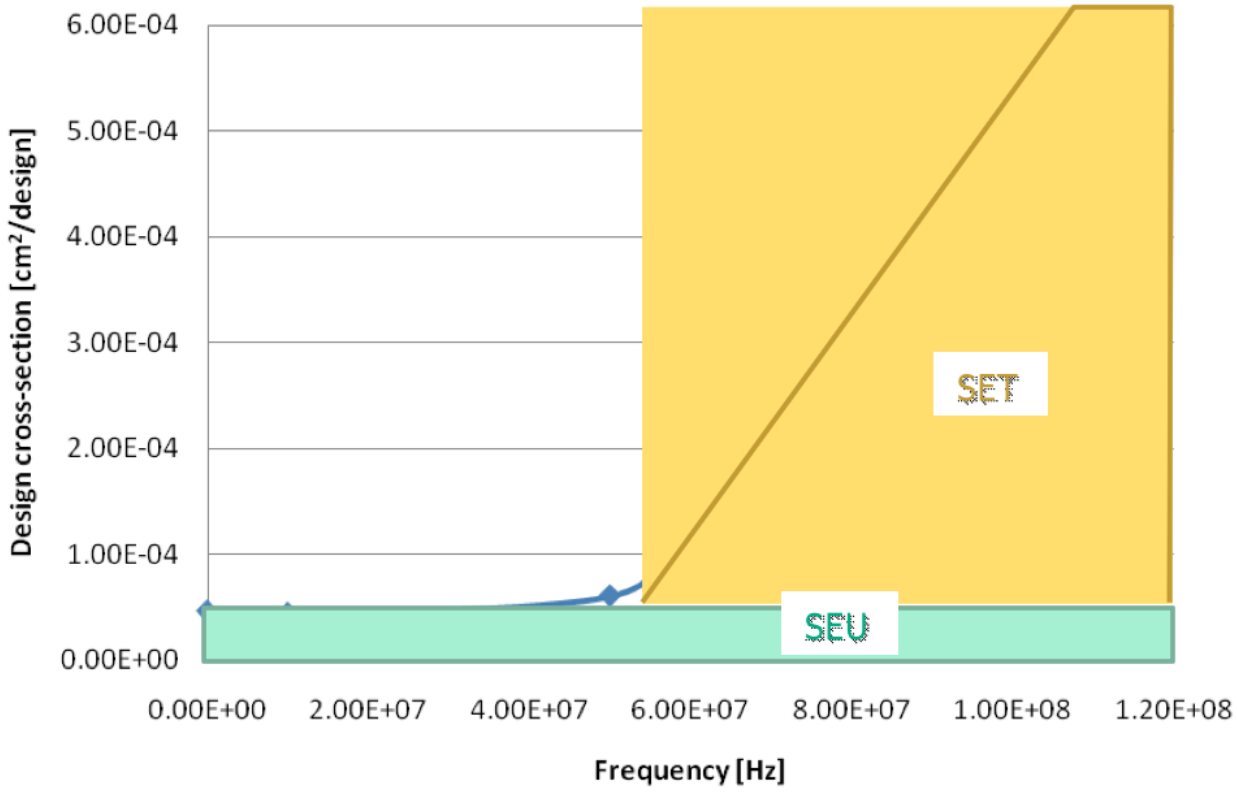
- A particle hitting the Flash-based FPGA basic block can provoke three effects:

1. if hits a sensitive node, can induce a pulse that propagates through the logic
2. It can affect a logic cell configured as a latch → SEU
3. it can hit a junction in the floating gate switch → No transient effects have been recorded



Introduction (iv)

- SETs phenomena is a growing concern



Radiation tests performed at the HIF, Louvain-La-Neuve, Belgium
Iodine beam LET 61.8 MeV cm^2 / mg

Related work (i)

- Flash-based FPGA configuration memory SEU immunity proven by several radiation tests
- ECC and TMR conventional solutions adopted for the user data memory (SRAM) and logic memory (FF)

Related work (ii)

- Flip-Flop implementation for SET filtering
  - Two latches block created by synthesis tools
  - Dual-sampling latch with internal sampling
  - Significant delay, area and power overhead
- Changing the configuration node by changing the configuration memory pattern [DATE'09]

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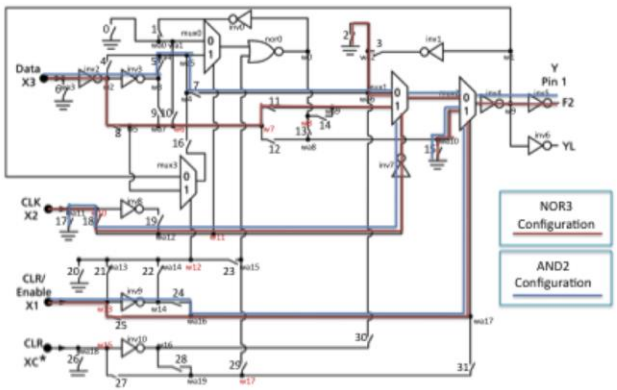
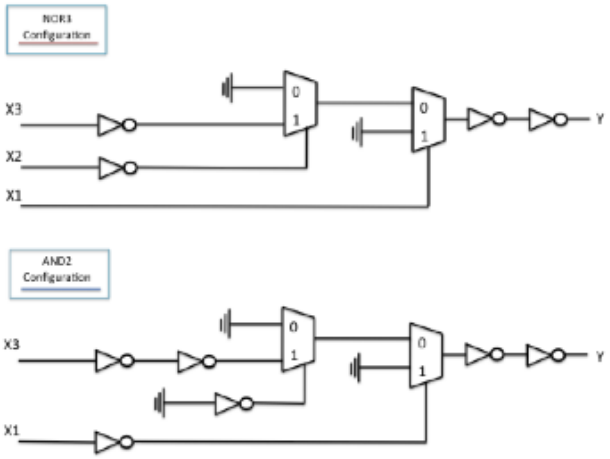




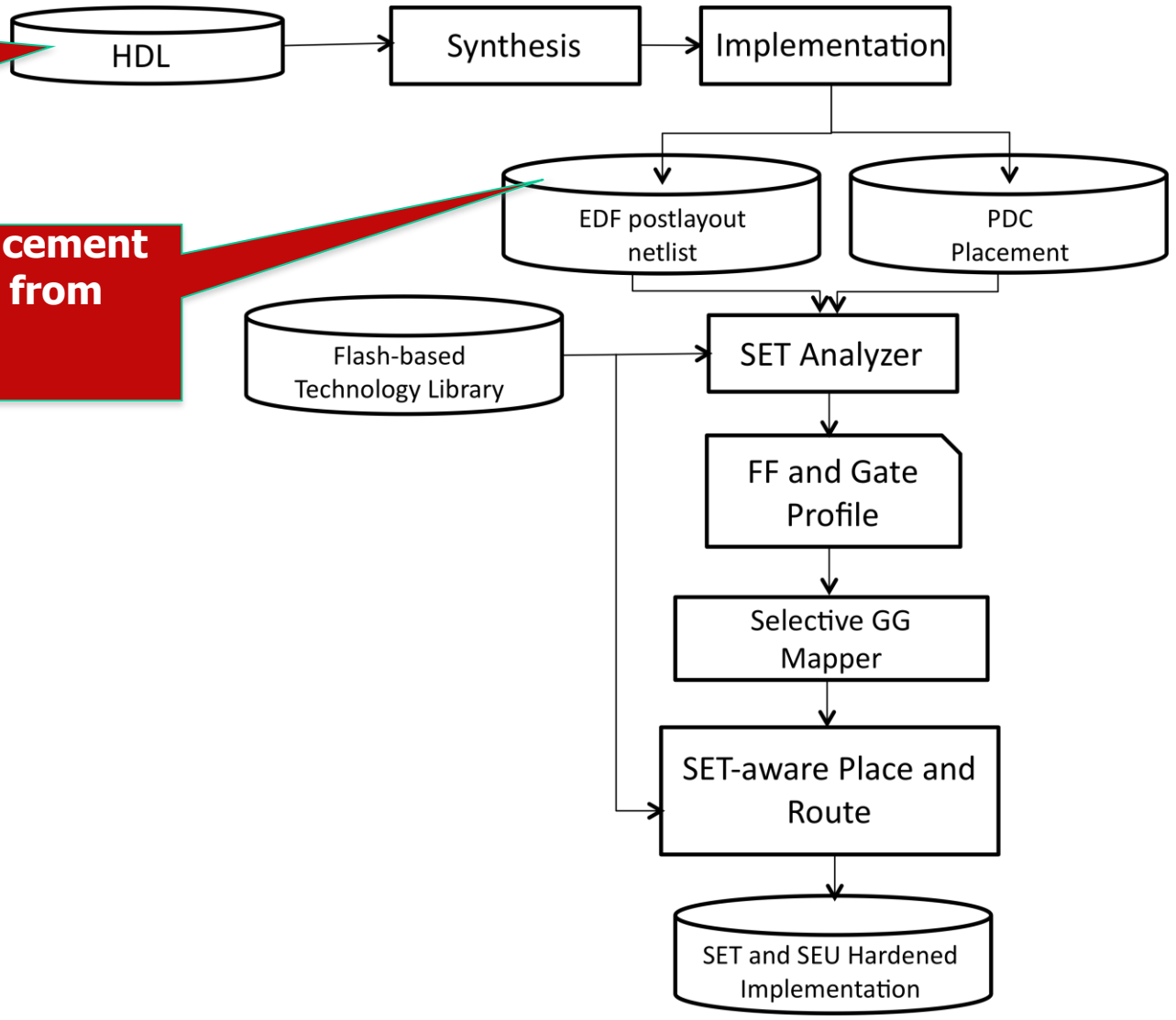
The proposed method (i)

- A set of back-end tools for the SEE analysis and SEE-aware implementation of circuits on Flash-based FPGAs
  - Based on a Place and Route solution
  - Does not require logic cell modification
  - Optimizes the reduction of SETs phenomena

The proposed method (i)

Native implemenation flow starting from the VHDL/Verilog

Postlayout netlist and placement locations are extracted from commercial tools



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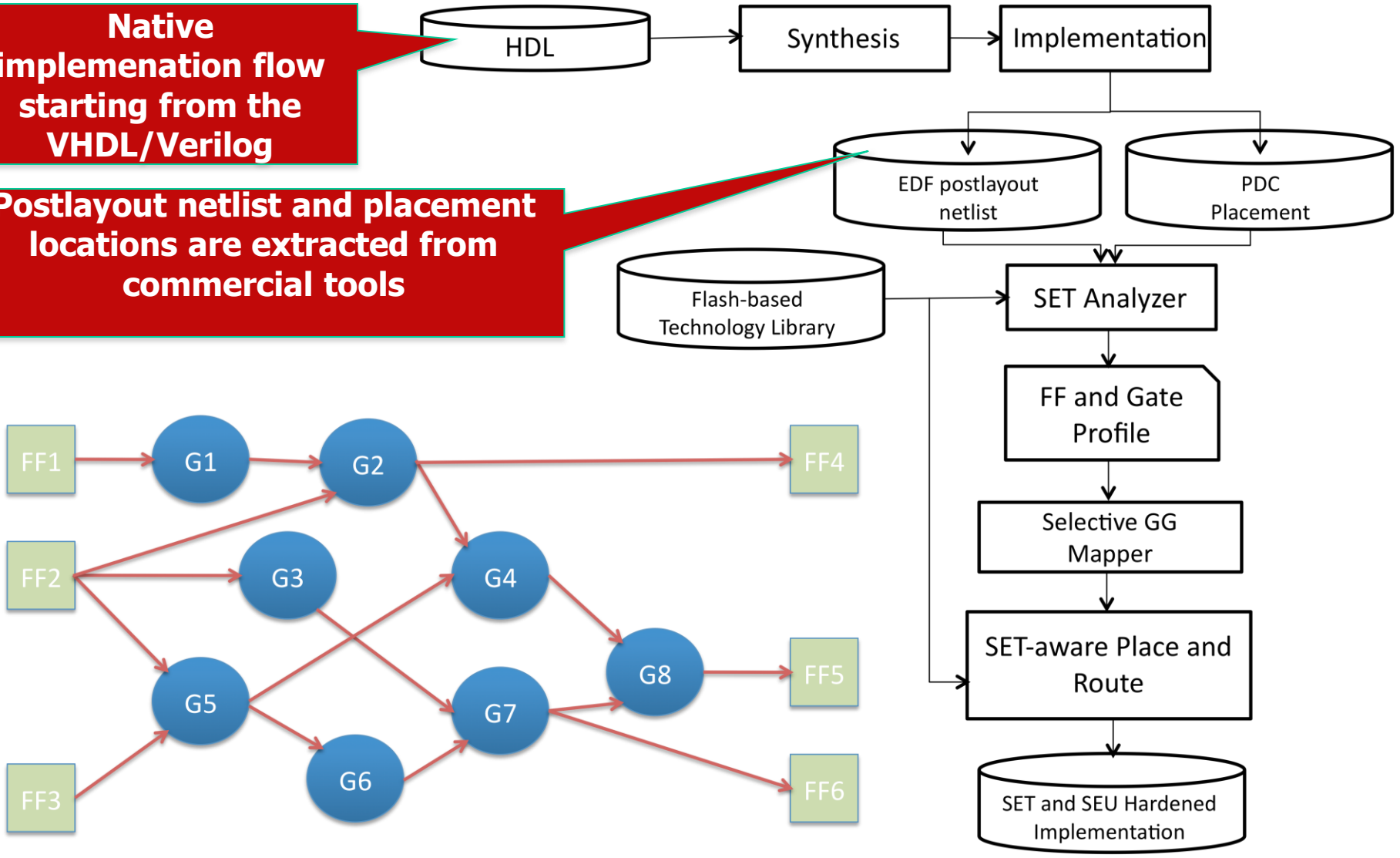
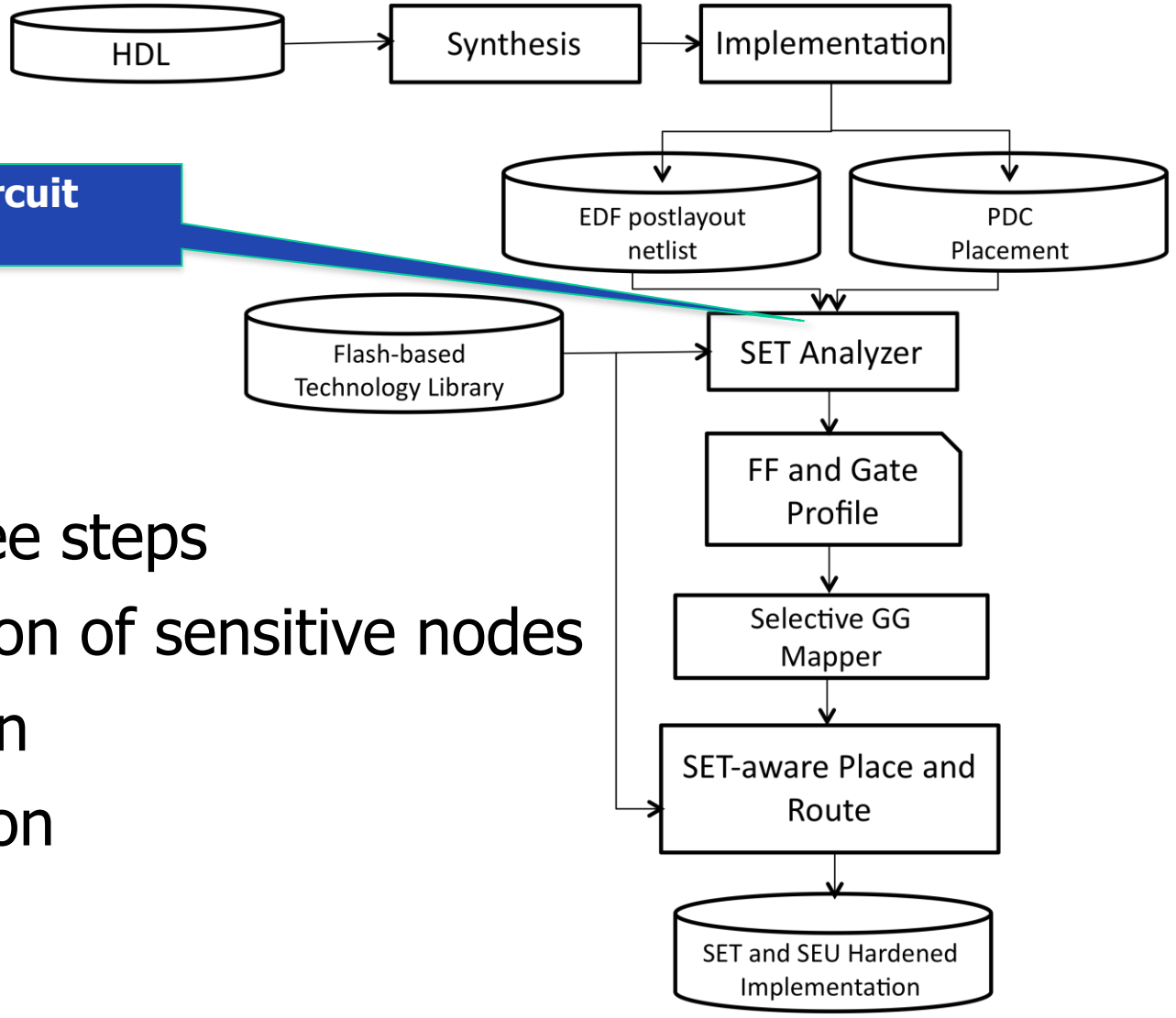


The proposed method (iii)



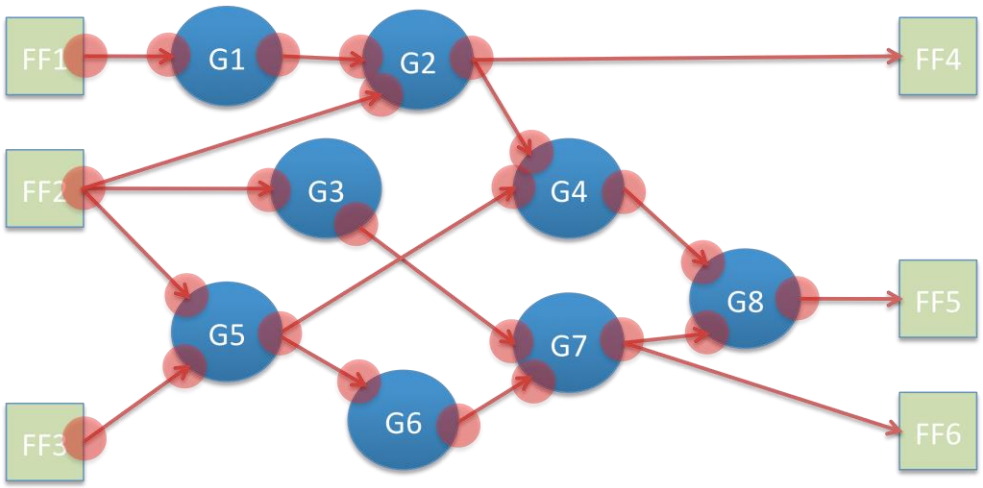
Analysis of the SET circuit sensitivity

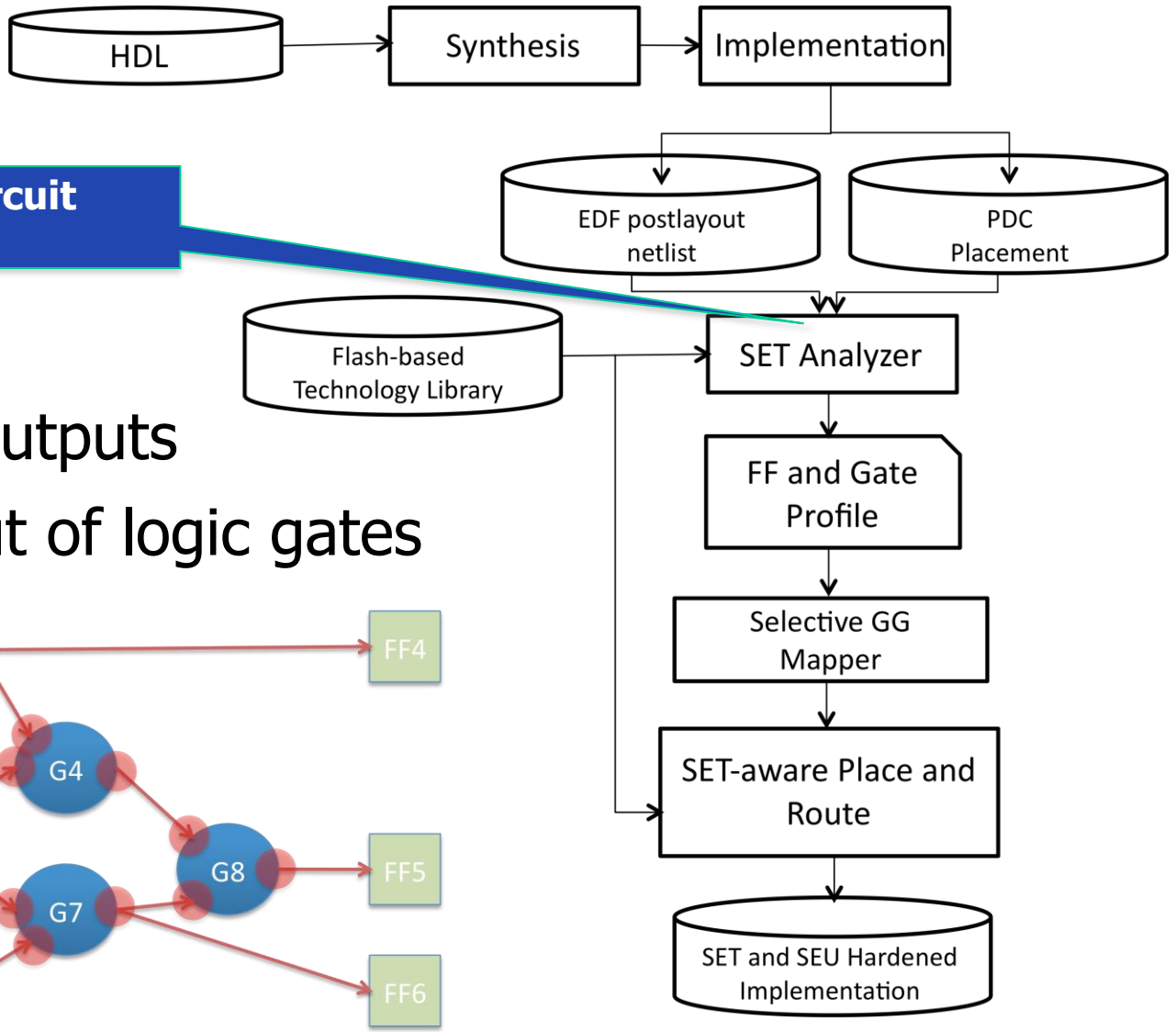
- Executed in three steps
  - Identification of sensitive nodes
  - Propagation
  - Classification

The proposed method (iii)

Analysis of the SET circuit sensitivity

- Terminal node outputs
- Input and output of logic gates

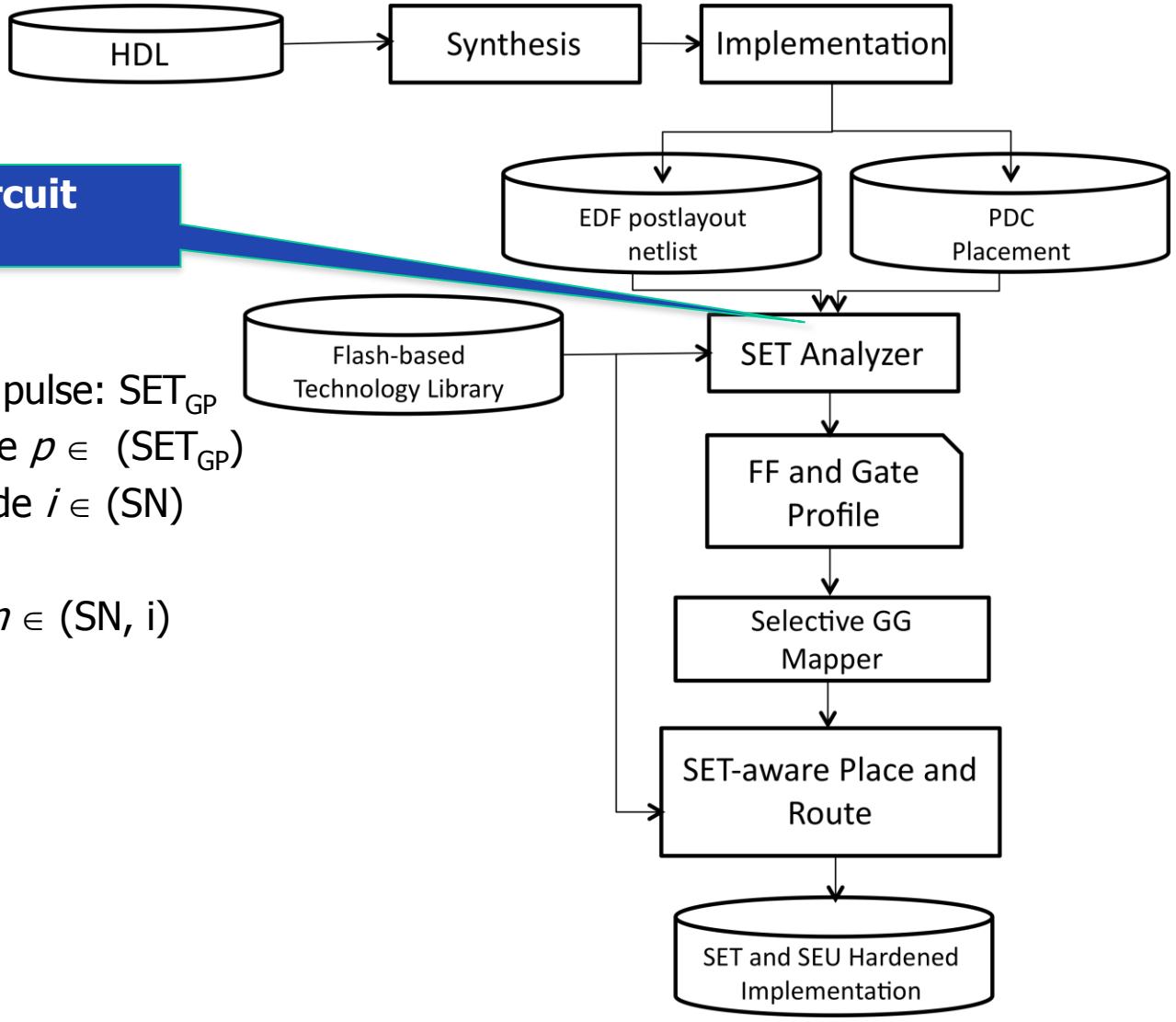




The proposed method (iii)

Analysis of the SET circuit sensitivity

1. Generate the list of SET pulse: SET_{GP}
2. For each generated pulse $p \in (SET_{GP})$
   2. For each sensitive node $i \in$ (SN)
   Apply pulse p to i
   Find destination node $dn \in$ (SN, i)
      3. For each dn
      Propagate p on (i, dn)



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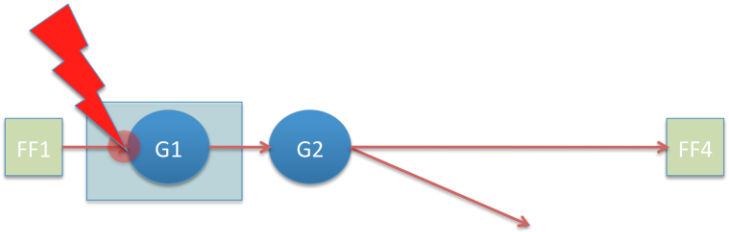

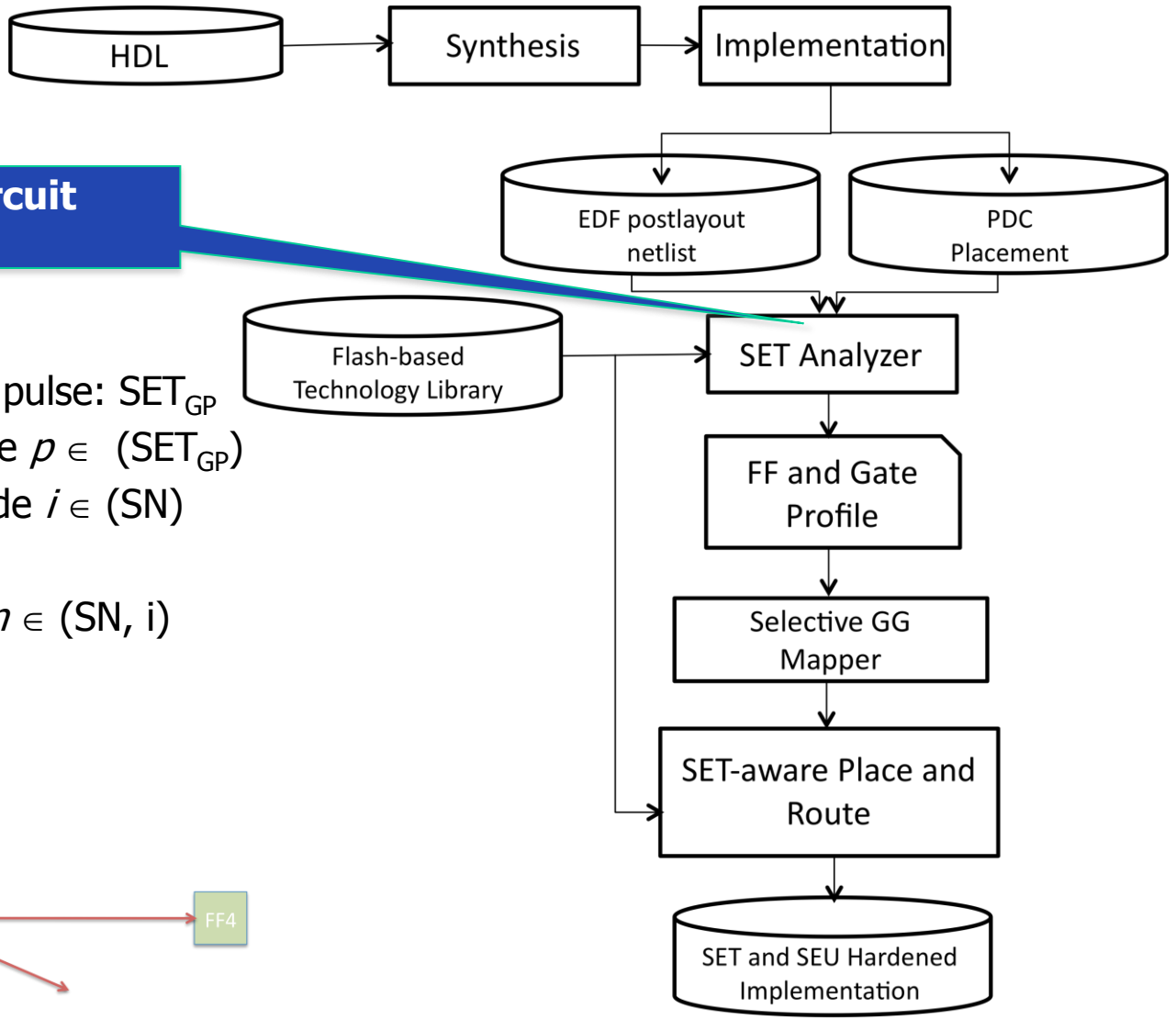

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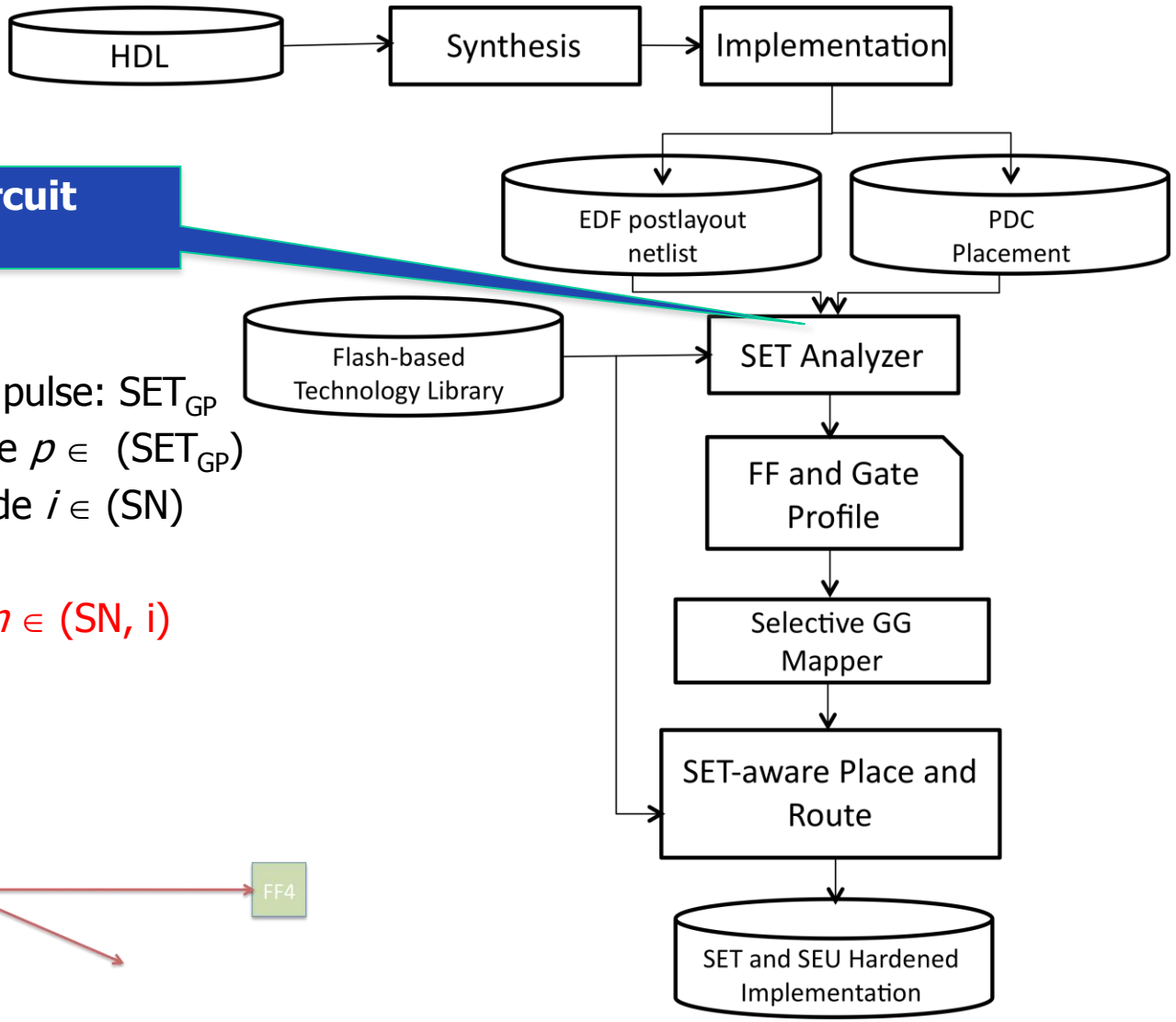

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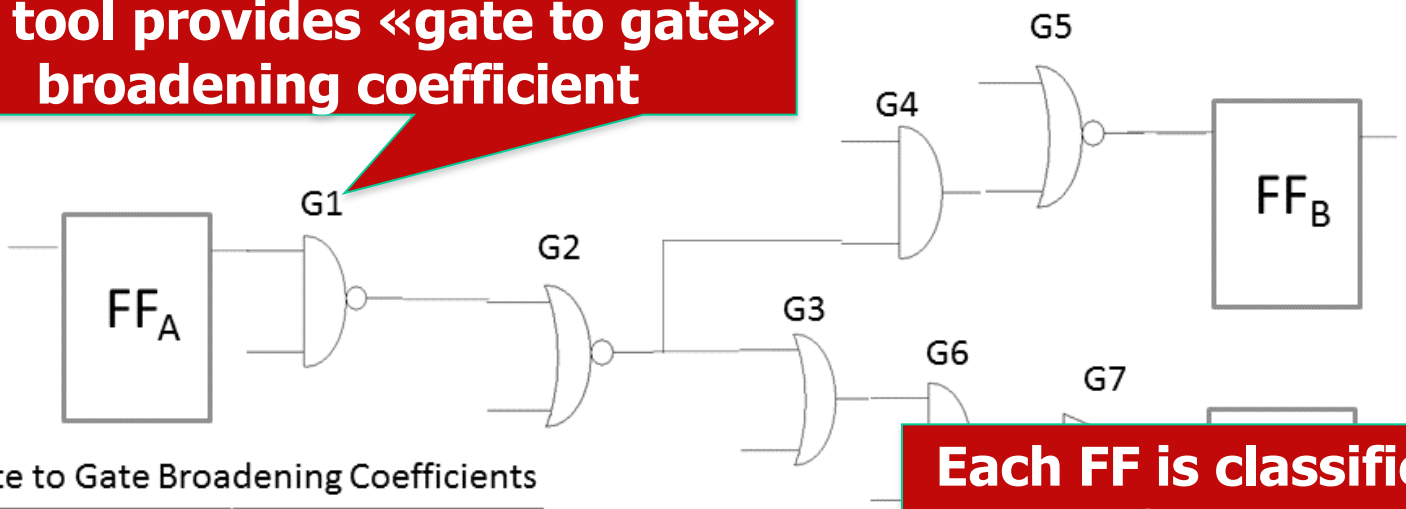
P_{G1} is transformed in P_{G2}

Flip-Flop and Gate SET profiles

The tool provides «gate to gate» broadening coefficient



Gate to Gate Broadening Coefficients

Gate to Gate	Broadening [ns]
FFA – G1	-0.128
G1 – G2	0.458
G2 – G4	0.070
G2 – G3	-0.090
G3 – G6	0.480
G6 – G7	0.092
G7 - FFC	0.140
G4 – G5	-0.094
G5 - FFB	0.130

Each FF is classified on the basis of its maximal pulse broadening

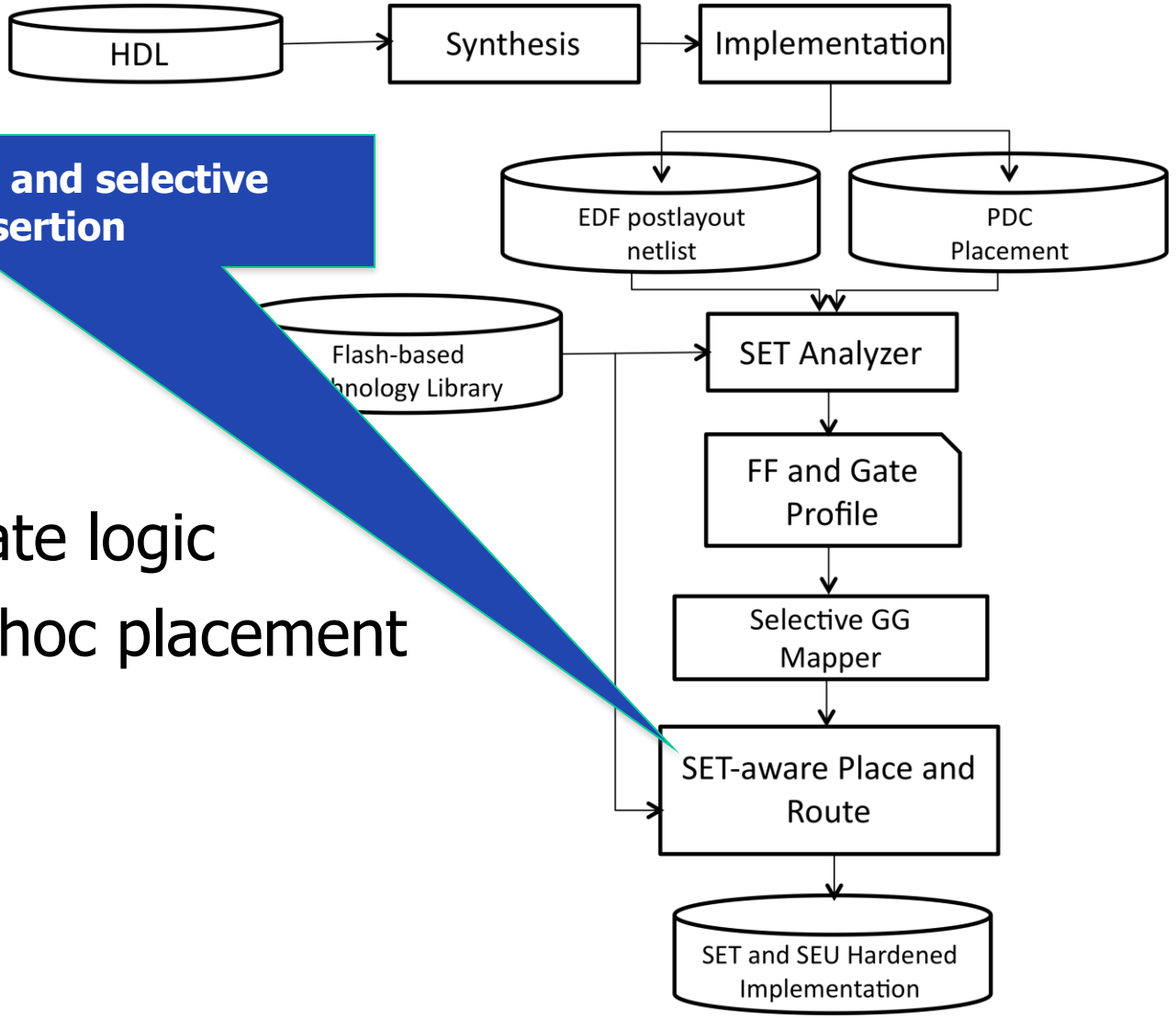
FFs maximal broadening pulses

Flip-Flop	Maximal Pulse [ns]
FFB	0.436
FFC	0.952

The proposed method (iv)

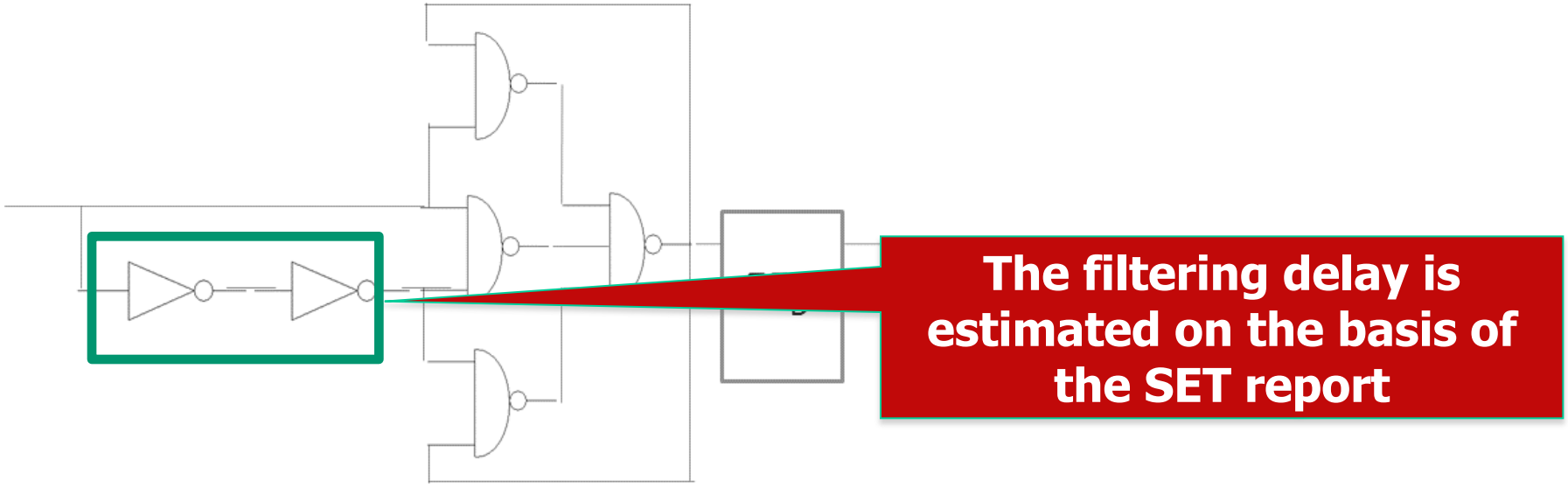
SET-aware placement and selective Guard-Gate insertion

- Inserts guard gate logic
- Performs an ad-hoc placement



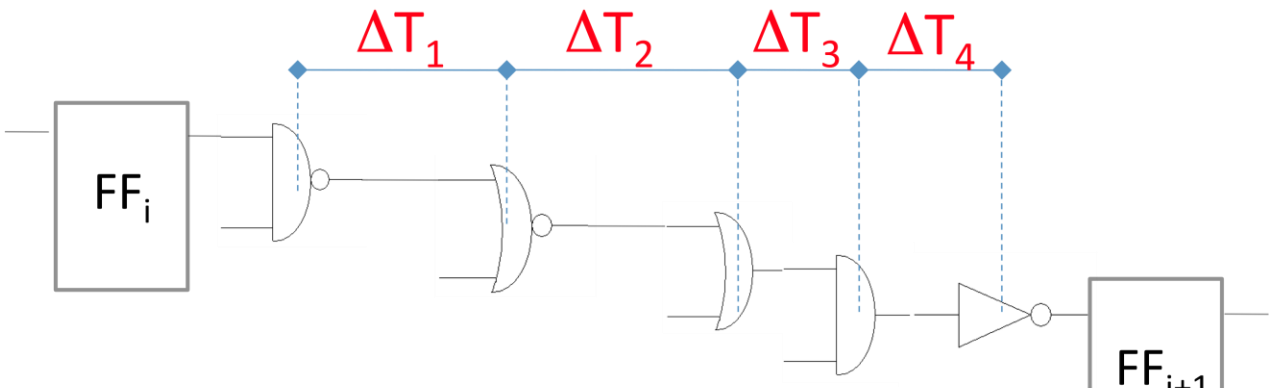
Selective Guard Gate Mapper

- It inserts a guard gate logic structure on the input of the selected FF
- It acts on the paths the remains critical at the end of the SET analysis phase
- The overhead of each guard gate structure depends on the maximal pulse broadening



SET-oriented Placement algorithm

- It acts on the critical gate paths reported by the SET analyzer
  - If a gate G and the next gate G+1 are inverting gates the placement is performed in the closest position
  - In other cases the placement is performed in a longer distance



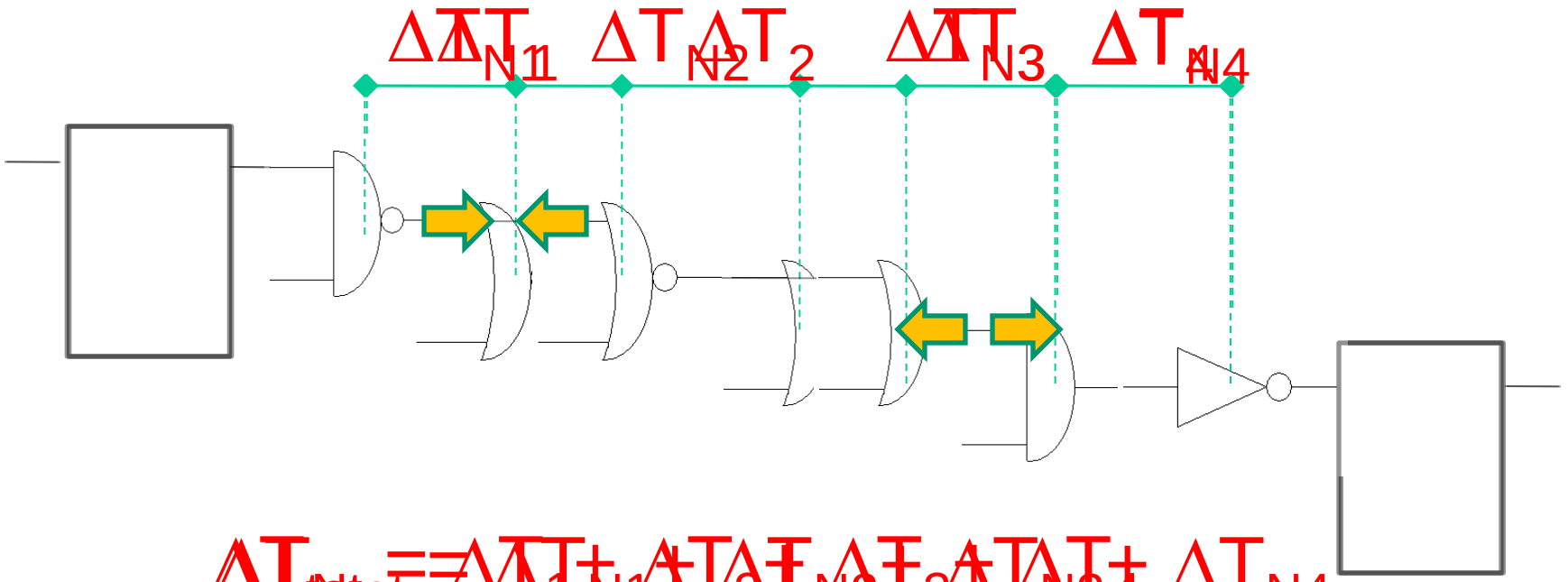
$$\Delta T_{tot} = \Delta T_1 + \Delta T_2 + \Delta T_3 + \Delta T_4$$

SET-oriented Placement algorithm

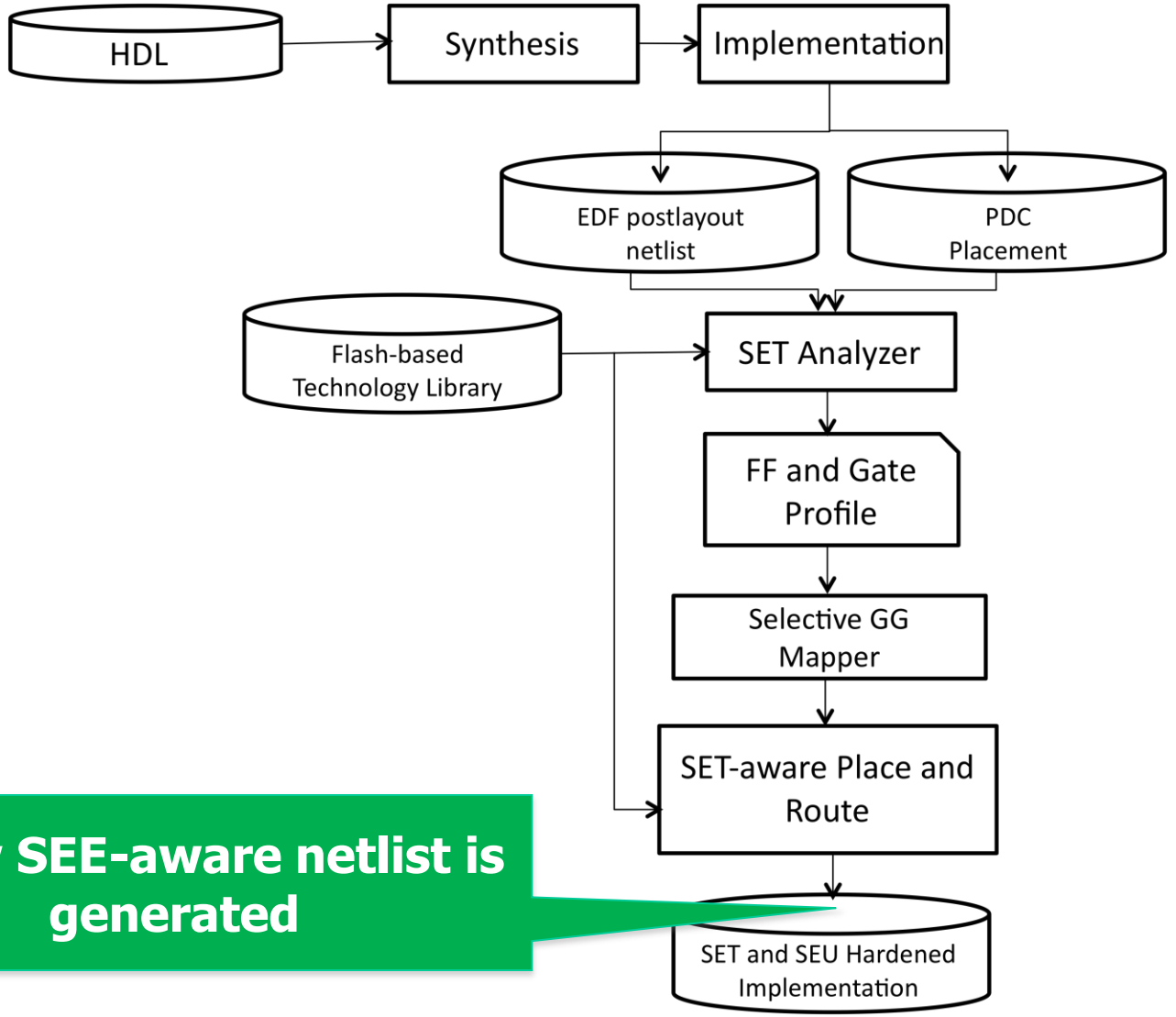
$\Delta T_{N1} << \Delta T_1 \quad \Delta T_{N3} >> \Delta T_3$

$\Delta T_{N2} = \Delta T_2 \quad \Delta T_{N4} = \Delta T_4$

$\Rightarrow \Delta T_{Ntot} = \Delta T_{tot}$

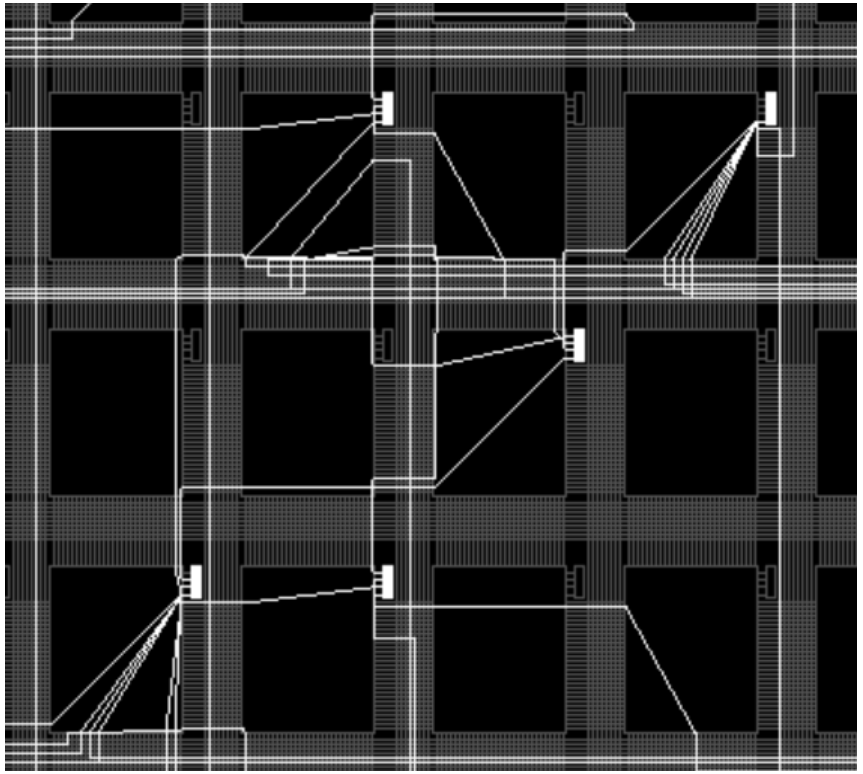


The proposed method (v)



The proposed method (vi)

- The Place and Route algorithm is based on the CAD tool Polito framework
  - Ad-hoc FPGA architecture layout
  - Placer algorithm
  - Routing algorithm

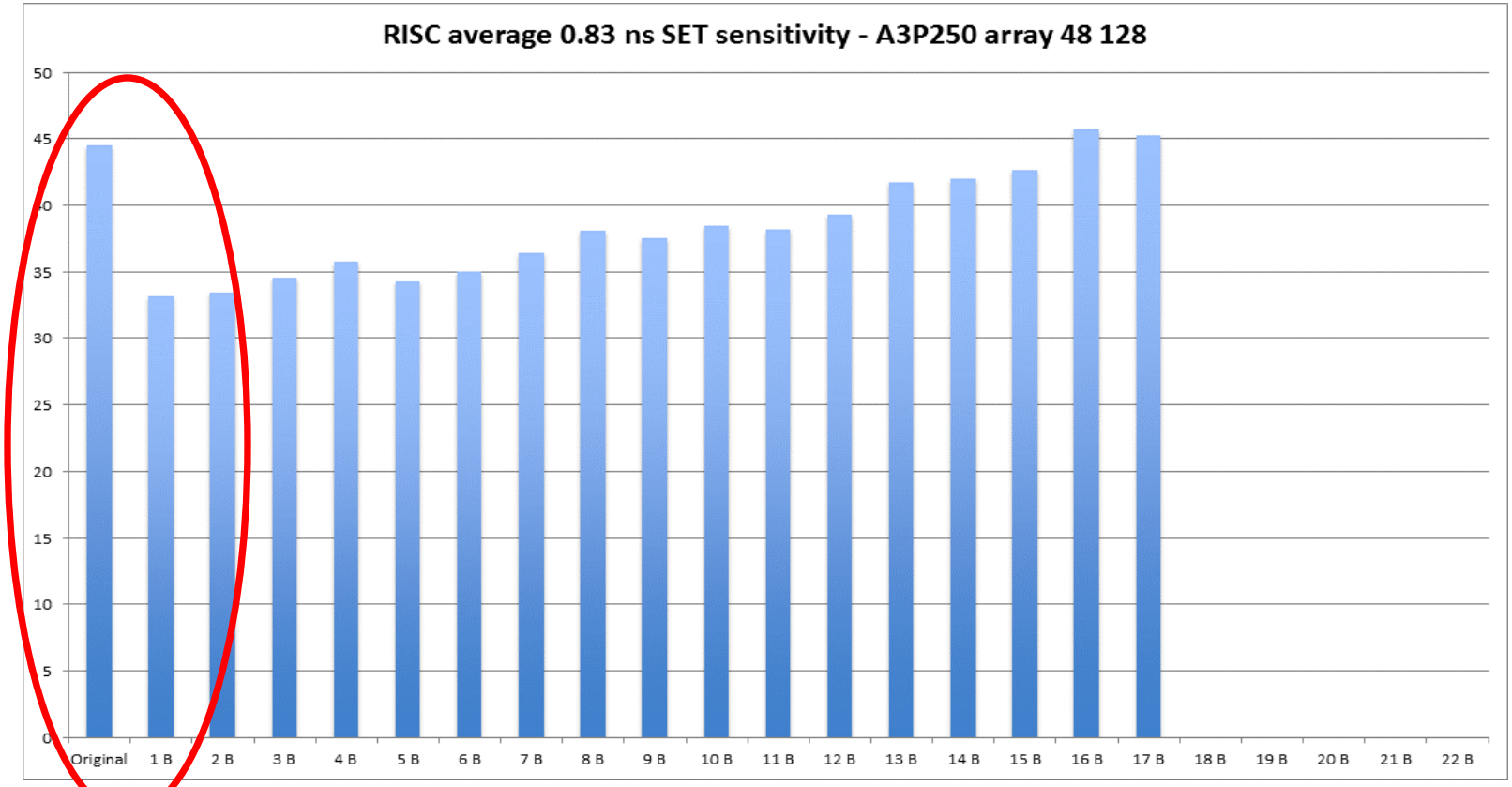


The SETA tools

- The analyzer allows to obtain:
  - Maximal broadening report and Maximal Pulse report
  - Detailed analysis of each FF
- The placer and routing algorithm:
  - User defined array area
  - Evaluate, perform or modify a solution
  - User defined delay coefficient

The SETA tools

- [%] of sensitivity on the whole design FFs



Experimental results (i)

- Implementation of a set of circuits on Microsemi ProASIC3 Flash-based FPGA
  - 130 nm
- Analysis of microprocessor cores: Intel 8051 and a RISC processor
- The experimental analysis includes
  - SEE static analysis
  - SEU and SET simulation
  - Heavy Ions Radiation Test (applied on RISC core)

Circuits characteristics

Design name	Logic Gates	FFs
B04	493	67
B05	415	66
B12	565	123
B13	162	50
8051	3,414	249
RISC Plain	1,401	1,156
RISC TMR + GG (1ns)	20,808	3,468
RISC TMR - FF	4,203	3,468
RISC our method	5,514	3,468

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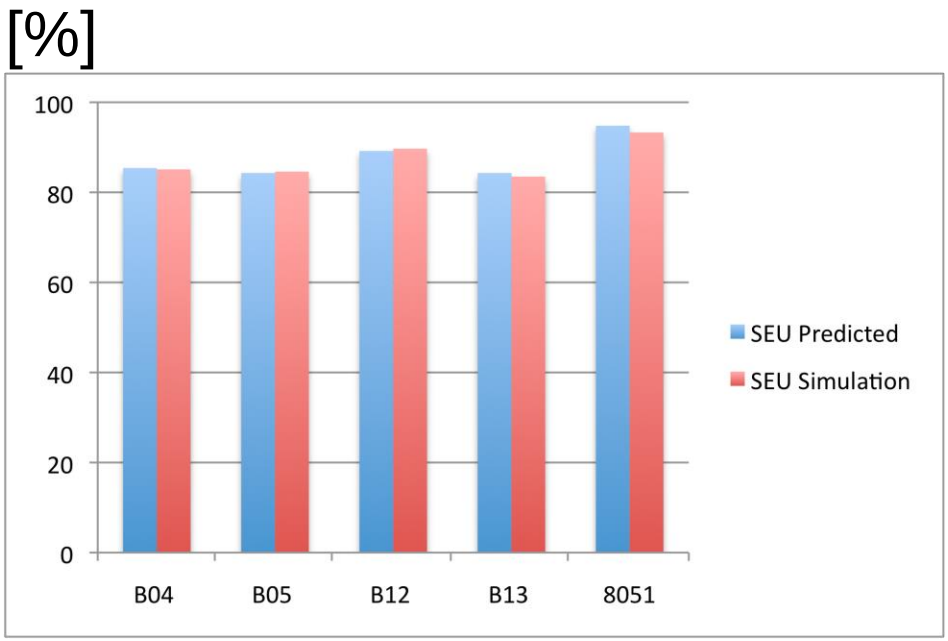
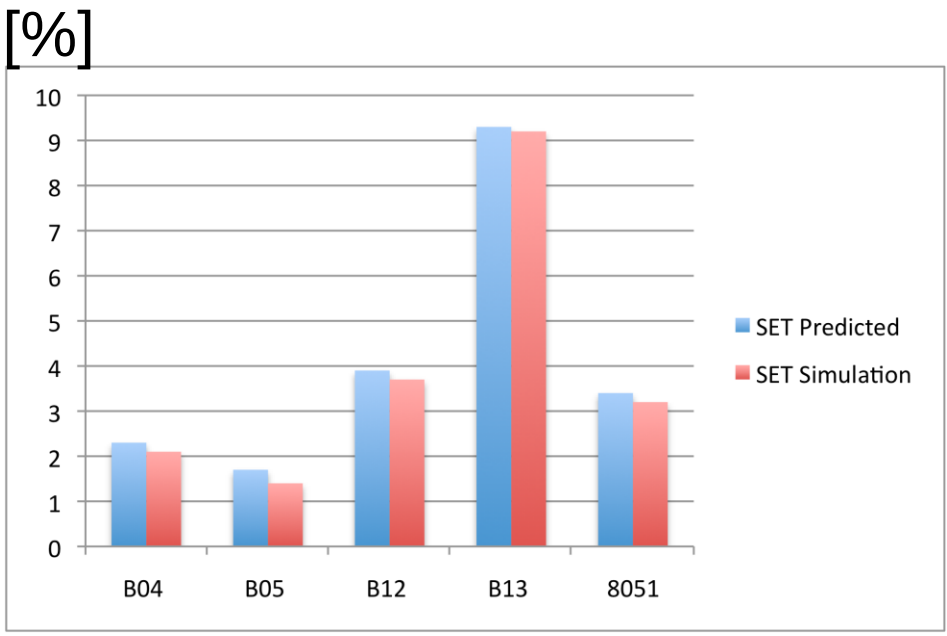
Limited area overhead if compared to other hardening techniques

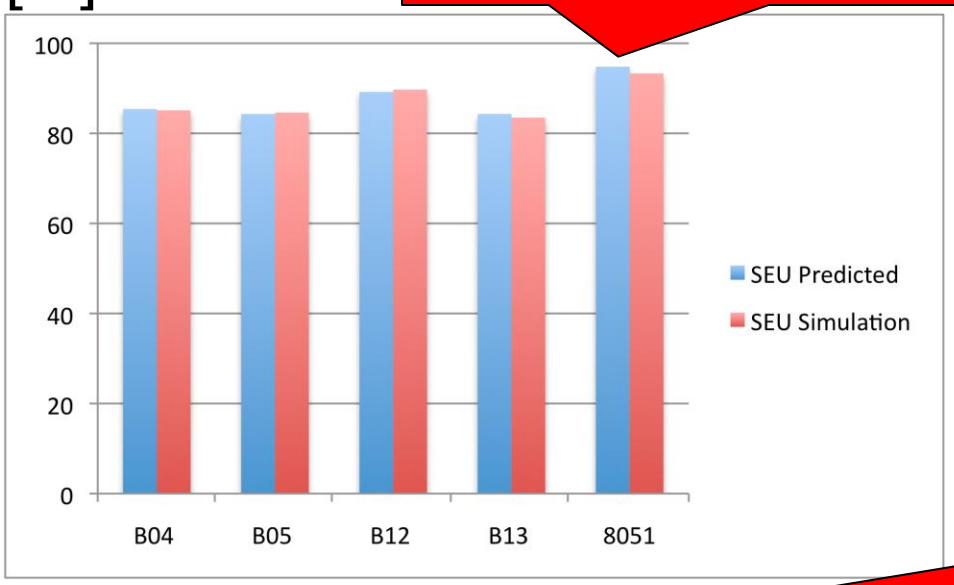
SEU and SET analysis

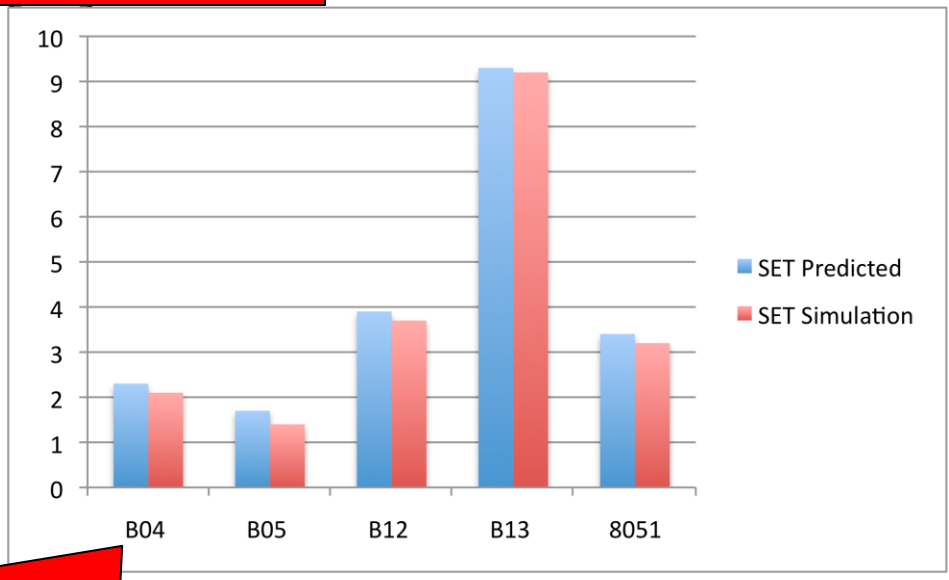




SEU and SET analysis

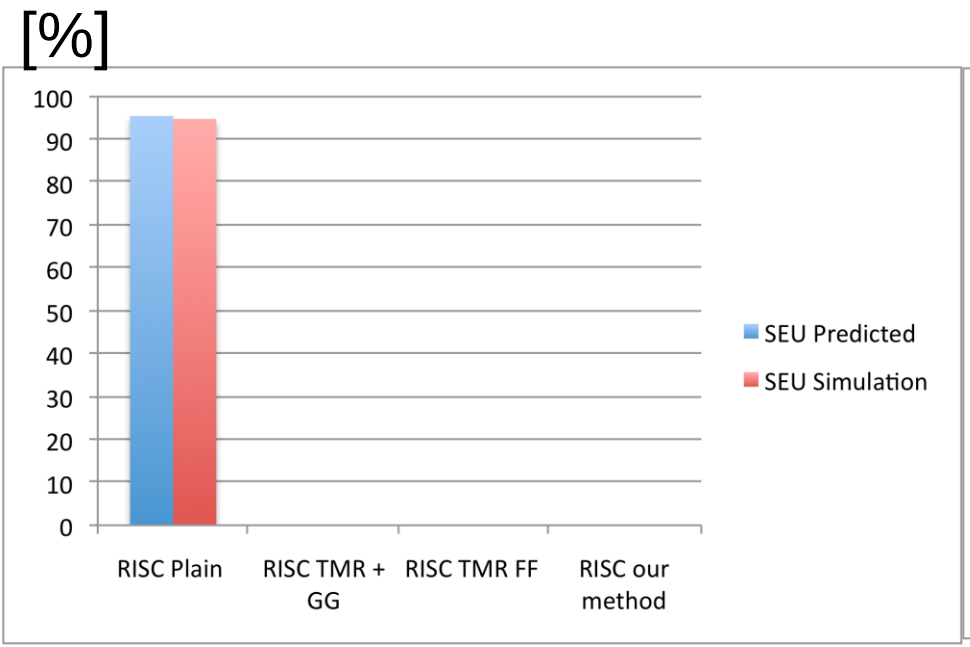
SEUs static prediction is accurate (precision < 0.5%)

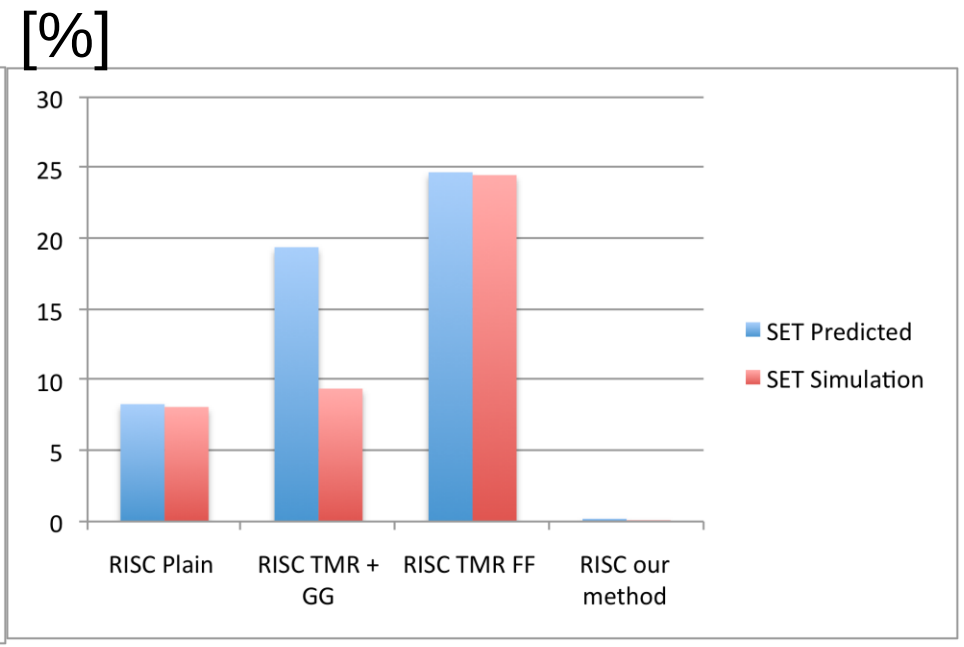




SETs static prediction is accurate but pessimistic (<1.5%)

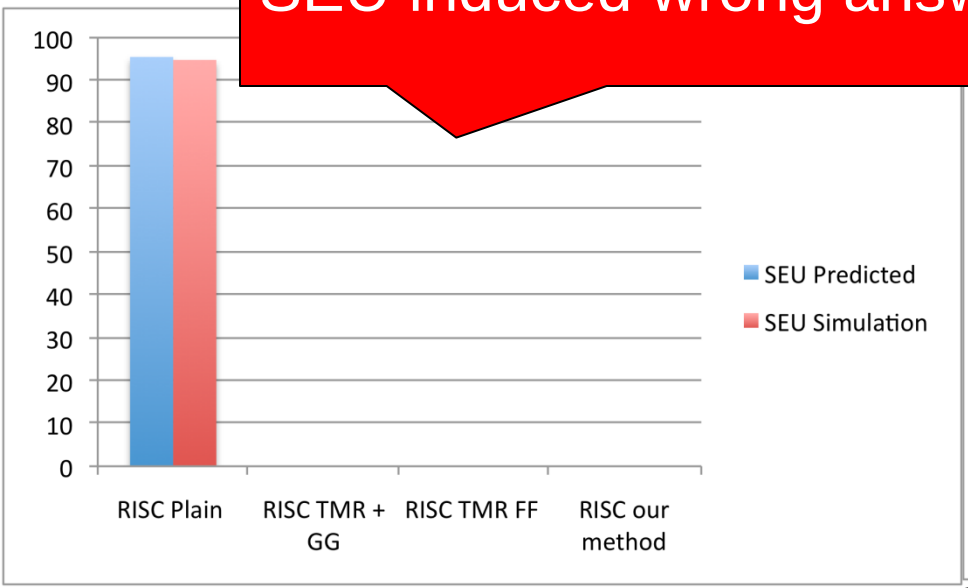
RISC analysis

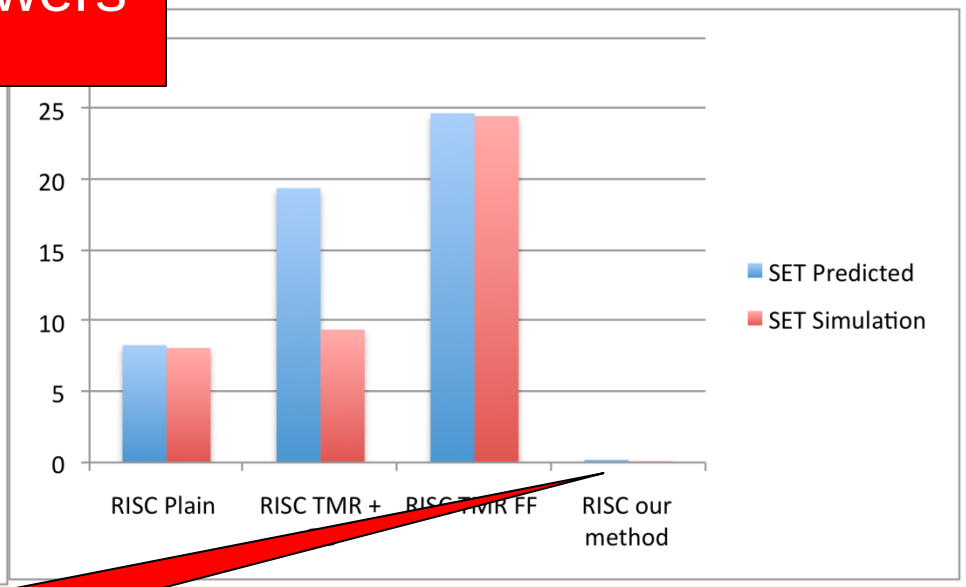




RISC analysis

Mitigation techniques nullify SEU induced wrong answers





The proposed solution drastically reduce the sensitivity against SETs

RISC analysis

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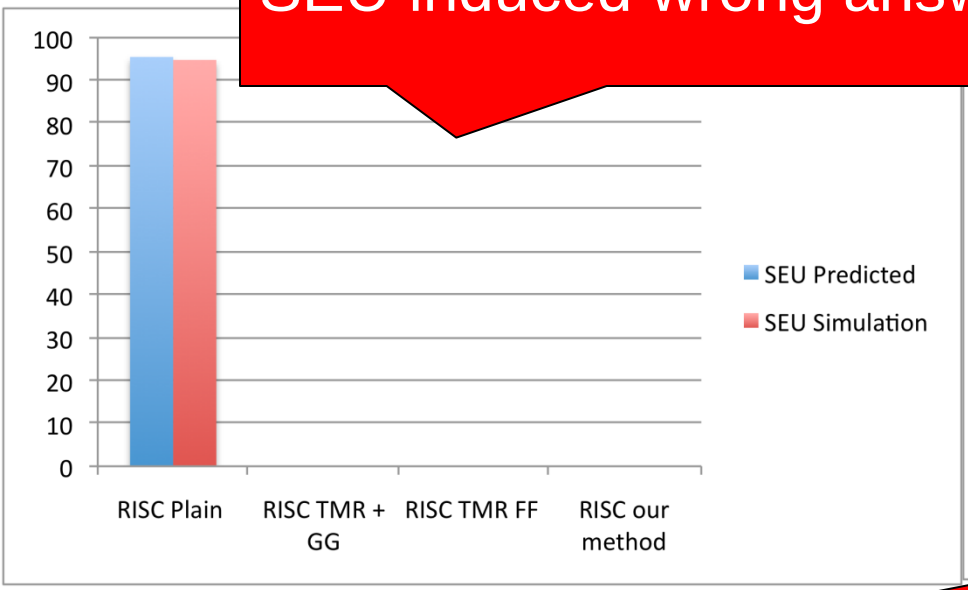
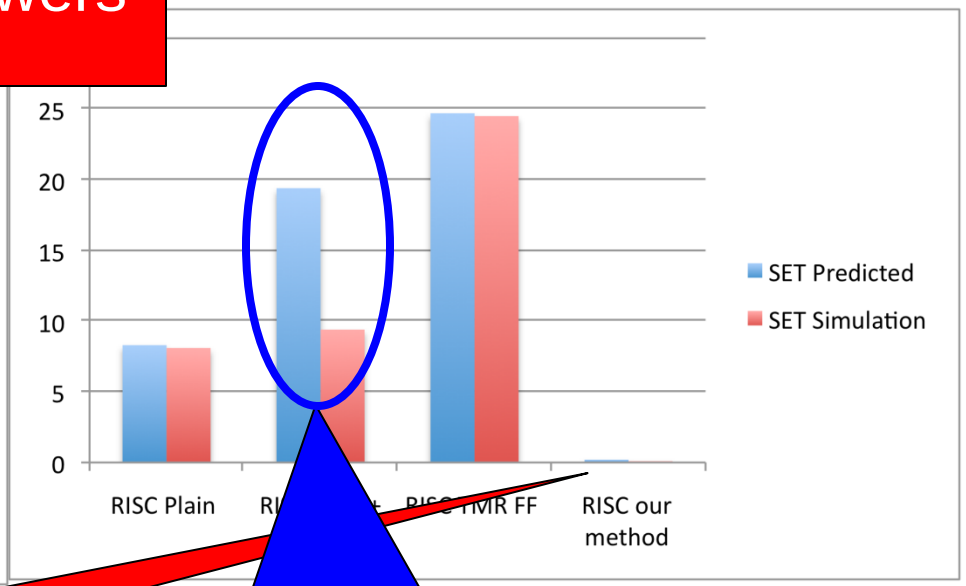




The proposed solution drastically reduce the sensitivity against SETs

Simulation model weakpoint: it does not model broadening effects on SETs

Radiation test analysis

- Heavy ions test performed at the Cyclotron of the Université Catholique de Louvain (UCL)
  - Kripton ion with a fluence of 3.04E8 (particles)
  - Average flux 1E4 (particles/sec)
  - RISC working frequency of 20MHz

RISC processor version	SEE Cross-section [MeV cm^2/mg]
Unhardened	1.45E-9
Full TMR + GG	6.37E-10
Our Approach	3.12E-12

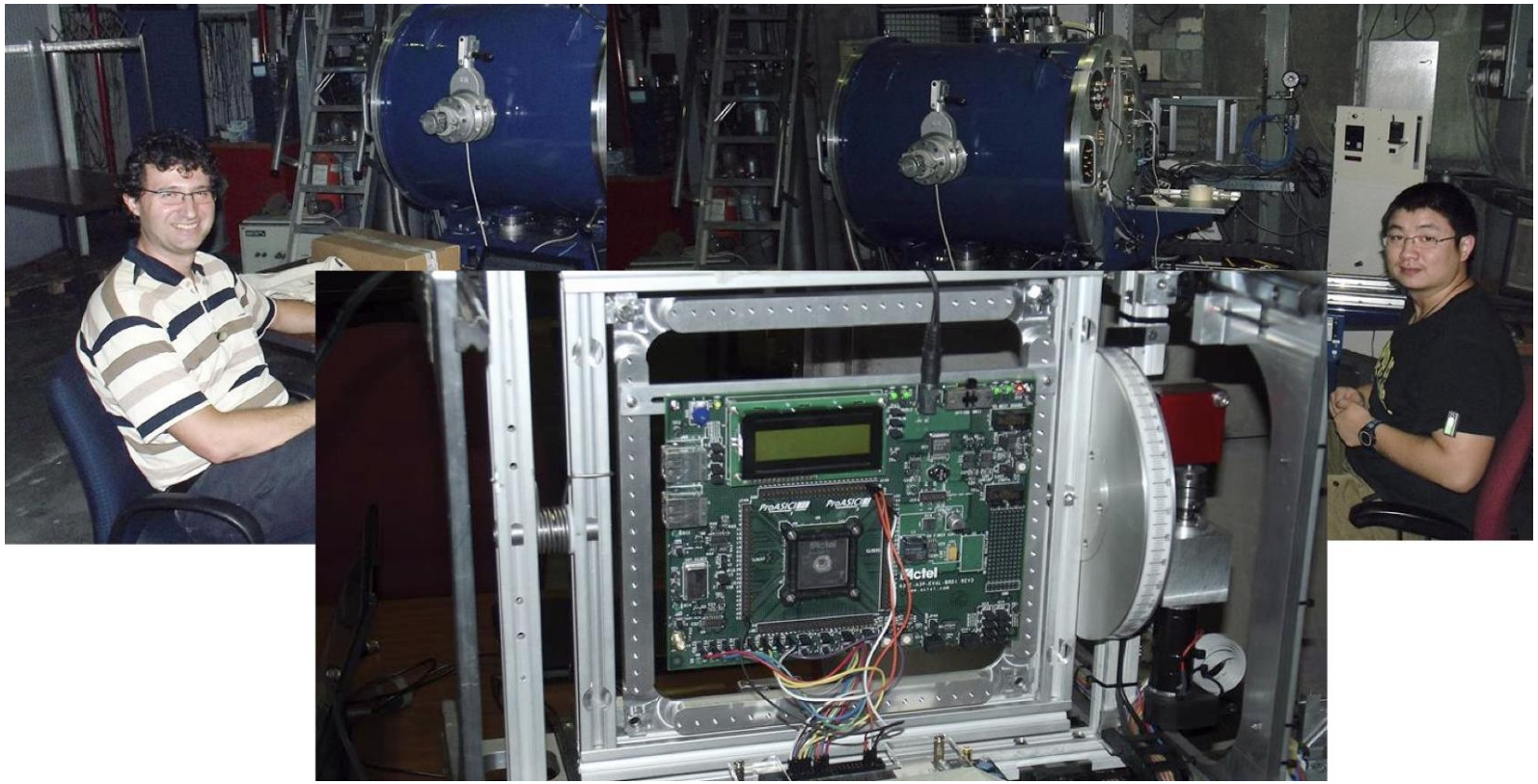
Demo

- SETA analysis execution
  - Detailed report presentation
  - Test on real circuits
- Place and Route
  - Technology library and layout database
  - Placement test
  - Routing test
  - Layout view

Future works

- Perform further evaluation on the performance trade-off
- Analysis of ARM processor core embedded on A3P3000 Microsemi FPGA
- Application of the approach on ASIC technology

Thank you for your attention



[Photos taken during Heavy Ions Radiation Tests in Louvain-la-Neuve]

SEU and SET analysis

Design mame	SEU Wrong Answer [%]		SET Wrong Answer [%]	
	Predicted	Simulation	Predicted	Simulation
B04	85.4	85.1	2.3	2.1
B05	84.3	84.6	1.7	1.4
B12	89.2	89.7	3.9	3.7
B13	84.3	83.5	9.3	9.2
8051	94.8	93.3	3.4	3.2
RISC Plain	95.5	94.8	8.3	8.1
RISC TMR + GG	0	0	19.4	9.4
RISC TMR FF	0	0	24.7	24.5
RISC our method	0	0	0.2	0.1