SEFUW: SpacE FPGA Users Workshop, 2nd Edition

Tuesday 16 September 2014 - Thursday 18 September 2014

European Space Research and Technology Centre (ESTEC)

SEFUW 2014 is organised with the support from Thales Communications & Security

Tuesday 16 September 2014

Registration (09:30 – 10:00)

Welcome to SEFUW 2014 (10:00 - 10:15)
Presenter: Mr. DANGLA, David (CNES); Mr. MERODIO CODINACHS, David (ESA)

Session FPGA/CAD Vendors: (10:15 – 11:30)
Chair: *Mr. MERODIO CODINACHS, David (ESA)*

	10:15	**RHBD FPGA AT40K Family** *Presenter: Mrs. BRIOT, Valerie (ATMEL)* ATMEL has proven the principle of the RHBD FPGA after its first experiences on the AT40 and ATF280 devices. Thanks to the use of RHBD FPGA, users do not have to take into account any mitigation techniques, SEE is guaranteed by design. And, thanks to the use of SRAM-based FPGA, users can perform unlimited reprogramming. ATMEL is currently introducing new device and Multi Chip Modules (MCMs): - The ATFS450 with up to 450K equivalent ASIC gates, using a 150 nm SOI technology - The ATF697 including a AT697 processor and a ATF280 FPGA - The ATFee560 including 2 ATF280 FPGA and 2 AT69170 EEprom A presentation of the products will be done, with some examples of application on Evaluation Kits, including communication links between boards.
	11:05	**IDS/FIGARO Enhancement Program** *Presenter: Mr. BRICARD, Yohann (ATMEL)* ATMEL has been working for 1 year to improve the overall quality of the tools. A new team has been created to implement new quality standards, provide new features and Enhance Mentor Precision tool integration. It includes the management of pre-placed/routed IPs.

Session: Design for Space Applications: Tools (11:30 – 13:00)
Chair: *MERODIO CODINACHS, David (ESA)*

	11:30	**Analysis and Mitigation of SEUs on SRAM-based FPGAs using the VERI-Place tool** *Presenter: Prof. STERPONE, Luca (Politecnico di Torino)* Single Event Upsets on SRAM-based FPGAs is a hot topic for more than a decade. After different investigations have been performed, a first algorithm for the prediction of SEU error probability on circuits on SRAM-based FPGAs is presented and analyzed by software prediction and fault injection analysis. Experimental results and comparison with other methods such as Xilinx Essential Bits report are provided.
	12:00	**Role of Fault Injection in Digital Design for Space** *Presenter: Dr. AGUIRRE, Miguel A.; Dr. GUZMAN MIRANDA, Hipolito (Universidad de Sevilla)* Fault injection over an integrated circuit is a procedure that mimics the consequences of Single Event Effects within radiation environments, and checks, when they are transformed into faults, how are they managed by the circuit logic. During the normal flight time of the integrated circuit, radiation is one of the most relevant source of anomalies of the circuit functional behavior. Impacts of energetic particles on critical points can change the current state of a digital circuit driving it to an unexpected evolution and to unpredictable consequences. The present abstract pursues the clarification of the role of fault injection in the context of radiation and radiation testing. If radiation is a big concern in the context of microelectronics for space applications, fault injection can help to analyze part of the problem, understanding well its limits and its role within the problem. Fault injection has been traditionally intended to be part of the set of tests just before the tapeout of an ASIC or the configuration of an FPGA. Authors have experienced that there is its use can be even richer if used as a design tool. Both roles, design and test, will be further analyzed.

	12:30	**SETs Broadening Tuning: A Place and Route Approach** *Presenter: Prof. STERPONE, Luca (Politecnico di Torino)* Transient Pulse broadening is a realistic phenomena induced by high-energy particles in deep-submicron technology. Electrical filtering has been demonstrated to be an effective solution to reduce the overall SET broadening effect. In this presentation an approach based on the Place and Route algorithm is presented and commented with a realistic application to Flash-based FPGAs.

Networking Luncheon (13:00 – 14:00)

Session: Design for Space Applications: Fault Tolerance Methodologies (14:00 – 15:30)
Chair: *Mr. DANGLA, David (CNES)*

	14:00	**FPGA use in future space rover navigation** *Presenter: Dr. LENTARIS, George (National Technical University of Athens, Greece)* Future planetary exploration will rely on autonomous space rovers with increased moving speed and highly accurate visual odometry algorithms. ESA estimates that the 2020+ Mars missions will involve stereo cameras on robots moving at 6cm/s and calculating high definition depth maps in less than 20sec. Moreover, the error of these processes shall be less than 2m when traveling 100m paths and less than 2cm when calculating the depth of objects located 4m away from the rover. Given the low processing power of the space-grade CPUs, executing such complex computer vision algorithms requires an excessive amount of time, e.g., minutes or even hours, i.e., much greater time than the aforementioned specifications. The solution being explored today is to use space-grade FPGA devices for accelerating the rover's visual processes with speed-up factors in the order of 10x to 1000x. In the context of project SEXTANT of ESA, we perform HW/SW co-design to implement a number of computer vision algorithms on a custom HW/SW system consisting of a PC (emulating the space-grade CPU) and a Virtex-6 XC6VLX240t-2 FPGA device (emulating the space-grade FPGA). The developed algorithms are combined to form a robust visual odometry pipeline and a stereo vision pipeline used for the “localization” and “mapping” modes of operation of the space rover, respectively. The former inputs one 512x384 stereo image and outputs the pose of the rover once every second, whereas the latter inputs three 1120x1120 stereo pairs and outputs a 3153x1051 depth map once every 8.4 seconds. Our “localization” pipeline utilizes the Harris corner detector, the SIFT corner descriptor, a feature matching function, as well as functions for filtering and motion estimation. Our “mapping” pipeline utilizes the plane-sweep algorithm. The algorithms/pipelines are selected after extensive cost-performance evaluations. Their HW/SW partitioning relies on detailed profiling and algorithmic analysis, which considers various computational requirements (time, memory, arithmetic accuracy, etc) and the capabilities of the underlying HW. The outcome of such analysis allows us to determine those parts that must be accelerated by FPGA and those suitable for SW execution. Thus, we implement on FPGA the corner detection, description, matching, and stereo correspondence algorithms, which account for 96% to 99% of the total computations of the system. The proposed architecture bases on input data decomposition, resource reuse, pixel pipelining, parallel memory organization, parallel computation of mathematical formulas, and modification/optimization in algorithmic level. Moreover, we develop a custom CPU-FPGA communication scheme with raw Ethernet packets to facilitate the HW/SW co-processing. The HW modules are coded with parametric VHDL to allow tuning at the final stage of SEXTANT, which ultimately leads to a HW/SW system meeting all ESA requirements. In particular, our HW accelerators achieve significant speed-up factors with respect to the space-grade CPU: 63x for detection, 100x for description, 125-425x for matching, and up to 1111x for stereocorrespondence. The final HW/SW system achieves a speedup of 16x for localization and 444x for mapping mode, both with sufficient accuracy and HW cost (36% FPGA LUTs and 78% FPGA RAM utilization for localization, 10% LUTs and 57% FPGA RAM for mapping). Overall, the results of SEXTANT verify the necessity of using FPGA to perform efficient visual navigation of space rovers.
	14:30	**Dynamically Reconfigurable Hardware for Resource Efficiency and Fault Tolerance in Space Applications** *Presenter: Mr. COZZI, Dario (Bielefeld University)*

		Reconfigurable hardware is gaining a steadily growing interest in the domain of space applications. The ability to reconfigure the information processing infrastructure at runtime together with the high computational power of today's FPGA architectures at relatively low power makes these devices interesting candidates for data processing in space applications. Partial dynamic reconfiguration of FPGAs enables maximum flexibility and can be utilized for performance increase, for improving energy efficiency, and for enhanced fault tolerance. The DRPM platform (Dynamically Reconfigurable Processing Module) was developed as a highly scalable prototyping environment for satellite payload processing systems, combining dynamically reconfigurable FPGAs with the required interfaces such as SpaceWire, MIL-STD-1553B, and SpaceFibre. Partial reconfiguration of the FPGA area is supported by a dedicated hardware IP core, enabling maximum reconfiguration speed. Additionally, the IP core realizes blind and readback scrubbing with scrub rates that can be adapted individually for different parts of the design. The presentation will recap the architecture of the DRPM as well as interface and processing performance achievable using the DRPM platform for different applications with a special focus on the integrated SpaceFibre interfaces. Furthermore, the presentation will give details on the development of a tool flow for detection and correction of permanent faults in FPGAs during a space mission. Once faults have been detected and located, the flow generates fine-grained patch hard macros that are used to mask out the discovered faulty resources, allowing partially faulty regions of the FPGA to be available for further use. In this activity, the DRPM is used as a test platform for benchmarking and evaluation. During the demo session, the scrubbing and processing performance of the DRPM is demonstrated, streaming a sequence of images thought the SpaceWire and SpaceFibre interfaces.
	15:00	**From Rosetta to current developments using FPGAs for scientific space missions** *Presenter: Mr. LANGE, Tobias (IDA TU Braunschweig)* More than one and a half decade ago, the Data Processing Unit (DPU) of the Rosetta Orbiter Spectrometer for Ion and Neutral Analysis (ROSINA) instrument was developed at IDA using a processor system and 6 Actel RT14100A devices, providing a total capacity of only about 8k logic modules with fixed functionality. Nowadays, the DPU for the Polarimetric and Helioseismic Imager (PHI) instrument on Solar Orbiter will have a total capacity of more than 140k logic cells with even higher functionality and embedded memory, which also shows the dramatically increased complexity of such a development. Additionally, almost the complete functionality is reconfigurable during flight by using radiation tolerant SRAM-based Xilinx FPGAs. This is necessary to cope with the demanding on-board processing capabilities, i.e. to handle very high data rates, extract and process final physical values by an autonomous, intelligent, and reliable application already on-board the spacecraft, and adapting itself to the changing mission needs. Classical ground-processing steps need to be performed on-board, making this a design driver for future robotic missions and planetary landers. The benefits of such an adaptable processing platform are a superior data yield and a reduced risk of a total instrument loss. An additional advantage of adaptability is the possibility to time-share resources for a more efficient hardware and power utilization, when dedicated functions are not necessary at the same time. After having demonstrated the successful usage of SRAM-based FPGAs for scientific instruments with the SRAM FPGA-based computer for the Venus Monitoring Camera (VMC) on Venus Express, the first development using in-flight reconfigurability is currently done for the PHI instrument on Solar Orbiter. PHI will provide maps of the continuum intensity, the magnetic field vector and the Line-Of-Sight velocity in the solar photosphere. The polarimeter measurement technique of PHI is ideally suited to apply a robust and reliable technique to obtain maps of the physical quantities already on-board. A non-linear, least square, iterative process is used for this Radiative Transfer Equation (RTE) inversion, which is utilizing the parallel structures of FPGAs to speed up processing. Additionally to the implementation of the FPGA configuration, a mission specific qualification for assembly of the ceramic flip-chip column grid array (CF) package of the used Xilinx device is performed since no qualified process manufacturer for such an assembly was available in Europe. The basic architecture of the PHI DPU design is based on the results of the ESA study for a Dynamically Reconfigurable Processing Module (DRPM). A modular processing system based on SpaceWire communication, featuring an ASIC processor as system controller, a

		static configuration controller FPGA and two reconfigurable SRAM-based FPGAs was built in the scope of investigating in-flight dynamic partial reconfiguration of FPGA technology, which was a joint effort of Astrium Ltd. and IDA. Within the framework of the DFG research unit Controlling Concurrent Change (CCC) at TU Braunschweig, we are developing a controlled change application using reconfigurable FPGAs under the challenging constraints of space missions. The exchange of single modules has to be possible without modifying the overall system, i.e. without degrading the once achieved qualification for functionality, performance and external behavior. The primary objective is to demonstrate usability and capabilities of autonomy using the mechanisms developed in CCC under the safety, reliability and availability requirements of a typical space application in order to maximize the use of resource limited HW platforms in a multi-functional and adaptable manner. Reconfigurable SRAM-based FPGAs are very susceptible to radiation effects and the system reliability and qualification has to be guaranteed in the harsh space environment. Therefore, the PHI DPU will be equipped with dedicated mitigation techniques against SEEs (Single Event Effects), such as read back scrubbing via JTAG. Further details will be given during presentation, together with some general design issues and tools.

Networking Coffee Break sponsored by Thales Communications & Security (15:30 – 16:00)

Demo Session and Cocktail Reception sponsored by Thales Communications & Security (16:00 – 18:00)
Chair: *Mr. DANGLA, David (CNES)*

SEFUW Dinner (20:00 – 22:30)
3 Course Menu and drink arrangement at “Iets Anders in Bistro Bardot"
(Pickeplein 4 - 2202 CK Noordwijk)

Wednesday 17 September 2014

SEFUW Intro – Opening Remarks (08:50 - 09:00)
Presenter: Mr. DANGLA, David (CNES); Mr. MERODIO CODINACHS, David (ESA)

Session: FPGA/CAD Vendors (09:00 – 10:40)
Chair: *Mr. PRESSECQ, Francis (CNES)*

09:00	**Update on Microsemi Radiation Tolerant FPGAs and Space System Manager Products** *Presenter: Mr. O'NEILL, Ken (Microsemi)* This presentation will provide an overview of key enabling technologies addressing the increasing demands for reduced size, weight and power (SWAP) and enhanced signal processing throughput in next generation space systems, without sacrificing reliability. RTG4 is Microsemi's next generation FPGA family for radiation environments using a 65nm low-power flash process, which is immune to changes in configuration due to radiation effects. We will provide an overview of the features and performance of RTG4 FPGAs, and discuss availability of development software, devices and systems for prototyping, and qualified flight parts. We also will provide an overview of the features, benefits and availability schedule of Microsemi's Space System Manager products, which will provide significant improvements in size, weight and power in satellite telemetry and power control applications.
10:00	**Xilinx Space Grade Packaging & Development Updates** *Presenter: Mr. ELFTMANN, Daniel (Xilinx)* Xilinx has been producing Space grade Field Programmable Gate Array (FPGA) with flip chip ceramic column grid array packages since 2008 with its Virtex-4 FPGA family, adding Virtex-5 in 2011. This type of package is not well understood by the space community, and the JEDEC JC-13 participants and DLA-LM spent the past several years to develop the class Y Non-Hermetic Ceramic Packaging and released it in MIL-PRF-38535, revision K. This presentation will describe the construction of the Non-Hermetic Ceramic Flip Chip Column Grid Array package, its unique characteristics, advantages, and limitations. In addition, descriptions will be provided on recent package modification and assembly site change, plus the associated qualification requirement and current progress.

Networking Coffee Break sponsored by Thales Communications & Security (10:40 – 11:10)

Session: Industry Experiences (11:10 – 13:10)
Chair: *Mr. PRESSECQ, Francis (CNES)*

11:10	**Design experience and verification methods using the latest Microsemi RTAX FPGAs** *Presenter: Mr. RIED, Ottmar (Airbus DS GmbH)* In Airbus DS there is an extensive usage of Microsemi RTAX devices. Recently also the RTAX4000 FPGA has been introduced for a new project. The complexity of these type of devices have increased two fold: - number of gate capacity, meaning higher complexity of the function - number of pins, meaning higher complexity for assembly or repair As a consequence potential late modifications, e.g. due to a bug fix, especially after box closer, are getting more and more costly, and therefore a strict design and verification process and, moreover, new verification methods need to be employed. These are in particular: - Formal Verification methods - Verification using emulation hardware The presentation highlights the challenges and achievements of using Microsemi RTAX devices at Airbus DS and it describes the new verification methods employed.

	11:40	***General use of FPGAs in Thales Alenia Space*** *Presenter: Mr. GRIMONET, Gregory (Thales Alenia Space)* Thales Alenia Space uses for several years FPGAs from various vendors which are chosen depending on their size, their performances and the application using it. This presentation will show the FPGAs used in TAS and how they are chosen. Moreover a concrete example will be developed.
	12:10	**FPGA in SODERN recent projects for space applications** *Presenter: Mr. POURRIER, Christophe (SODERN)* SODERN has recently used two different FPGA for earth observation missions. One ATMEL AT40K is embedded in the BSA sub-assembly of ATLID instrument for the EarthCARE satellite. It carries the whole digital functions that drive a 2-axis pointing mechanism. Commands and telemetries are transmitted through one serial link on request of the host processor. One MICROSEMI PROASIC3 is embedded in the camera of TARANIS instrument. It drives 2 CCD sensors and delivers digital video images. One serial link is used to upload control data and parameters for the CCD and the analog chains, and one parallel link is used to transfer digital video data in streaming. This presentation will bring a succinct description of the FPGA designs (theirs functions, frequencies, resources), a topic on the advantage of programmability that we have put forward, the advantages and drawbacks we faced.
	12:40	**SRAM-based FPGAS for Space Applications: Current Projects @INAF** *Presenter: ALDERIGHI, Monica (INAF)* The talk illustrates the main features of two ESA projects that are currently on-going at INAF: FLIPPER 2 and Hi-Rel COTS based Computers for on board systems. FLIPPER 2 represents the second release of the fault injection system for Xilinx SRAM-based FPGAs, developed by INAF. With respect to the previous release, it includes a DUT board specifically designed for Virtex 4 devices, and features an Ethernet link at 1 Gbit/s towards the PC and a DDR2 SODIM, replacing the previous USB connection and board memory chips respectively. The talk summarizes the new implemented functionalities and presents the results of some fault injection campaigns on two sample circuits provided by ESA. Concerning the Hi-Rel COTS based Computers for on board systems project, it is a project in collaboration with Thales Alenia Space Italia (Prime), Politecnico di Torino, INAF, Universita' di Roma Tor Vergata, and Sanitas EG s.r.l. The objective of the project is to study and design on-board computing systems based on "Commercial Off-The-Shelf" components for future missions of the Agency. COTS components include processors, FPGAs and memories. INAF involvement has concerned the selection of and use of FPGA devices and the definition of the EGSE. The talk briefly describes the activities performed and the results achieved so far.

Networking Luncheon (13:10 – 14:10)

Session: Design for Space Applications: Fault Tolerance Methodologies (14:10 – 14:40)
Chair: *Mr. DANGLA, David (CNES)*

	14:10	**An Orbit-specific Fault-injector to Assess Fault-mitigation Strategies in Space FPGAs** *Presenter: Dr. BELTRAME, Giovanni (Polytechnique Montreal)* Particle and ionizing radiation can alter and severely disrupt the normal behavior of electronics, and lead to their premature failure. For this reason, computing systems for space applications have to be designed using methodologies to mitigate such issues. Field Programmable Gate Arrays (FPGAs) provided with reconfiguration capabilities can facilitate the implementation of fault-mitigation methodologies, and allow the use of fault-injector IP cores, which play an important role in the validation of fault protection strategies. In this work, we describe the implementation of a particular fault-injector that, given a target orbit, can simulate transient faults induced by particle radiation at a rate consistent with the characteristics of that portion of space. This fault-injector comprises three different models that can be found in literature, and it has been inspired by previous research in the domain. We also suggest how our tool can be used to validate a smart fault-mitigation technique, based on the mathematical framework known as hidden Markov models, exploiting reconfiguration and spare resources on FPGAs.

Session: Radiation Testing (14:40 – 15:55)
Chair: *Mr. POIVEY, Christian (ESA), Mrs. FERLET-CAVROIS, Véronique (ESA)*

14:40	**Overview of the XRTC Single-Event Test Results on the Xilinx 7-Series FPGAs** *Presenter: Mr. SWIFT, Gary (Swift Engineering and Radiation Services, LLC)* Since September 2013, the Xilinx Radiation Test Consortium collectively and individual members have been subjecting the Kintex-7, Artix-7, and Zynq devices to particle beam testing. Basic upset characteristics of configuration and block RAM and user flip-flops have been measured and clusters of upsets were observed. Additionally, an unusual latchup-like, but non-destructive phenomenon of current steps was observed in the Vaux power rail.
15:25	**Results of Heavy-Ion Broad and Micro Beam Testing of Flash-Based FPGAs** *Presenter: Mr. EVANS, Adrian (IROC Technologies)* The first part of the presentation consists of an in-depth study of single event transients (SETs) in MicroSemi ProASIC3L FPGAs. The devices were tested at the Heavy-ion Irradiation Facility (HIF) at Louvain-La-Neuve, Belgium. Several combinatorial VersaTile configurations were studied in order to evaluate the effect of logic function and input state on SET sensitivity. The effect of temperature and voltage was also studied. A novel detector circuit was used to perform accurate and calibrated, on-chip measurement of the SET pulse width. Using this detector, pulse broadening was studied and shown to be quite significant for positive (0->1->0) transients. The study also investigated the effect of SETs in several typical complex combinatorial circuits (e.g. adders, state-machines, ..). The second part of the presentation consists of a study of the sensitivity of the embedded RAM (BRAM), flip-flops and the PLL in the same ProASIC3L devices. This study was performed using a heavy-ion micro-beam at the GSI facility at Darmstadt, Germany where individual ions can be targeted at specific locations in the device with a spatial resolution of better than 1µm. Spatial sensitivity maps were created for the structures being tested and in this way the physical to logical decoding of the BRAMs was determined and the sensitive regions of the PLLs were identified. In addition, limited results about permanent effects will be presented. Specifically, several of the devices that were tested could not be re-programmed after the exposure to heavy-ions. In some cases, these permanent effects could be reversed through annealing while other devices did not recover. Taken together, these results provide significant insight into the suitability of ProASIC3L devices for space applications.

Networking Coffee Break sponsored by Thales Communications & Security (15:55 – 16:25)

Session: Radiation Testing (16:25 – 16:55)
Chair: *Mr. POIVEY, Christian (ESA), Mrs. FERLET-CAVROIS, Véronique (ESA)*

16:25	**Single Event Upset Characterization of Commercial Grade SRAM and FLASH-based Field Programmable Gate Array Using Proton Irradiation** *Presenter: VAŇÁT, Tomáš; POSPÍŠIL, Jan (Nuclear Physics Institute of the ASCR)* ALICE experiment at LHC collider in CERN laboratory in Geneva is preparing the upgrade of inner tracking system based on ~25 . 10^9 silicon pixel sensors with envisaged number of data links reaching 1000. Due to expected large number of FPGAs, only commercial grade FPGA can be considered. FPGA should have the reliable performance up to the expected lifetime total ionization dose of 10 krad. These requirements call for dedicated FPGA selection procedure. The cyclotron in Nuclear Physics Institute in Rez near Prague with proton beam energies up to 35 MeV and broad range of beam intensities is used to measure SEU probability as a function of proton beam flux, dose, beam energy and FPGA clock frequency. Precise dosimetry is based on ionization chamber cross-calibrated with Medipix type device. The measurements will be used for setting up a calibrated fault injection model of a particular FPGA, which will be used for simulation of various designs foreseen for this FPGA without the need of testing them each individually in radiation environment.

Session: Handbooks (16:55 – 17:50)
Chair: *Mr. MERODIO CODINACHS, David (ESA)*

16:55	**VHDL Best Practices and Design Principles for FPGA /ASIC** *Presenter: Mr. LIABEUF Gabriel; Mr. MANNI Florent (CNES)* FPGA (and/or ASIC) are becoming the key element in the Electronic equipment. Nowadays, the possibilities and the resources offered by these components allow to develop more and more complex systems. To cope with such technical challenges, designers have developed methodologies and rules specific to VHDL to reduce risk of failure. But, most of the time, those methodologies and knowledge are not public. CNES started in 2014 an activity to establish a VHDL Design guideline handbook document which will be public, in collaboration with our partners in France and ESA.
17:20	**Introduction to the up-coming new ECSS Handbook on "Techniques for Radiation Effects Mitigation in ASICs and FPGAs"** *Presenter: Mr. FERNANDEZ LEON, Agustin (ESA)* After the completion in 2012 of the first draft of the ECSS–Q-HB-60-02 handbook through an ESA contract with TIMA(F), an ECSS Working Group of space IC experts was created in 2013 to revise and improve the contents of this document. The WG is working in order to release a final draft in March 2015 for ECSS public review. Then, after receiving and implementing the final suggestions, it should finally be released as a new ECSS Handbook before the end of 2015. This handbook compiles a list of the most frequently used / best known mitigation techniques against radiation effects in ASICs and FPGAs. It is written with multiple and different users in mind: ASIC and FPGA designers who are new to space, but also space IC designers who want further advise, engineers involved in the creation or use of rad-hard IC library cells, IC layouts, space SoC designers (digital, analogue or mixed-signal), electronic-system and SW engineers who may also want or need to add mitigation outside the chip, customers of the developers/vendors of the mitigated ICs using the handbook as a reference to assess what techniques are used or not, etc. The talk will summarise the history, goals, general structure and present status of the handbook and will put the focus on the techniques that can be applied to FPGAs.

Wrap up and Open discussion (17:50 - 18:10)
Presenter: Mr. DANGLA, David (CNES); Mr. MERODIO CODINACHS, David (ESA)

Thursday 18 September 2014

SEFUW Intro – Opening Remarks (08:50 - 09:00)
Presenter: Mr. DANGLA, David (CNES); Mr. MERODIO CODINACHS, David (ESA)

Session: FPGA/CAD Vendors (09:00 – 10:00)
Chair: *Mr. POUPAERT, Jelle (ESA)*

09:00	**Automated techniques for Building-in High Reliability and debugging your FPGA design** *Presenter: Mr. MCMILLAN, Frank (Synopsys)* There is a need for electronic systems to operate with high-reliability and high-availability in the face of radiation-induced "soft errors". The need for high-reliability and high-availability electronic systems has now expanded to include many applications including communications infrastructure, industrial automation, control and medical devices but these soft errors are still of particular concern when they occur in semiconductors that are deployed in military and aerospace systems. This presentation introduces design techniques included within Synplify Premier FPGA design tools that can be used to create circuitry that automatically detects and flags these errors, and then allows FPGA based systems to recover from them so that they continue to work reliably.

Session: Industry Experiences (10:00 – 10:45)
Chair: *Mr. POUPAERT, Jelle (ESA)*

10:00	**EREMS Feedback about flight FPGA development** *Presenter: Mr. SARRERE, Rémi, Ms. ZAOUCHE, Sandrine (EREMS)* EREMS designs FPGAs according to a development flow which contains the following steps: final target selection, prototypes realisations, VHDL design including synthesis, place and route, performance analysis and finally component programming. The presentation outlines EREMS FPGA feedback based on space projects examples like CARMEN, PVL, TARANIS and CPUGEN. These missions are interesting to point out because they contain substantial designs relied on a range of FPGA targets: Microsemi RTSX and RTAX series, and ATMEL ATF series.
10:30	**Algorithm implementation on ATF280 and CPUGEN board** *Presenter: Mr. PERRAUD, Laurent (CNES)*

Networking Coffee Break sponsored by Thales Communications & Security (10:45 – 11:10)

Session: Design for Space Applications: Fault Tolerance Methodologies (11:10 – 12:40)
Chair: *Mr. POUPAERT, Jelle (ESA)*

11:10	**BRAM Radiation Sensor for a Self-Adaptive SEU Mitigation** *Presenter: Mr. GLEIN, Robért (Friedrich-Alexander-Universität Erlangen-Nürnberg)* In order to design a reliable FPGA system as a satellite On-Board Processor, firmware designers have to take Single Event Effects into account. Mitigation schemes (Triple Modular Redundancy, Algorithm-Based Fault Tolerance, ...) ease the consequences of this effects. The main disadvantages of these mitigation schemes in FPGAs are resource overhead and additional path delay, depended on the type of mitigation. We present a concept that only uses mitigation schemes when they are needed (e.g. during solar flares). With a self-adaptive mitigation enabled by a Block RAM radiation sensor inside the FPGA we apply an optimal redundancy at runtime. Dynamic partial reconfiguration is used here to reconfigure areas of the FPGA in dependence of current and changing radiation levels. More precisely, the idea is to trigger a mitigation scheme such as Dual Modular Redundancy or Triple Modular Redundancy in response to a continuously monitored Single Event Upset rate measured inside the on-chip memories itself, e.g., any subset (even used) internal Block RAMs. Depending on the current radiation level the FPGA is configured with the appropriate redundancy at runtime. In our case study, we show that we can avoid the resource overhead of a mitigation scheme over 90 % of the time (no flare condition) in a Geostationary Earth Orbit. Our work is a part of the In-Orbit Verification of

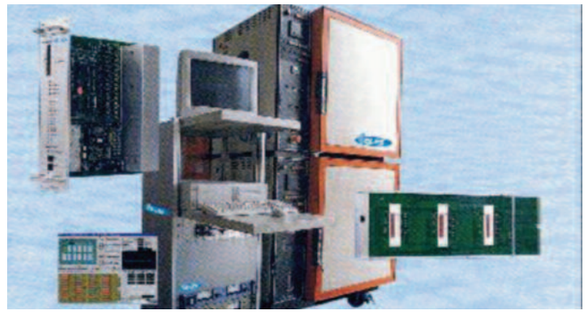
		the Heinrich Hertz communication satellite.
	11:40	**ESTEC experience for Flash-based FPGAs in Space: design and verification guidelines for critical applications** *Presenter: Mr. FURANO, Gianluca (ESA)* ESA path towards high capacity Flash-based FPGA started few years ago with large number of independent radiation tests in dynamic mode to compare their behaviour with established one-time-programmable antifuse-based solutions. Thanks to radhard by-design (RHBD) techniques and specific validation procedures, those devices can be made at least as resilient with respect to Single Event Upsets (SEU) as the antifuse. This paper will show how the grade of reliability is dependent on the fault-tolerant techniques applied to the logic and the expected performances and design overheads of the logic itself. The definition of the target envirioments, design margins and trade-offs for use of RHBD techniques in space-borne Flash FPGAs as well as the Single Event Upsets mitigation techniques necessary will be presented. A specific tailoring for Flash-based FPGAs for the standard development flow for space-grade designs will be proposed, and the advantages with respect to development risk mitigation discussed. If correctly managed, the overheads inferred by RHBD techniques and controlled development flow instead of becoming an additional design hurdle, may allow the exploit of the greater flexibility and performances of Flash FPGAs with respect to antifuse.
	12:10	***Static Design-Dependent SEE rates on SRAM-based FPGAs: a designer flow*** *Presenter*: *Mr. MERODIO CODINACHS, David (ESA)* The use of SRAM-based FPGAs in space equipment is growing. Their radiation-hardness needs to be assessed for the final application (i.e. design) that is implemented in the FPGA device. The talk proposes an approach for FPGA designers to predict the SEE rates during the design activities. The first step addresses the computation of the static SEE rates of each architectural block of the FPGA device with the environment information of the target mission. This step follows well-known procedures based on SEE characterization by radiation testing and the use of CREME96. The second step focuses on the FPGA application-specific calculation. In this part we propose the combination of different tools to help the FPGA developer compute the final SEE rate depending on the design, identifying the critical bits in the FPGA Configuration Memory, user Flip-Flops and the Internal RAM. This helps to iterate and optimise the design taking into account not only parameters as area, speed and power consumption; but also SEE rates.

Concluding remarks and closure (12:40 - 13:00)
Presenter: Mr. DANGLA, David (CNES); Mr. MERODIO CODINACHS, David (ESA)

Reliability testing

Reliability tests are used to eliminate newly emerging problems and assess product strength and operational life expectancy:

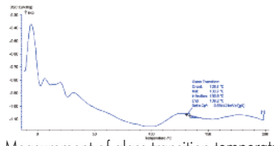
- Accelerated aging testing, thermal cycle testing, highly accelerated stress testing, product consistency testing, damp heat testing.
- Burn-in testing, endurance testing, static/dynamic life testing.



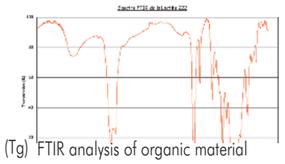
Contamination/pollution analysis

The CEL laboratory has the facilities to analyse all types of organic contaminants/polluants.

- Characterisation of organic materials
- Analytical chemistry techniques
- Thermogravimetric analysis
- Outgassing of organic materials



Measurement of glass transition temperature (Tg)



FTIR analysis of organic material of substrate

Our molecular analysis system comprises:

- a thermal desorption unit
- a gas chromatograph
- a mass spectrometer

The CEL laboratory provides customers with full support for various types of studies:

- *Application of the RoHS Directive and resolution of issues related to lead-free soldering*
- *Electrical diagnostic and defect location for advanced technologies (nanotechnologies, etc.)*
- *FIB design editing for copper and aluminium technologies*
- *Back-end and front-end sample preparation*

THALES COMMUNICATIONS & SECURITY S.A.S.
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COMMUNICATIONS & SECURITY

CEL

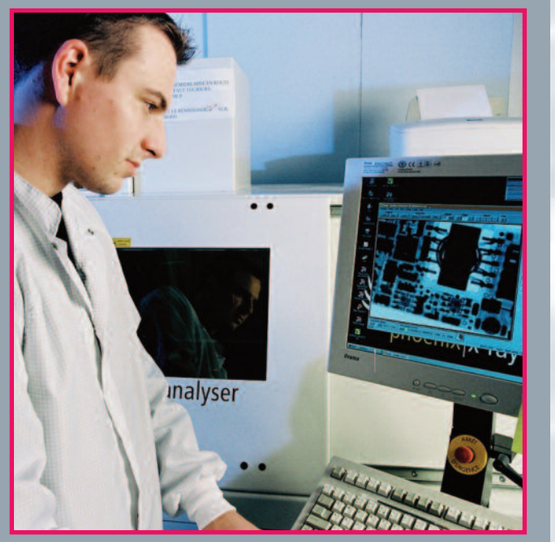
Component Engineering Laboratory

CEL

Failure analysis, security and reliability of electronic components

Thales has expanded its capabilities in electronic component security and reliability with the CEL (Component Engineering Laboratory). CEL offers a complete range of services including design support, technological analysis, failure analysis, electrical characterisation, reliability testing, contamination/pollution analysis and engineering. It also has facilities to assess the behaviour of electronic components under extreme conditions.

The CEL laboratory has know-how and experience spanning more than fifteen years. CEL operates in close partnership with CNES, the French space agency and shares a 700-sqm laboratory in Toulouse.



- Analysis (technological, failure, materials, contamination, etc.)
- Defect localisation (static/dynamic mode)
- Electronic component engineering
- Electrical characterisation, electrostatic discharge, latch-up testing
- FIB reconfiguration - FIB edit
- Counterfeiting

WHAT WE DO

As CEL, the laboratory advises its customers and provides effective support for all types of problems related to electronic components, materials and contamination/pollution. We serve customers in a broad variety of sectors, including defence, aviation, space, transport, energy, component design/manufacturer and consumer products.

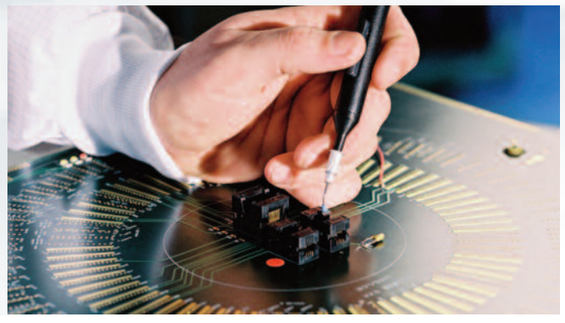
CEL works closely with Thales Research and Technology to offer specific services in the area of COTS component qualification. The laboratory is one of Europe's leading electronic component management facilities.

Electrical characterisation

A variety of techniques are used to characterise electronic components.
Applications include:

Uprating, second source qualification, obsolescence management, failure validation.

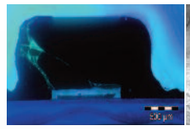
Electrical characterisation of passive, discrete, digital, hybrid and analogue components. Screening, uprating, electrostatic discharge testing, latch-up testing.



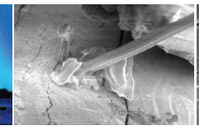
Technological/failure analysis

Technological analysis involves detailed assessment of component technologies with respect to stated specifications and latest industry standards.

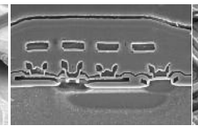
Failure analysis is used to confirm and localise physical defects to help customers to determine the root causes of defects.



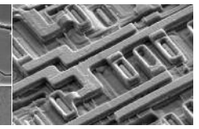
Analysis of passive components



Whiskers analysis



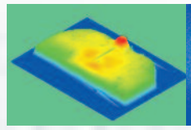
Front-end analysis Observation of integrated circuit structure by microsection



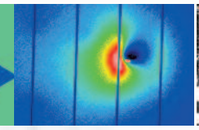
Front-end analysis Destratification of integrated circuits

Defect localisation

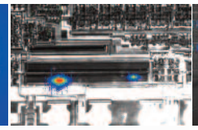
Defect localisation techniques are an integral part of failure analysis.



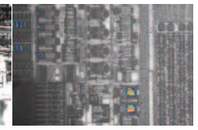
Location by infrared camera



Phemos 1000 emission microscope



Static/dynamic location with Phemos 1000



DEFECT LOCALISATION INSTRUMENTS

- Phemos 1000 light emission microscope
- Tri phemos
- Meridian

DEFECT LOCALISATION TECHNIQUES

- Thermal laser stimulation (TLS) - OBIRCH (Optical Beam Induced Resistance Change)
- Emission microscopy (EMMI)
- Dynamic laser stimulation (DLS)

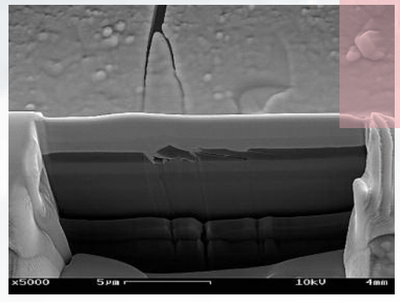
CEL has developed specific back-end preparation methodologies applicable to these defect location techniques. It is one of the only laboratories equipped with these advanced techniques.

FIB reconfiguration

Focused ion beam (FIB) technologies provide a powerful design editing tool to considerably reduce new integrated circuit design time and, as a result, time to market. FIB technologies also support failure analysis.

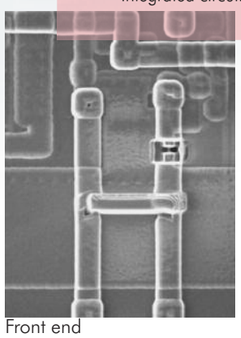
CEL has two FIB systems:

- Credence OptiFIB
- FEI Dual Beam

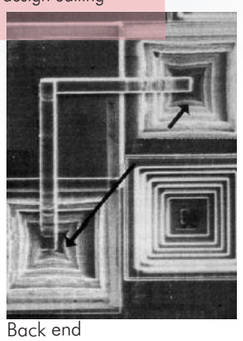


FIB microsection for observing highly localised defects

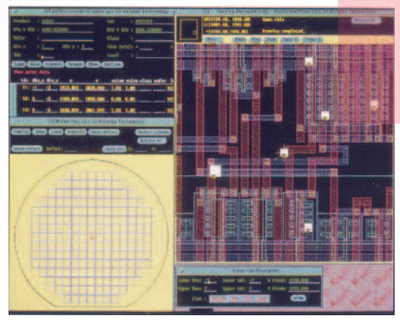
Integrated circuit design editing



Front end



Back end



Editing of integrated circuit layouts to aid navigation

SOCIAL DINNER – SEFUW 2014

SEFUW dinner will take place on Tuesday night (September 16th) in
"Iets Anders in Bistro Bardot" at 8pm

Price: 42.5 EUR
The price includes a 3 course menu and drink arrangement.
The restaurant is situated in **Pickeplein 4 -2202 CK Noordwijk**.

MENU

French onion soup with a cheese crouton
or
Beef carpaccio with tomato salsa and Parmesan cheese
or
Goat cheese salad with walnuts, raisins and vinaigrette

* *

Grilled salmon served with tartare sauce and salad
or
Steak and brisket with Madeira sauce and grilled vegetables
or
Vegetarian pasta with dried tomatoes and grilled green asparagus

* *

Crèpes Suzette with Grand Marnier/orange sauce and vanilla ice cream
or
French cheese platter