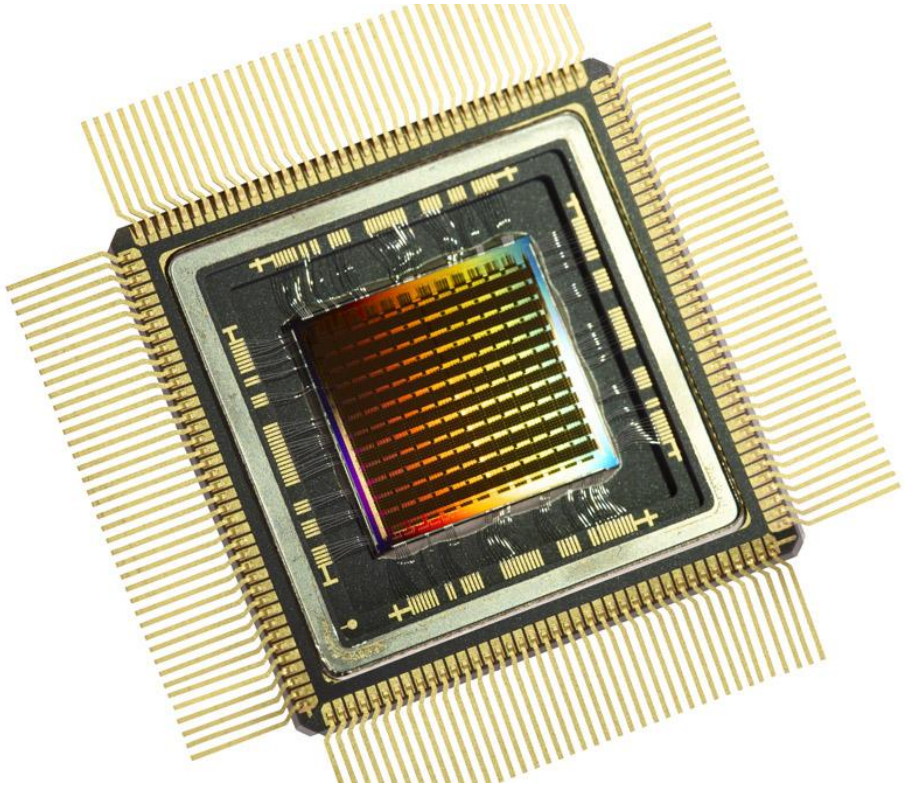
AT40K FPGAs Platform For SPACE APPLICATIONS



Tools & Environment

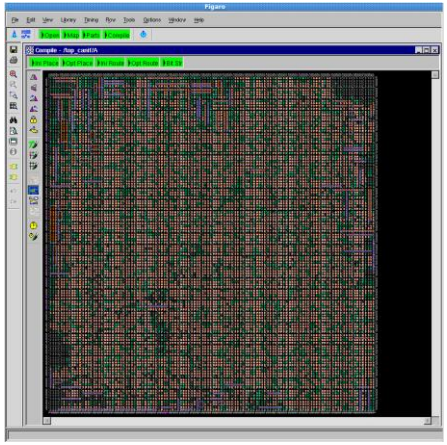
2014, Sept.

AT40K SYNTHESIS, PLACE & ROUTE TOOLING

SYNTHESIS

MENTOR Precision

- VHDL / Verilog entry
- Automatic IDS Macro detection and mapping



PLACE & ROUTE

ATMEL IDS: Automated Place & Route

- STA
- Power Estimator
- VHDL / Verilog netlist export with SDF back-annotation
- Bitstream generation

What's new since last SEFUW ?

AT40K SYNTHESIS, PLACE & ROUTE TOOLING

Release Overview

Release	IDS	Precision	date
3.2	9.1.3	2012b	November 2012
3.3	9.2.1	2012b	March 2013
3.4	9.3.2	2013b	June 2014
3.5	9.3.3	2013b	August 2014
3.6	**9.3.4**	**2014b**	**Septembre 2014**
3.7	9.3.5	2014b	Q1-2015 (TBC)

AT40K SYNTHESIS, PLACE & ROUTE TOOLING

Precision Major Improvements

- ***PCS – RSBUF/GCLKBUF Management***
  - RSBUF is inserted on the external reset port having the highest reset fanout, unless an internal reset signal exists having a higher reset fanout. In this case no RSBUF insertion is performed on external reset
  - User-specified PAD attributes have the highest priority.

- ***PCS - RAMDSYNC DRC rules***

  Precision respects new DRC rule introduced by Atmel for RAMDSYNC instances: RAMDSYNC instances shall not have unconnected output ports. Unconnected output ports will be connected to unconnected input ports of the same instance whenever possible.

- ***PCS - ROM memory corruption***

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AT40K SYNTHESIS, PLACE & ROUTE TOOLING

Precision Major Improvements

- ***PCS - FSM optimization***
  The FSM optimization is an issue in precision, to avoid none functional design we recommend to use the following option
  - setup_design -advanced_fsm_optimization=false
  - setup_design -reencode_fsm_outputs=false

- ***PCS -*** **Verilog and VHDL netlist for Post- synthesis simulation and formal proof run.**

- ***PCS – Windows 7 support***

AT40K SYNTHESIS, PLACE & ROUTE TOOLING

IDS Major Improvements – Timing Analysis (STA)

- ***IDS - Multicycle Path Management***

  A new command for management of multicycle path is being integrated in IDS STA engine. This should be used to relax the timings on paths taking more than one cycle to propagate a signal to its end point.

- ***IDS – False Path constraints***

  The integration of the false path management allows to remove the false paths from the timing report or to impose constraints to the STA monitor.

- ***IDS – Derive Clock domains analysis***

  STA analysis can be performed on any of the clock domain present in the design, including derived clock.

- ***IDS – STA reports***

  Whatever the presence or not of a timing violation, IDS STA engine always reports the worst path timing of the design.

AT40K SYNTHESIS, PLACE & ROUTE TOOLING

IDS Major Improvements – Design Mapping

- ***IDS – Preserve Cell***
  Property '**preserve_cell**' is supported. The property preserve_cell is recognized by IDS mapper and annotated cell be preserved from being merged

- ***IDS - Global clock routing***
  A new clock option '**Routing On global clock**', in the timing constraints, applicable for main clocks, allow them to be routed on the standard network. Useful when the main clock drives a limited numbers of synchronous elements

AT40K SYNTHESIS, PLACE & ROUTE TOOLING

IDS Major Improvements – Power Computation

- ***IDS – Power Estimation***

A new power computation engine has been developped. It is run from the main menu after place and route: '**Tools->calculate power**'

- It takes into account for each clock domain:
  - the clock frequency
  - the number of flops
  - the switching activity

- A new parameter '**switching activity'** has been added into the clock constraints.

- The LVDS leakage power has been added.

AT40K SYNTHESIS, PLACE & ROUTE TOOLING

IDS Major Improvements – Simulation

- ***IDS – Modelsim Simulation Package***

  The modelsim library package *(verilog + vhdl libraries)* has been upgraded to **modelsim_package_V1.2.0** to ensure the support of
  - **at40kal**: AT40k librairies,
  - **atf280e**: ATF280K librairies – for ATF280, ATF697 and ATFEE560
  - **atfs450**: ATFS450k librairies.

- ***Simulation/Formal proof :***

  A new netlist is published at the end of the synthesis though Precision in order to allow post synthesis simulation. IDS libraries (verilog and VHDL) are made available to make simulation and Formal proof after synthesis.

AT40K SYNTHESIS, PLACE & ROUTE TOOLING

IDS Major Improvements – Devices Support

- ***IDS – Packages***

IDS is updated for support of the up-to-date AT40K family

- ATF280
  - QFP256, QFP352, MCGA472
- ATFS450
  - QFP352
- ATFEE560 (multi chip module with 2x ATF280 and 2x configurators)
  - ATFEE560-top-left
  - ATFEE560-bottom-right
- ATF697FF (multi chip module one ATF697 and one ATF280)
  - QFP352

AT40K SYNTHESIS, PLACE & ROUTE TOOLING

IDS Major Improvements – others

- ***IDS – Windows 7 support***

- ***IDS – Batch Mode***

  Following end-user requests, new commands have been added
  - Timing Analysis – 'run(timingAnalysis)
  - Number of routing optimization run - NbOptRoute=4
  - New variable in the batch file to enable or disable the LPM block generation - MGIBlocks = 'yesAll' | 'noALL'

- ***Measure of Execution run time***

  From SP 3.5/IDS 9.3.3, the exec run time is not only reported in user time but also reported in cpu time:

```
Old   Finished on September 15, 2014 at 12:47:25 PM - Success - Elapsed time 0:10:3

New   Finished on:    September 15, 2014 at 12:47:25 PM
      Status:         Success
      Elapsed time :  Real - 0:10:3,
                      CPU time - 0:8:2
```

AT40K SYNTHESIS, PLACE & ROUTE TOOLING

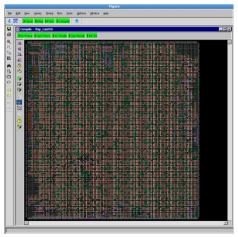
IDS Major Improvements – others

- ***IDS* – Hard Macros flow :**

  A new user hard macro has been integrated to allow the instantiation of pre-placed and pre-routed macros (IP) in the application.

  Pre-place and pre-route is performed by Atmel experts, hence guarantying optimal deterministic size and performances.

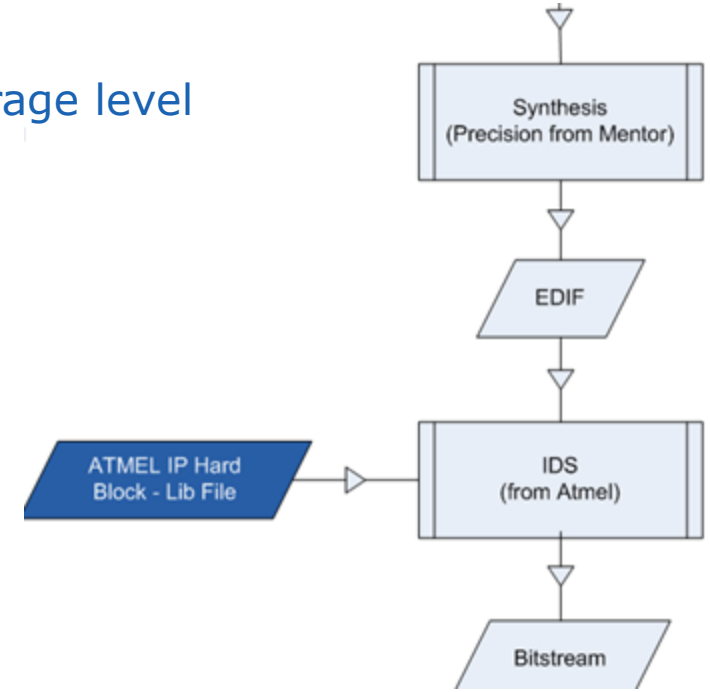
IP's SOLUTIONS



Goal Provide an accurate IP portfolio to get quick and efficient setup on FPGA applications.

IP During Place/Route step with IDS, the user get access to the placed&routed block

- Guaranteed performances
- Simulation files with high coverage level
- Validated on board



Current Development (2013-2014)

- SpaceWire
- 1553
- PCI
- UART

Next developments

- CAN
- SMCS TM/TC
- AVR8

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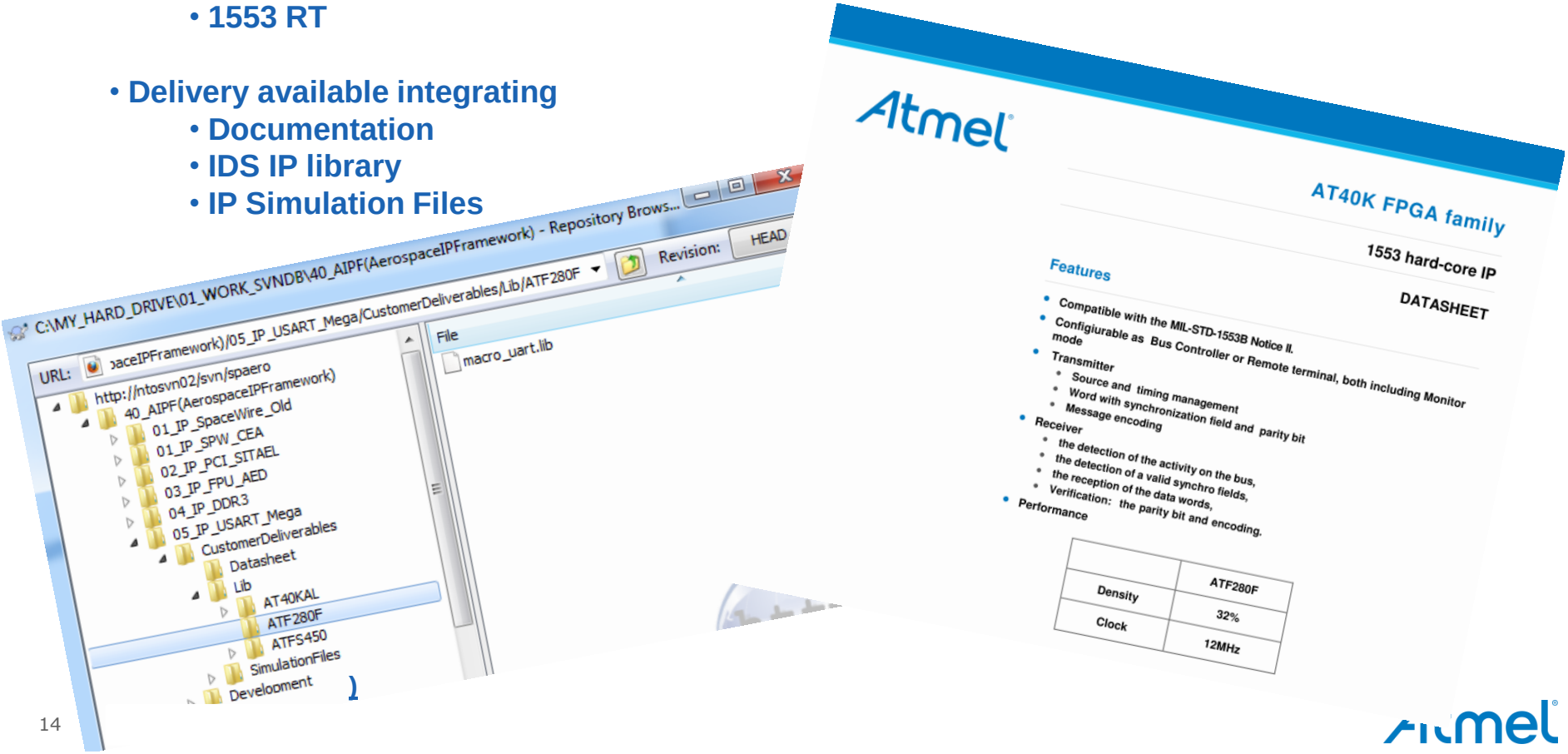
FPGA IP

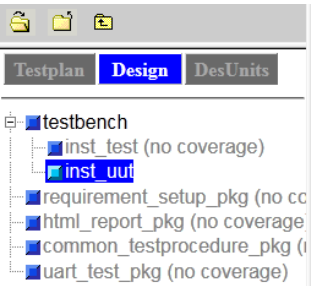
Achievements

- First Ips for application building
  - UART
  - SpaceWire
  - 1553 BC-RT
  - 1553 RT
- Delivery available integrating
  - Documentation
  - IDS IP library
  - IP Simulation Files



FPGA IP - Overview

Quality level



ModelSim Coverage Summary

Scope: /testbench/inst_uut

Local Instance Coverage Details:

Weighted Average:				96.20%
Coverage Type	Bins	Hits	Misses	Coverage (%)
Statement	276	276	0	100.00%
Branch	233	233	0	100.00%
FEC Expression	90	87	3	96.66%
FEC Condition	76	67	9	88.15%

Scope Details:

Instance Path:
/testbench/inst_uut
Design Unit Name:
work.usart
Language:
Verilog
Source File:
../testbench/top_tb.vhd

AT40K FPGA family

UART hard-core IP

DATASHEET

Features

- Full Duplex Operation (Independent Serial Receive and Transmit Registers)
- Asynchronous or Synchronous Operation
- Master or Slave Clocked Synchronous Operation
- High Resolution Baud Rate Generator
- Supports Serial Frames with 5, 6, 7, 8, or 9 Data Bits and 1 or 2 Stop Bits
- Odd or Even Parity Generation and Parity Check .
- Data OverRun Detection
- Framing Error Detection
- Noise Filtering Includes False Start Bit Detection and Digital Low Pass Filter
- Three Separate Interrupts on TX Complete, TX Data Register Empty, and RX Complete
- Double Speed Asynchronous Communication Mode

Performances

	AT40KEL040	ATF280F	ATFS450
Density	23,6%	3,8%	2,4%
Baudrate	2400 to 0.5 bps	2400 to 1M bps	2400 to 1M bps
Clock	1 to 8 MHz	1 to 16MHz	1 to 16MHz

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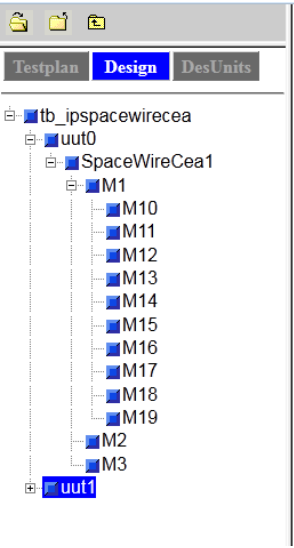
FPGA IP - Overview

AT40K FPGA family

SpaceWire hard-core IP

DATASHEET

Quality level



ModelSim Coverage Summary

Scope: /tb_ipspacewirecea/uut1

Recursive Hierarchical Coverage Details:

Weighted Average:				79.07%
Coverage Type	**Bins**	**Hits**	**Misses**	**Coverage (%)**
Statement	437	401	36	91.76%
Branch	292	256	36	87.67%
FEC Expression	75	54	21	72.00%
FEC Condition	74	42	32	56.75%
FSM State	27	25	2	92.59%
FSM Transition	77	63	14	81.81%

Features

- Low voltage differential signaling (LVDS)
- Data-strobe signal encoding
- Initial operating data signaling rate
- Data & Control Character
- Time-Code to support the distribution of a system time across a network
- Flow Control
- Detection of disconnect, parity and reception error
- Link error recovery
- AutoStart

Performances

	ATF280F	ATFS450
Density	7,1%	4,4%
Clock	25MHz	25MHz

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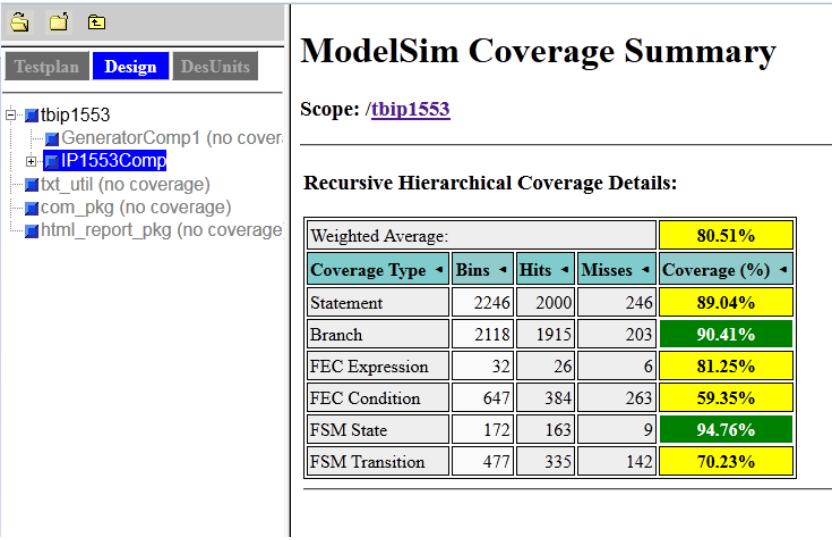
FPGA IP - Overview

Quality level



ModelSim Coverage Summary

Scope: /tbip1553

Recursive Hierarchical Coverage Details:

Weighted Average:				80.51%
Coverage Type	Bins	Hits	Misses	Coverage (%)
Statement	2246	2000	246	89.04%
Branch	2118	1915	203	90.41%
FEC Expression	32	26	6	81.25%
FEC Condition	647	384	263	59.35%
FSM State	172	163	9	94.76%
FSM Transition	477	335	142	70.23%

AT40K FPGA family

1553 hard-core IP

DATASHEET

Features

- Compatible with the MIL-STD-1553B Notice II.
- Configiurable as Bus Controller or Remote terminal, both including Monitor mode
- Transmitter
  - Source and timing management
  - Word with synchronization field and parity bit
  - Message encoding
- Receiver
  - the detection of the activity on the bus,
  - the detection of a valid synchro fields,
  - the reception of the data words,
  - Verification: the parity bit and encoding.

Performances

	ATF280F
Density	32%
Clock	12MHz

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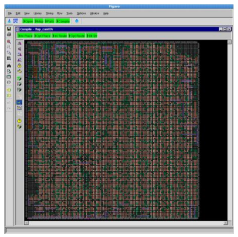
IP's SOLUTIONS



Structured Documentation

A simple HTML interface giving access to specifications and quality information: overview, test summary, test report, requirements report & coverage report

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IP Reports

Component Name : IP_USART_8_Bits

Component Version : V1.1

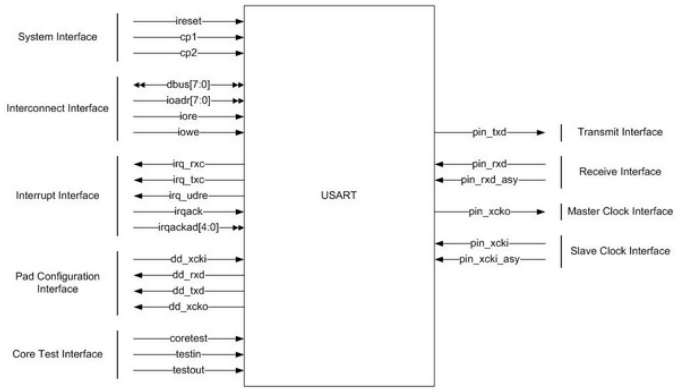
- Overview
- Test Summary
- Test Reports
- Requirements Reports
- Coverage Reports

Architecture Short Description :

STUB Component (AHB master):
Behavior:
- configure the tick timer
- configure the "LOADER_MODEL" to operate
- wait for cfg_start (from testbench) to send a dataflow (data rate depends on tick period)

Timers (APB component):
APB Base Address: 0xF000_0000
Behavior and Registers defined p.111 of AT697F datasheet (include from system_param.vhd)

LOADER_MODEL (AHB and APB component):
APB Base Address: 0xF020_0000 and AHB Base Address: 0xA000_0000
Registers defined in system_param.vhd file (from include)
- "Fifo_Model" module: all the dataflow received to this address is write into Fifo_Model (32 bits wide @ 100 MHz)
- "EXPANDER" module get the data (16 bits wide @ 200 MHz) and push them to the WR_BUFFER
- "WR_BUFFER" module get the data flow and simulate a "FABRIC" write operation
  * concatenate 6*16 bits words into a single 96 bits word
  * emulate a write cycle of 6 periods of 200MHz clock (configurable through LOADER_CFG_REG)



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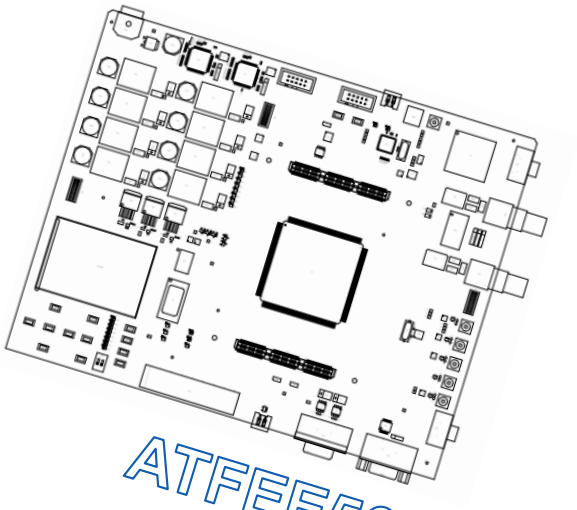
AT40K HARDWARE DEVELOPMENT PLATFORM

For each of the AT40K device, a hardware development platform is provided

Configurator
Programming Tool



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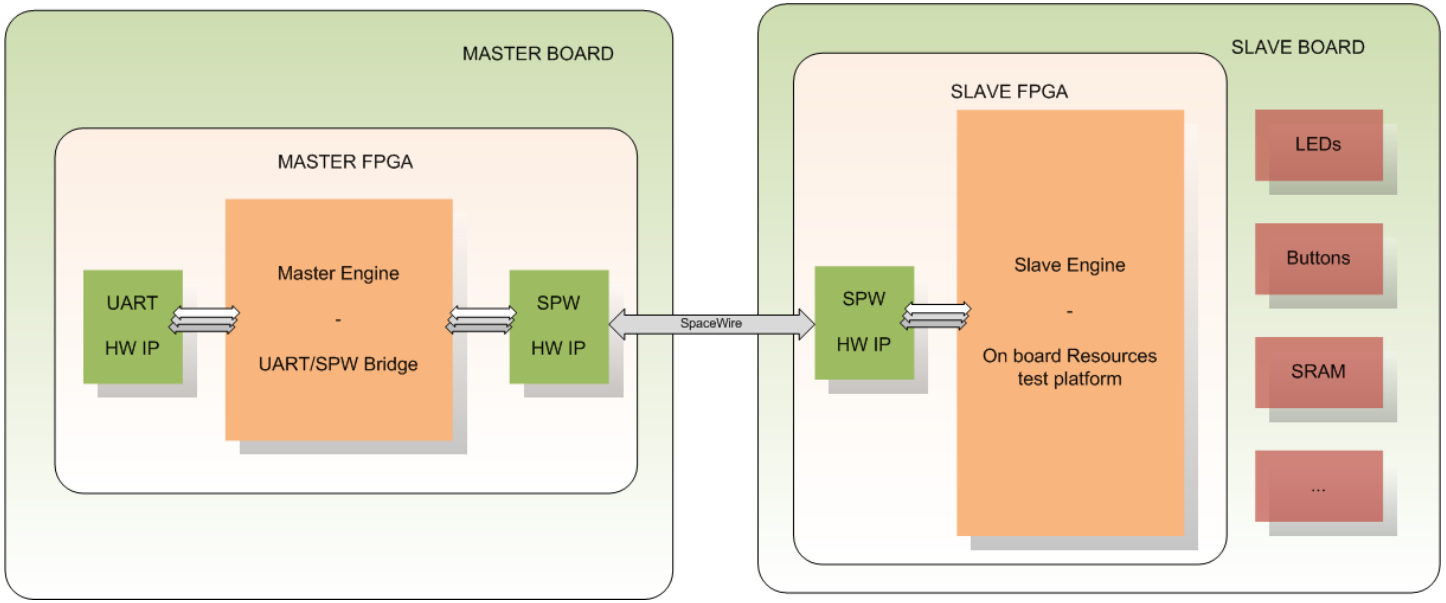
AT40K Demonstration

On the basis of the hardware developed since last SEFUW and the IPs integrated has hard blocks, the demonstration consists in managing the peripherals of an FPGA slave board that communicates with the FPGA master board thorough the space wire link

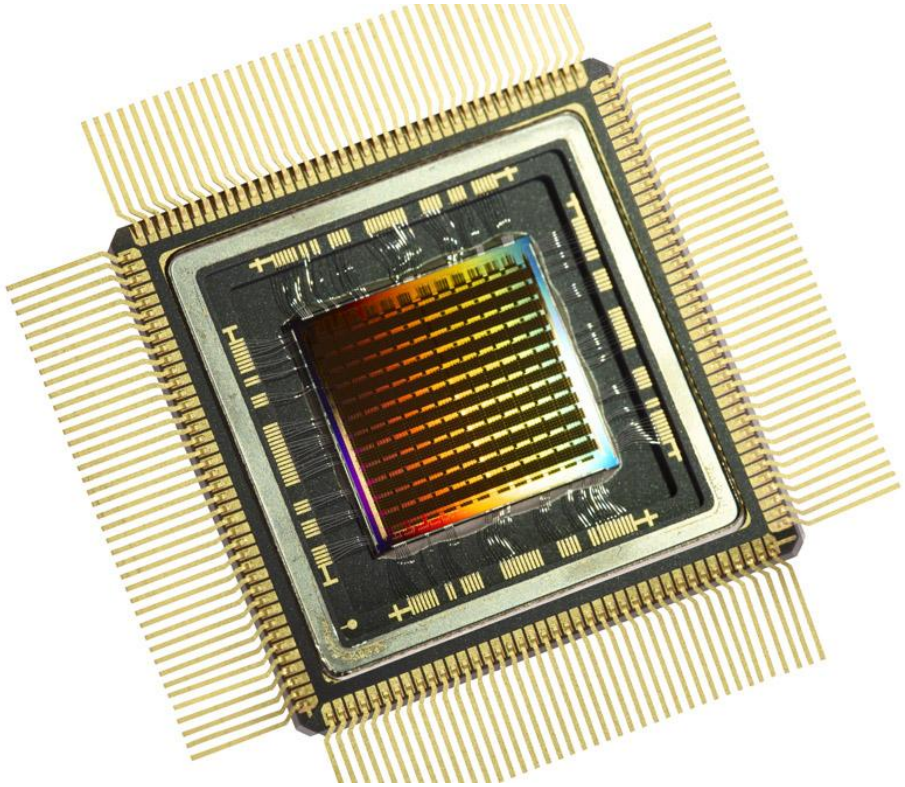
The FPGA master board integrate an uart and a spacewire hard blocks.

The FPGA slave board integrate a spacewire hard blocks.



Welcome to the demonstration Session!!!

AT40K FPGAs Platform For SPACE APPLICATIONS



Backup

2014, Sept.

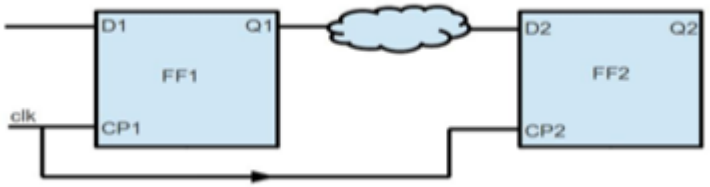
AT40K tooling

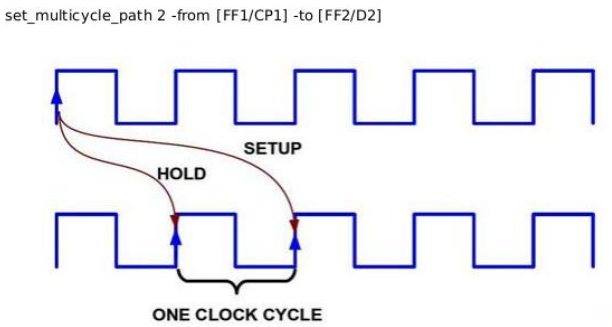
Improvements Continuation

- IDS - Multicycle Path Management

  A new command for management of multicycle path is being integrated in IDS STA engine. This should be used to relax the timings on paths taking more than one cycle to propagate a signal to its end point.

set_multicycle_path
[-setup] [-hold]
[-rise] [-fall]
[-start] [-end]
[-reset_path]
[-from from_list
| -rise_from rise_from_list
| -fall_from fall_from_list]
[-through through_list]*
[-rise_through rise_through_list]*
[-fall_through fall_through_list]*
[-to to_list
| -rise_to rise_to_list
| -fall_to fall_to_list]
path_multiplier





AT40K tooling

Improvements Continuation

Short due to unconnected DOUT ios **:**

- On the silicon the 4 Freeram DOUT pins are driven altogether. If some DOUT pins are not connected, the router considers the wires connected to the free DOUT pins as free and may use them to route an another net and then creates a conflict with the free ram output.

- The new release of IDS checks if some DOUT pins are not connected and in that case issues a fatal error: **All the DOUT ios must be connected** in the edif netlist (these ios can be easily connected in the RTL to the associated free DIN pins).

AT40K tooling

Improvements Continuation

Preserve_cell :

Property preserve_cell in EDIF file will be recognized by IDS mapper and be preserved from being merged

- Precision

set_attribute -design rtl -name preserve_cell -value true -instance {*inst_list*}

- Edif Netlist

(instance *inst_name* (viewRef NETLIST (cellRef *inst_type* (libraryRef *at_library*)))
(property preserve_cell (string "true")))

The preserve_cell property is automatically added for the replicated cells

Cells specified to be preserve by the option '**Options->Mapping->Replicated cells' .** The cells to be preserved can be specified only by suffix patterns that support Smalltalk regular expression syntax. Some suffixes are used by default, they are corresponding to replicated cells.