Public Discussion / AOB

All

Public Discussion

Proposed Discussion Topics

- **SSDP: priorities / schemes for software developments**
- **NGDSP: modified requirements and new IP for next attempt**
- **DSP IP vs. DSP ASIC vs. DSP hard IP in FPGA**
- **Feedback on updated ESA roadmap**
- **AOB**

Public Discussion - SSDP SW

Discussion: SSDP Software Priorities & Concepts

- Problem: available software / DSP libraries for SSDP are much more limited in comparison to what we are used from COTS products

- **Proposal:** pool resources from ESA-funded and other SSDP related activities, provide DSP kernels developed in such activities to community via
- **Implementation:** provide DSP kernels under **ESA OSS license**: Open for ESA member state users, non-infective = can be combined with own software in products.
- **First case:** NGAPP “AlgoLib”, developed by RSA / Univie. **Contractors agreed to provide DSP kernels under ESA OSS license => good example to follow.**
- **Issues to solve:** quality, optimization/performance, documentation => proposed that ESA does that via dedicated contracts.

- **Your opinion ?**

Public Discussion – new NGDSP

Discussion: NGDSP – modified requirements and new IP for next attempt

- **Problem:** COTS IP assessed for NGDSP turned out to be not suitable (ATMEL Diopsis) / not licensable (TI6727)/ not affordable (ADI 21469). Need for high performance floating point DSP continues to exist. Current fix is large / expensive FPGAs and specific ASICs.
- **Consequence of delays:** ECI4 money (600k) was re-allocated to DDR2 IP development (good and bad at the same time), original goal of >1 GFLOP insufficient, new suitable IP needs to be found.
- **New facts:** SSDP development ongoing, RECORE IP matured and hardened, **floating point Xentium IP can be developed with acceptable effort and dedicated activity proposed in TRP for approval at next AC** (issue: Geo-return … **AI**)
- **Proposal / ESA position:** develop floating point Xentium version, incorporate DSP IP in ESA IP portfolio for supporting future developments, proceed with manycore floating point DSP development, taking advantage of the LEONx/SSDP/NGDSP family approach for software and IP
- **Your opinion ?**

Public Discussion – DSP ASIC, IP, hard IP

Discussion: DSP IP vs. DSP ASIC vs. DSP hard IP in FPGA

- At ADCSS 2007 industrial participants voiced desire to have the ESA (NG)DSP IP also available as licensable IP, or IP as part of ESA IP portfolio, available for their own developments
- **SSDP:** DSP IP (including NoC , bridges, SDE) is licensable from RECORE b.v.
- **Proposed FP DSP IP development (AI) with RECORE b.v. is also aiming at incorporation of fixed + floating point DSP IP in ESA IP portfolio (supporting prototyping / TRP work), with defined conditions for support packages and FM development licenses for other projects.**
- **Your opinion ?**
- **Future options: DSP as hard IP in future European large FPGA.** Would allow efficient integration of software programmable backend with very fast data processing frontends (instrumentation, GPS, accelerated specific computations etc.)
- **Your opinion ?**

Public Discussion - Updated ESA DSP RM

	Task Name
1	**MPPB study**
2	**MPPB IP hardening in DARE+**
3	Floating point Xentium DSP development
4	Floating point Xentium DSP IP available
5	
6	**SSDP design, manufacturing & qualification**
7	SSDP prototype chip availability
8	SSDP qualification
9	SSDP FM availability
10	
11	**MPPB/SSDP architecture & SW eval**
12	SSDP IP assessment complete
13	
14	**NGAPP**
15	DPU architectural design based on SSDP available
16	SSDP DPU board development
17	SSDP Software (library / OS) developments
18	SSDP DPU board and SW available
19	
20	**DARE+180nm library development**
21	DARE+ 180nm XD prototype development & evaluation
22	
23	**HPDP**
24	HPDP prototype chip available
25	
26	**DSM 65nm technology development**
27	DSM Phase2.0 / CNES (ESCC eval of lib)
28	DSM Phase2.1 / ESA (incl. initial deployment)
29	DSM Phase2.2 / ESA contract (HSSL IP+char+CAD)
30	DSM Phase3.0 / ESA (submission of C65SPACE to EPPL)
31	DSM Flip Chip / ESA
32	
33	**NGDSP tradeoff study**
34	Manycore NGDSP ASIC pre-development (IP)
35	Manycore NGDSP prototyping
36	Manycore NGDSP qualification
37	Possible space qualified 65nm NGDSP chip availability
38	
39	**HPPDSP COTS computer for D-SRE**
40	HPPDSP breadboard available
41	
42	**Hi-P COTS based computer - Phase 1**
43	Hi-P COTS based computer - Phase 2
44	HI-P COTS based computer availability
45	

New FIP IP development

SSDP HW/ SW devel.

Funding allocated

No funding allocated yet

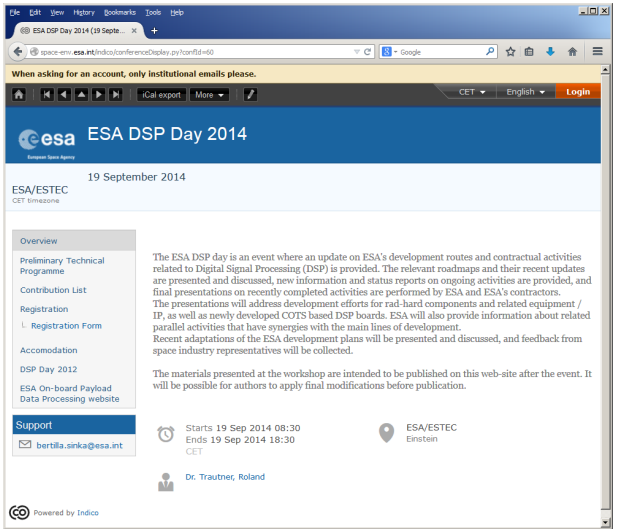
New NGDSP attempt with new IP:
- ECI
- TRP
- GSTP

ESA DSP Day 2014 – The End

Thank You!

FYI the presentations will be posted on the DSP day 2014 website:

http://space-env.esa.int/indico/conferenceDisplay.py?confId=60



ESA & TEC-EDP wish you a good evening & safe return.