DARE+ Application ASIC, Hardened DSP IP and Tools

Gerard Rauwerda, CTO & co-founder
Gerard.Rauwerda@recoresystems.com

RECORE

Recore Systems BV
P.O. Box 77, 7500 AB,
Enschede, The Netherlands
' +31 53 4753 000
7 +31 53 4753 009
info@recoresystems.com
www.recoresystems.com

Multi-core DSP for payload processing

- ESA TRP activities:
  - MPPB
    - Feasibility/benchmark study for next generation multi-core DSP for space applications (Jan ‘09 – Aug ‘12)
  - DARE+
    - Rad.-hard prototyping of MPPB elements in DARE180 (Jul ’11 – Dec ’13)
- ESA NPI activity:
  - Development of methodologies and tools for predictable, real-time LEON/DSP-based embedded systems (2011 – 2013)
    - Performed by Politecnico di Milano (Polimi)
    - Supported by Recore Systems / MPPB
- ESA CTP activity:
  - Scalable Sensor Data Processor (2014-)

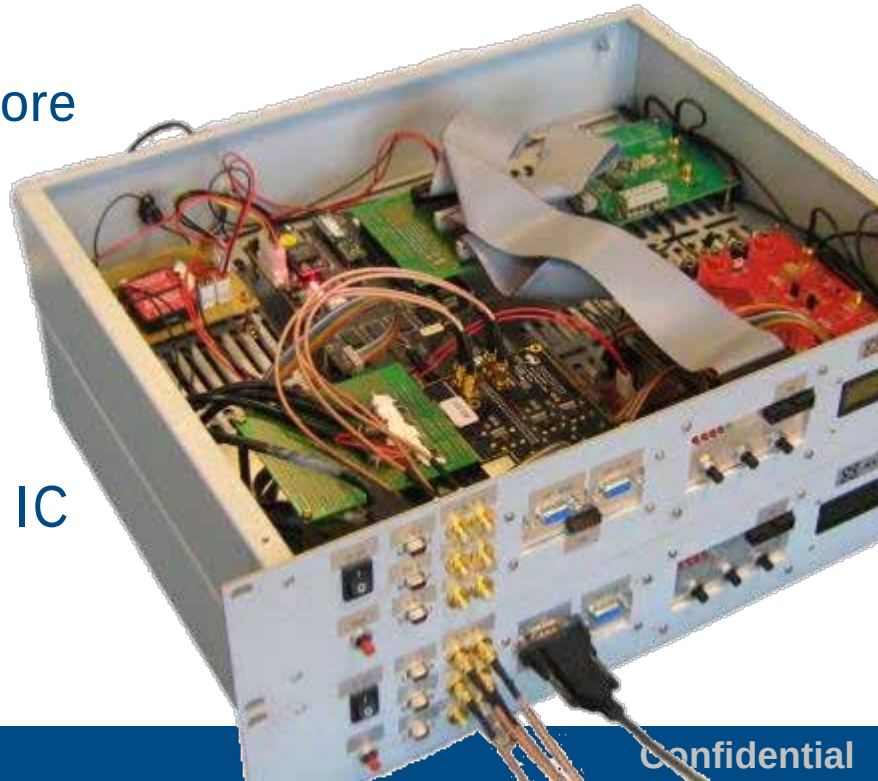
Step-wise approach

- Leave proven concepts alone: GPP subsystem
  - Leon2, SpaceWire, ...
- Test-drive multi-core reliability concept: small fault-tolerant DSP subsystem
  - NoC-based Xentium DSP multi-core
  - Heterogeneous and scalable

Step 1: FPGA prototype

Step 2: Rad.-hard prototype IC

Step 3: Rad.-hard multi-core DSP IC



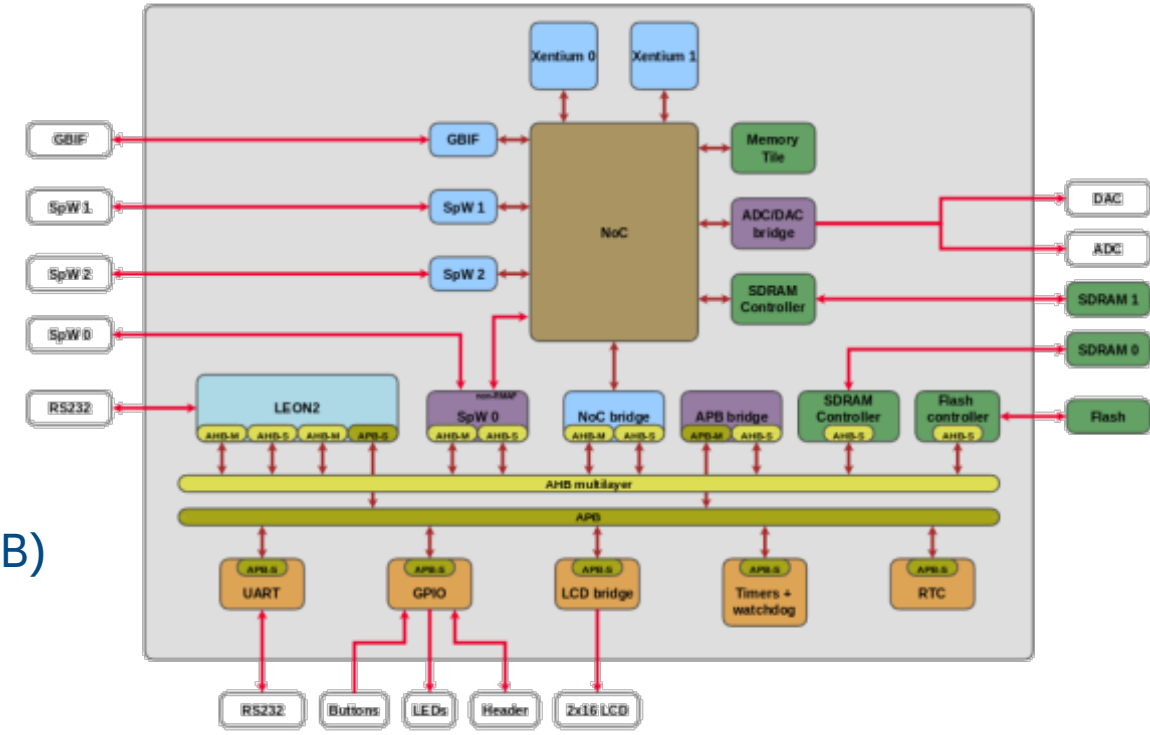
esa

Step 1 - MPPB

FUNCTIONAL PROTOTYPE

MPPB architecture

- Xentium-based DSP subsystem
  - Network-on-Chip (NoC)
  - 2 Xentium DSP core
  - Memory Tile
  - DMA controller
  - High speed interfaces
  - ADC/DAC interfaces
  - DDR
- Leon-based GPP subsystem
  - AMBA Bus system (AHB/APB)
  - SpW RMAP
  - DDR, Flash
  - Standard peripherals

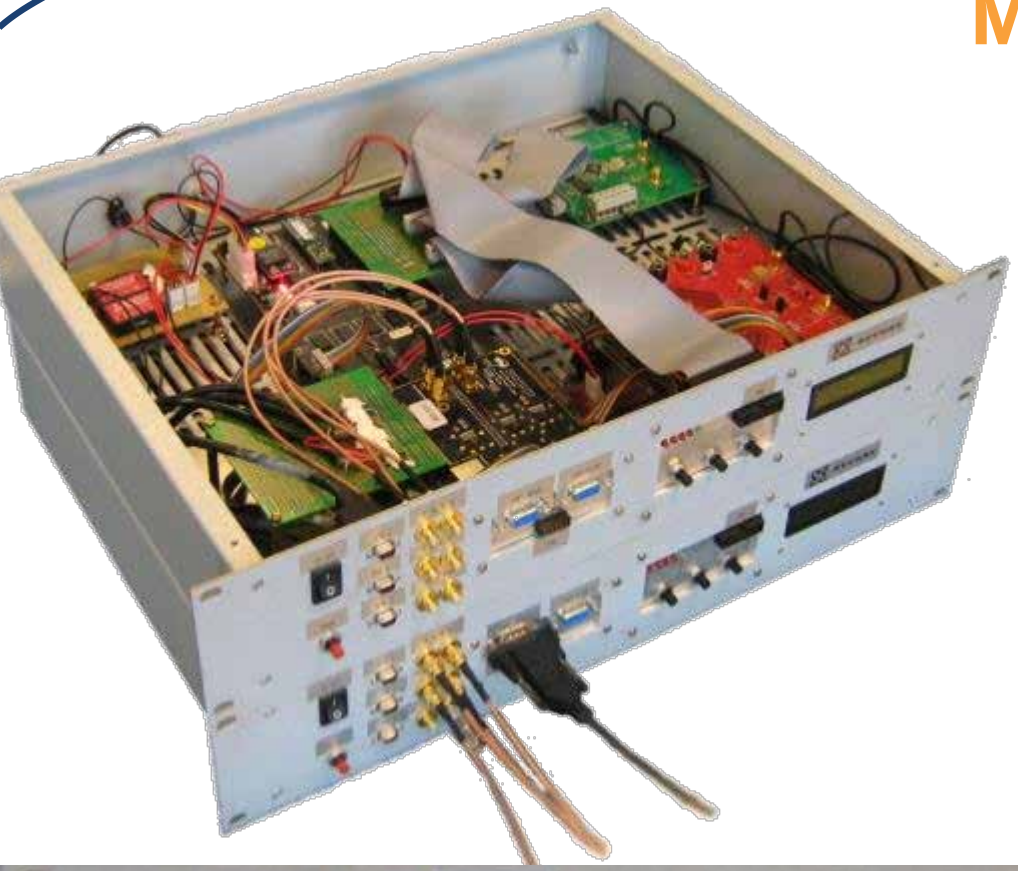


MPPB features
on a Xilinx Virtex-5 FPGA

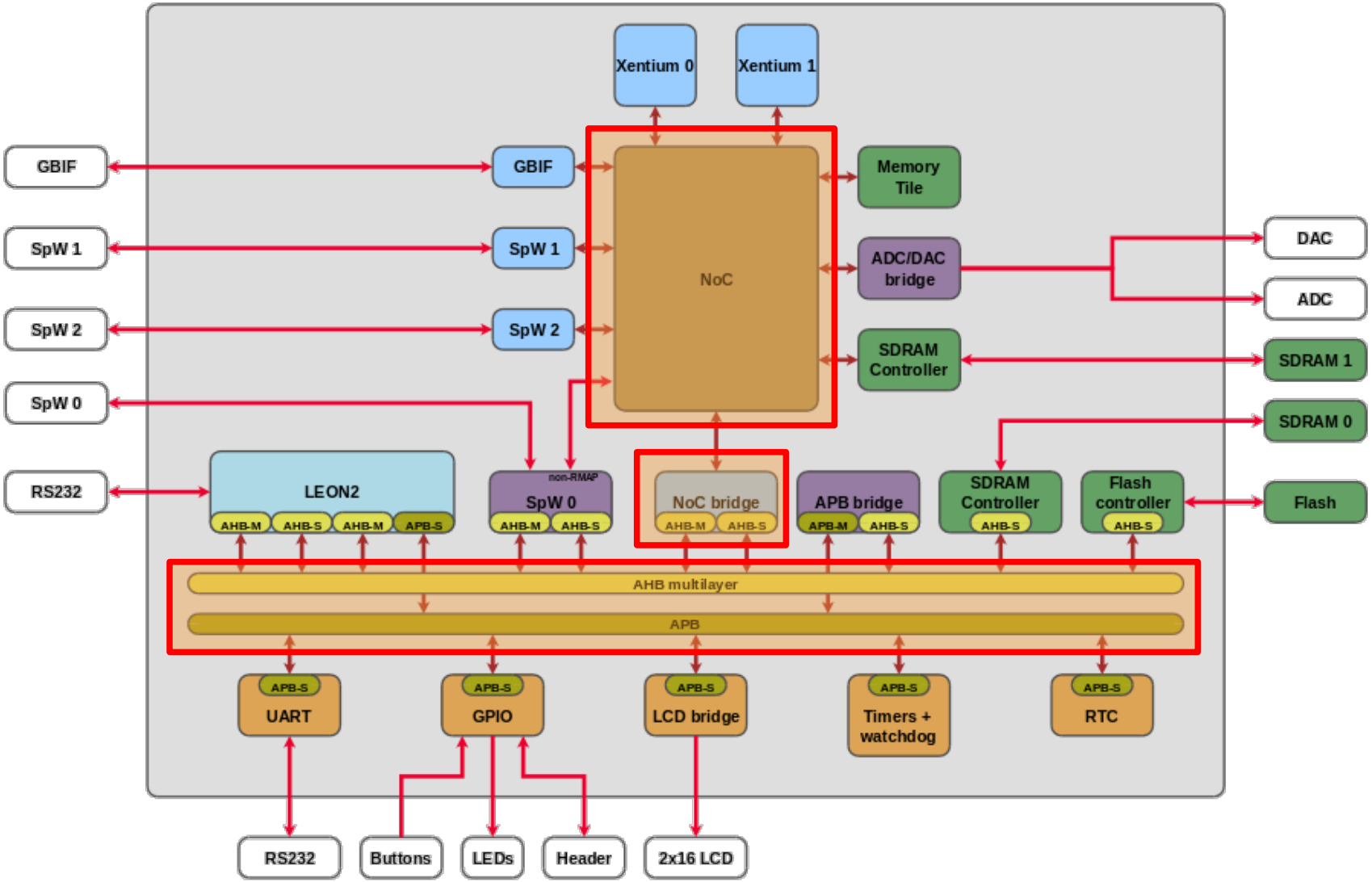
- 50 MHz system clock
- 2 Xentium tiles (@ 50MHz)
  - 2×200 16-bit MMAC/s
  - 2×100 32-bit MMAC/s
  - 2×100 16-bit complex MMAC/s
  - 2×32 KB data memory
  - 2×32 KB instruction cache
- 1 Leon2 processor (@ 50MHz)
  - 32-bit SPARC V8
  - Debug Support Unit / UART
- Network-on-Chip (@ 50MHz)
  - 32-bit packet-switched
  - 1.6 Gbps per link
    - In each direction
- Memories
  - 256 KB memory tile on NoC
  - 256 MB SDRAM on NoC
  - 256 MB SDRAM on AHB
  - 128 MB Flash on AHB
- SpaceWire (100 Mbps link)
  - 3 SpW-NoC interfaces
    - 1 including RMAP-target
- Gigabit interface
  - 1.1 Gbps full-duplex
    - Aurora link layer protocol
- ADC/DAC-NoC interface
  - Configurable sampling rate
  - 14-bit, 40 MS/s, ADC
  - 12-bit, 40 MS/s, DAC

MPPB Processing Unit

- Fully operational
- Ready for evaluation and software development
- 3 MPPB boxes delivered to ESA/ESTEC

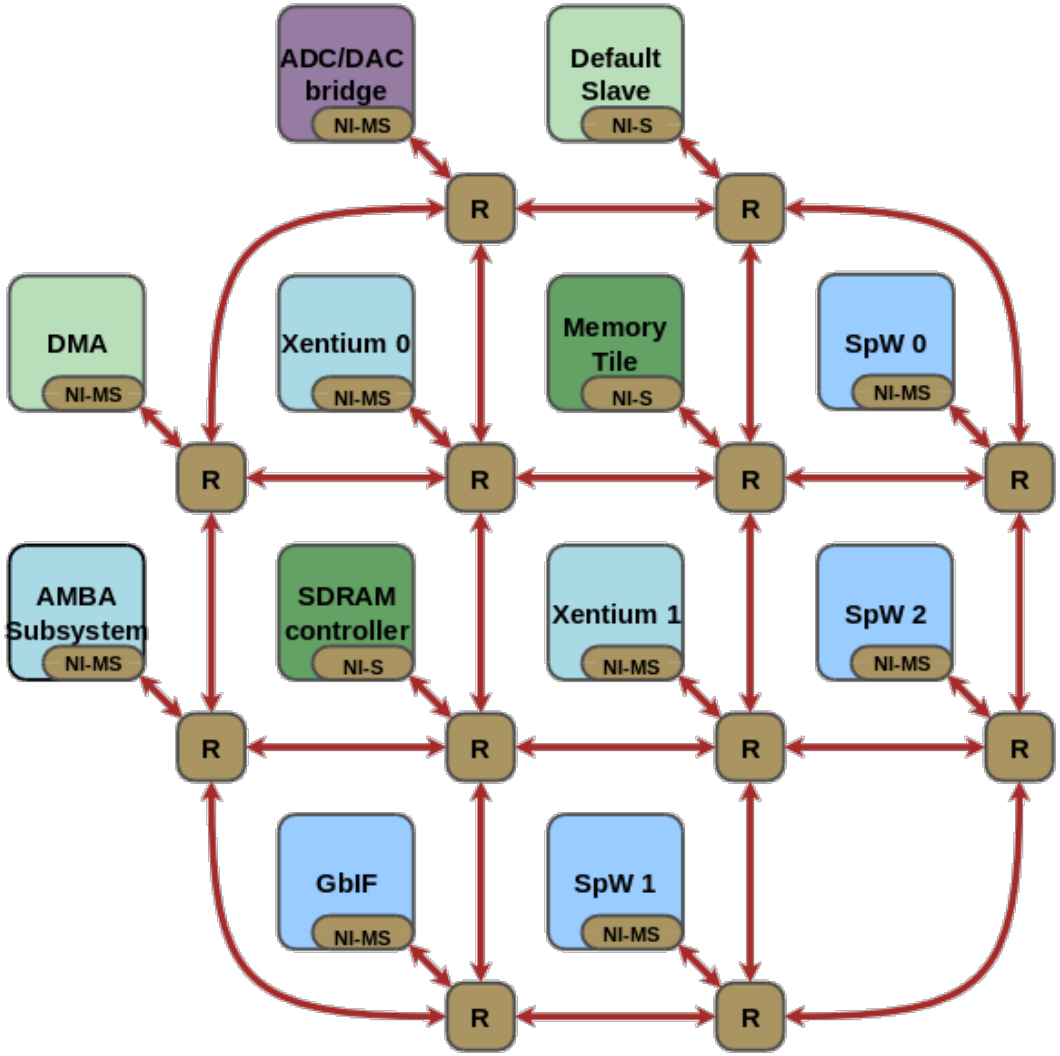


MPPB architecture
On-chip interconnect

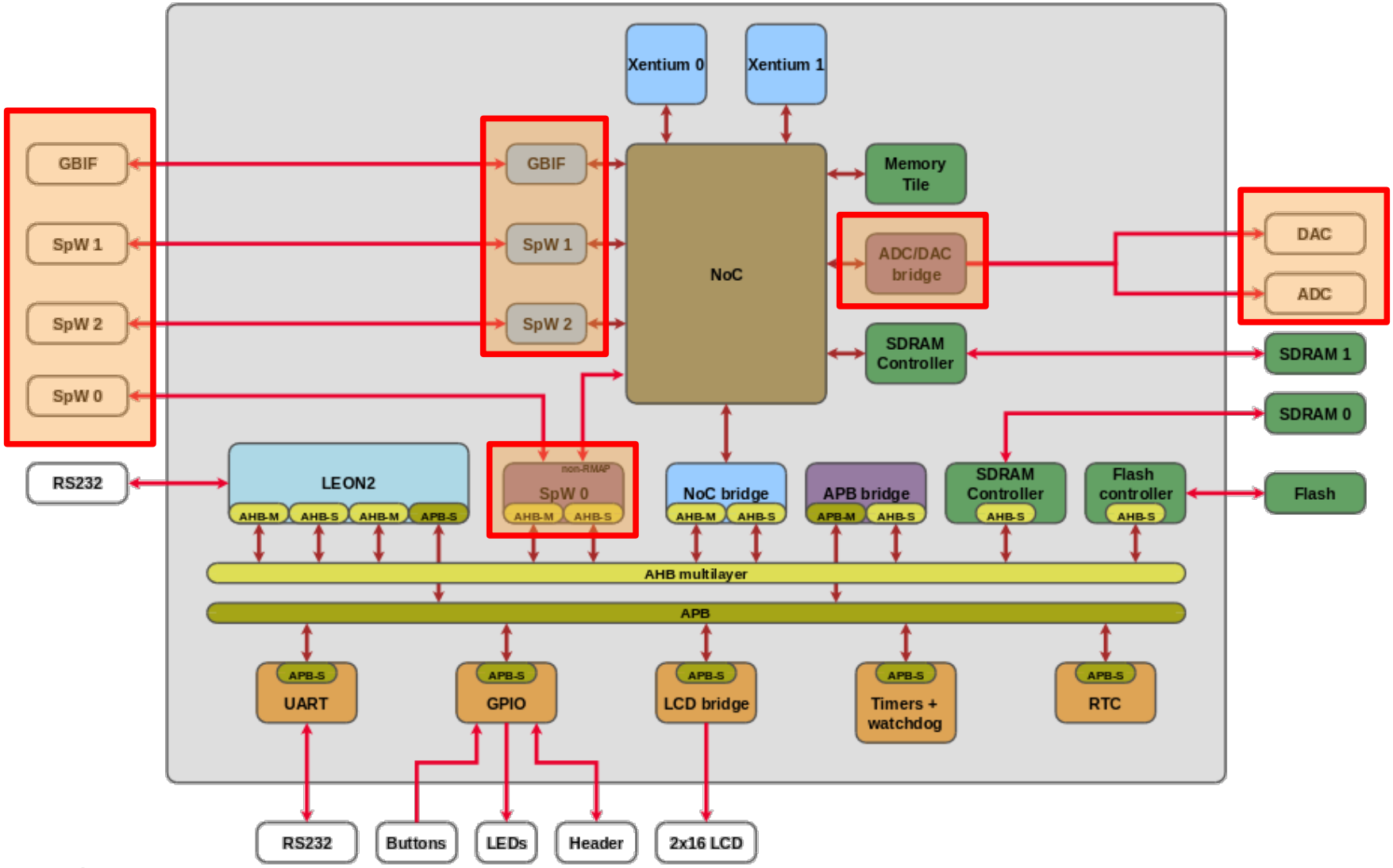


NoC subsystem

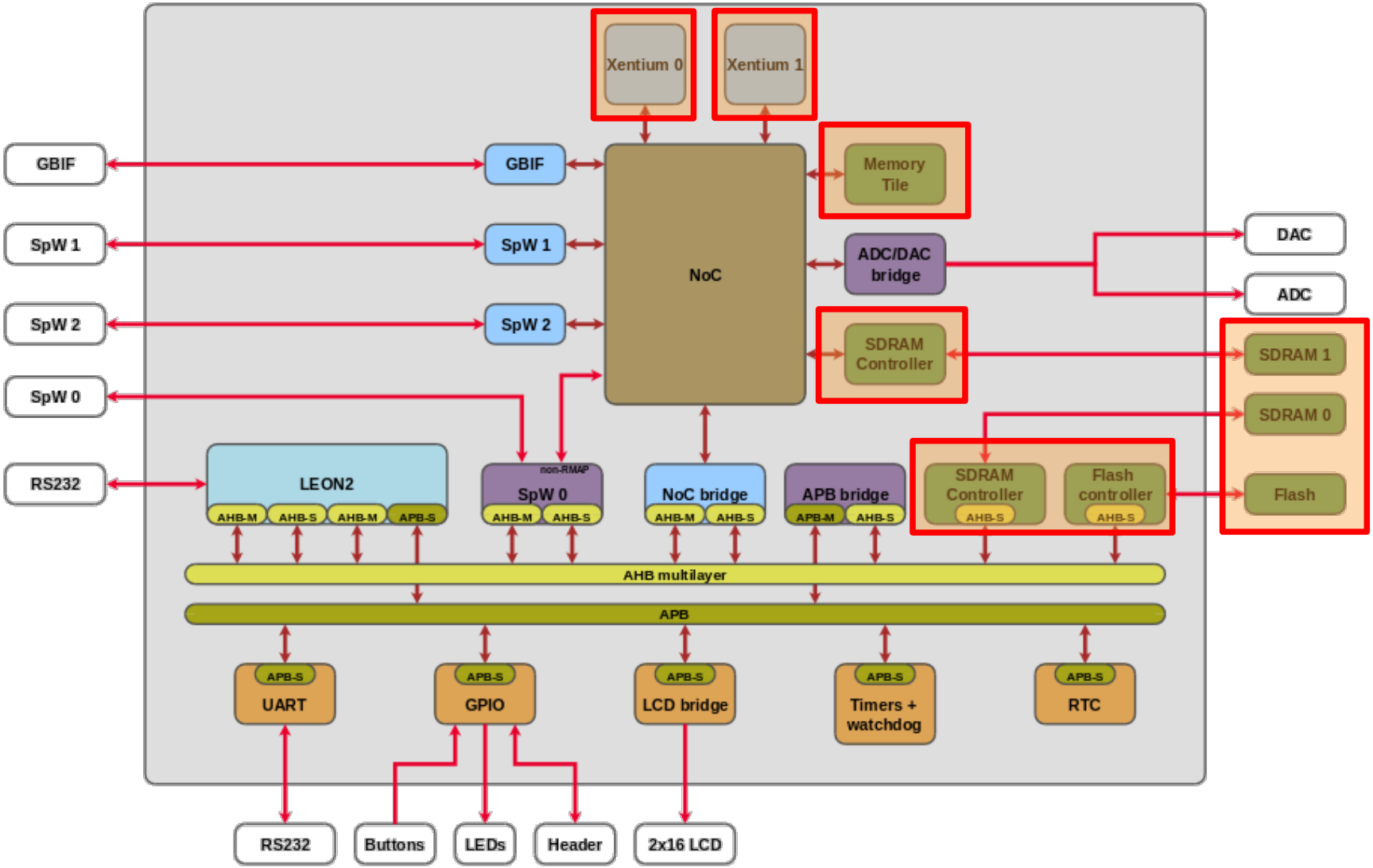
- Packet-switched routing
- 32-bit data links
- 5 port routers
- 4 services, priority based
  - for throughput and latency guarantees
- Memory mapped communication protocol layer
- X-Y routing
  - Deadlock free



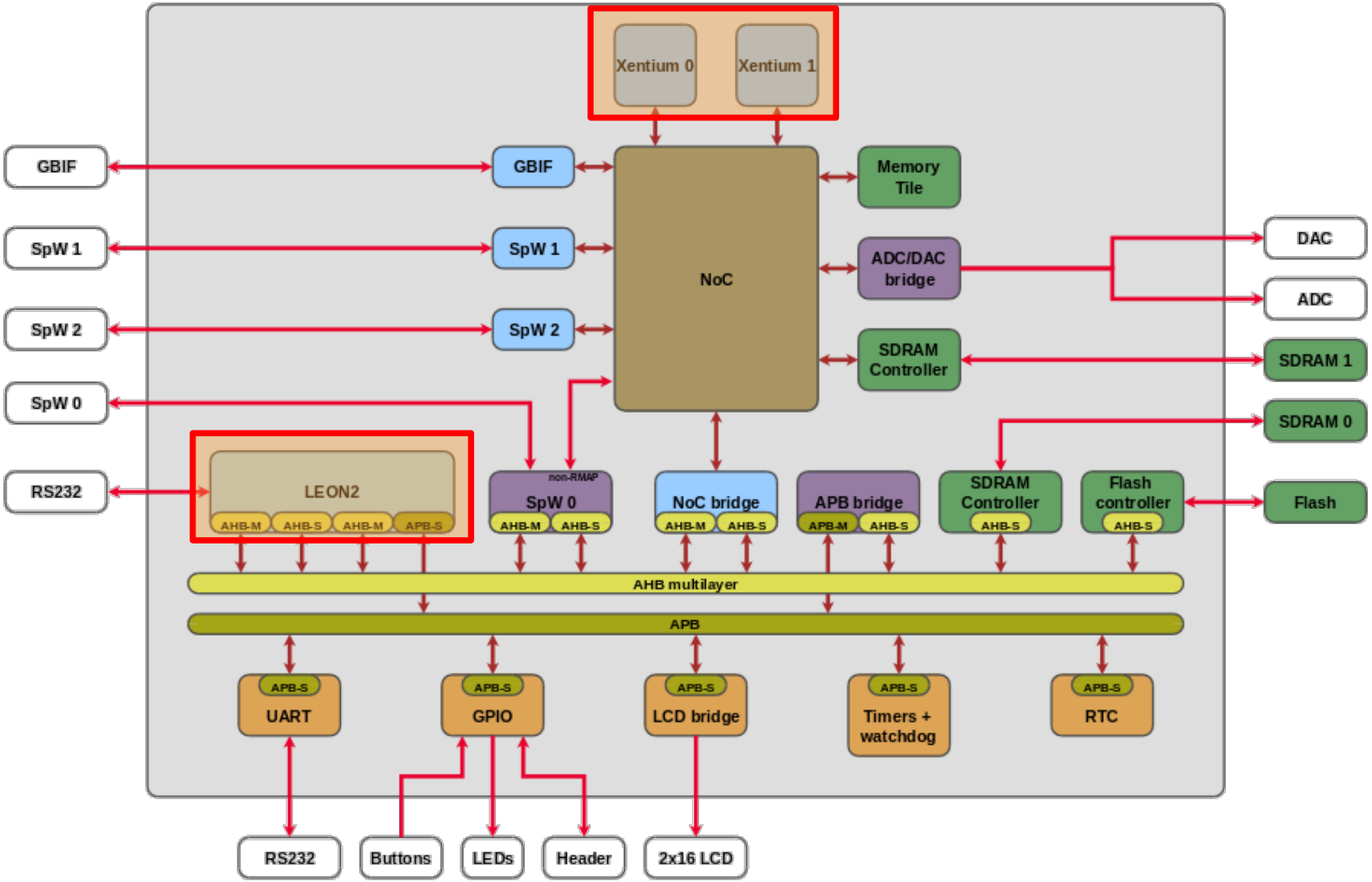
MPPB architecture
High-speed interfaces



MPPB architecture
Data Memories

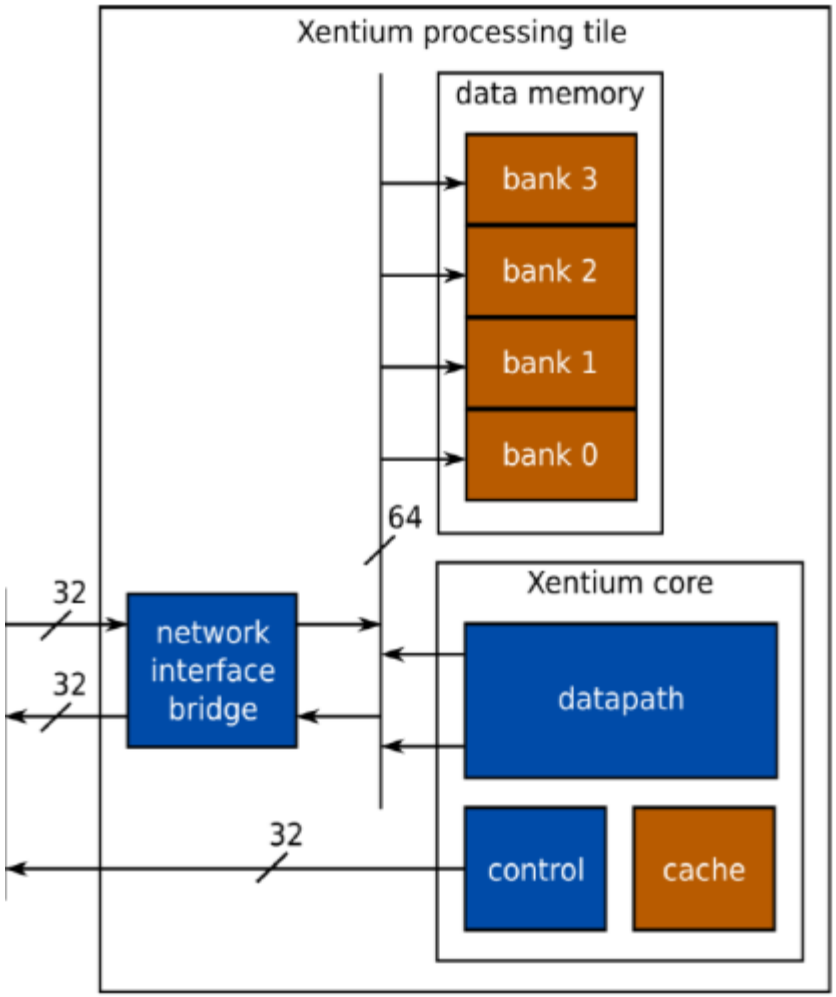


MPPB architecture
Processing cores

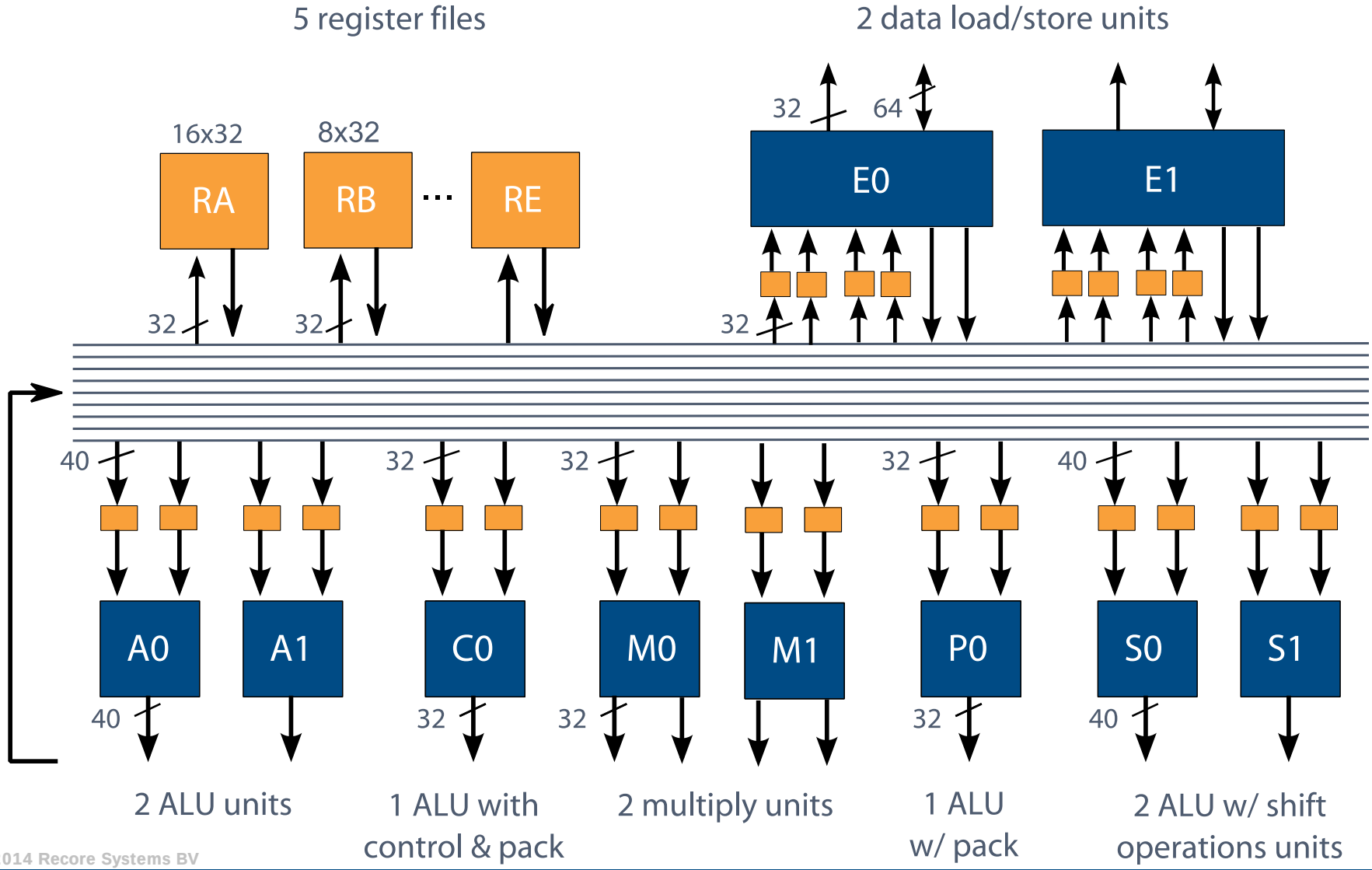


Xentium DSP Core

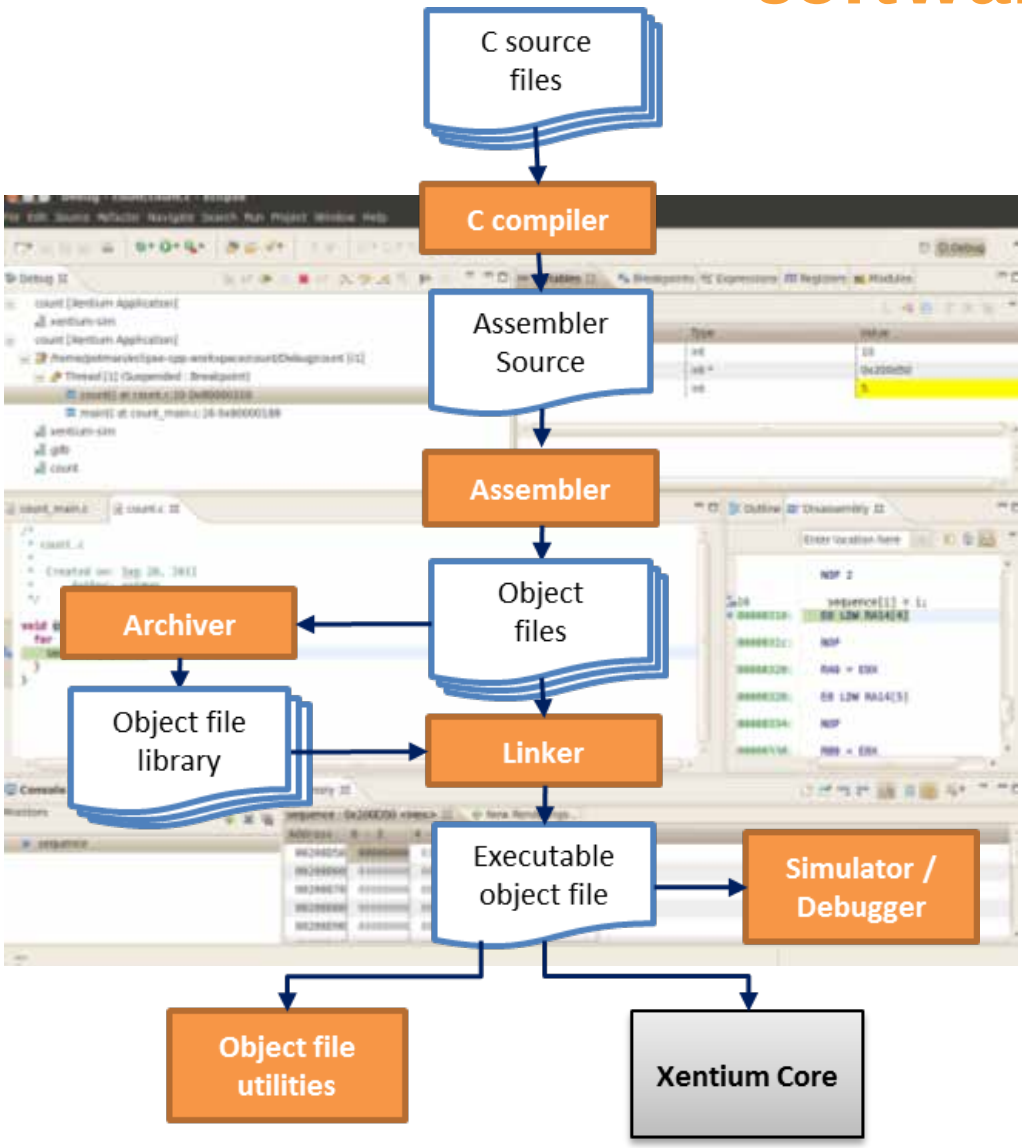
- Programmable high-performance DSP core
  - VLIW architecture with 10 parallel execution units
- Data precision
  - 32/40-bit fixed-point data path
  - 16-bit SIMD
- Features
  - Single-cycle data memory latency
  - Single-cycle instruction cache latency
  - Short 3-cycle pipeline
  - HW Loop buffer
  - Register bypassing
  - Efficient complex MAC execution: 2 16-bit complex MACs/cycle



Xentium - datapath parallel execution units

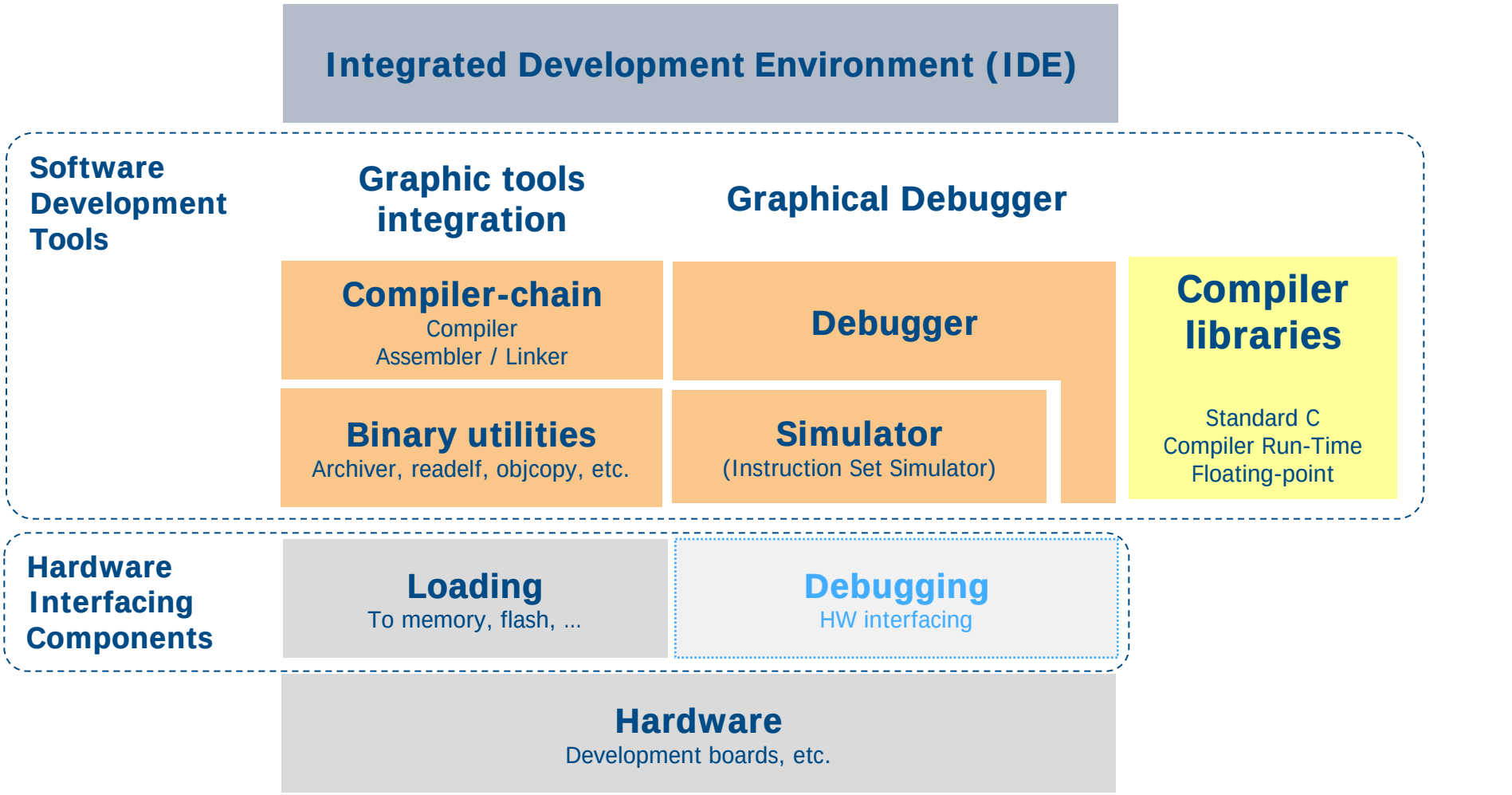


Xentium® software development flow



- Xentium C compiler
  - ANSI/ISO-standard C
  - Built-in functions for Xentium specific operations
  - Mix C and assembly functions calls
- Xentium assembler
  - Clean and readable
  - Extensive built-in preprocessor
  - Standard assembler directives
- Compile, assemble & link a program in a single step
- Xentium instruction set simulator
  - Trace program execution
  - Interactive debugging
  - Program profiling
- Xentium Eclipse Plug-in
  - Integrates command line Xentium tools into the Eclipse C/C++ IDE

Xentium Studio software development tools



Integrated toolchain

- Xentium binaries linked to LEON executable
- LEON executable uploaded to the platform in SREC format