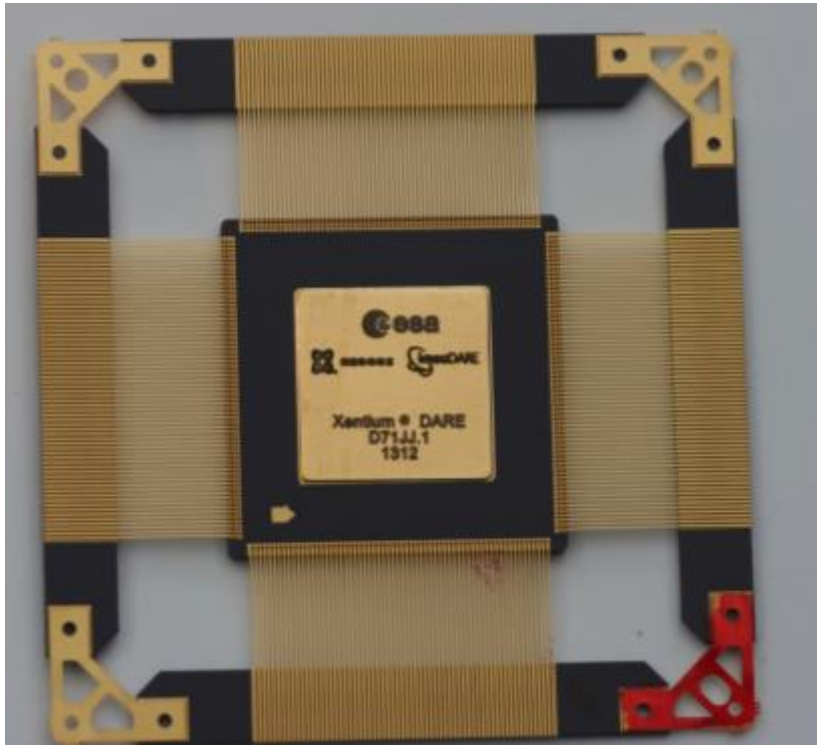


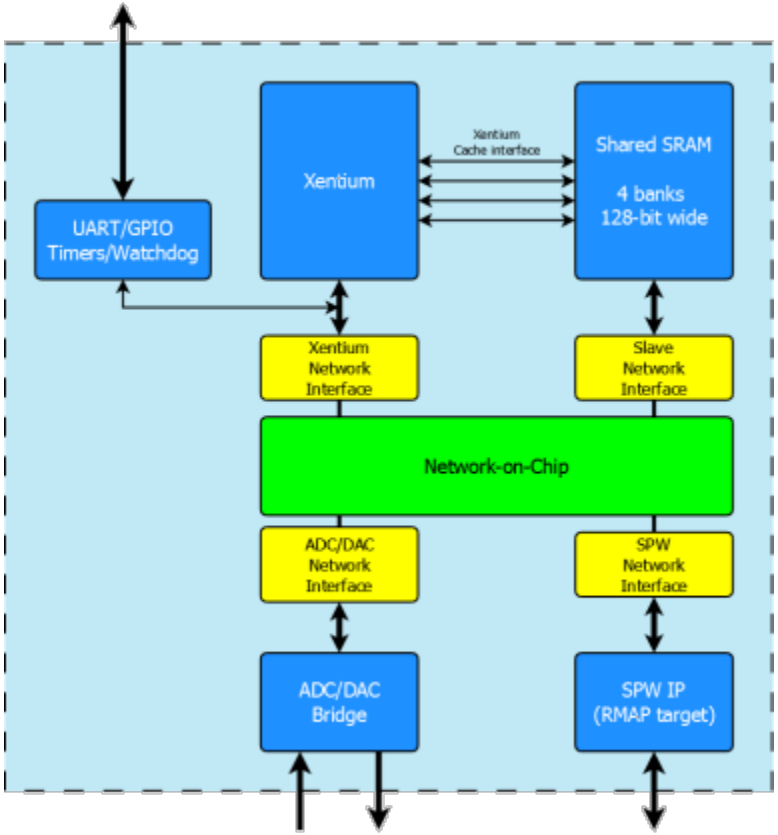
Step 2 – DARE+ / XentiumDARE

RAD.-HARD SILICON PROTOTYPE

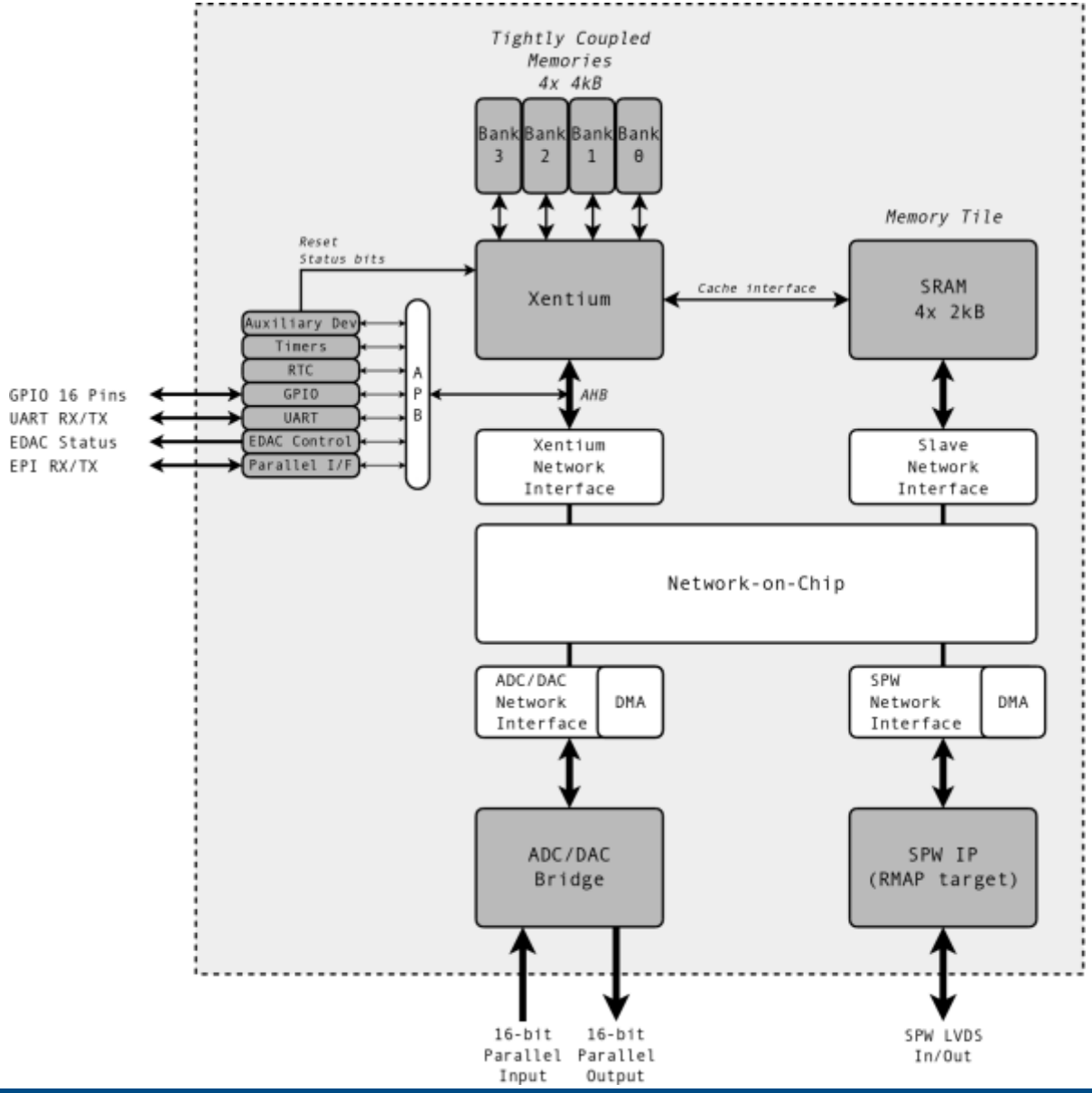
Rad.-hard DSP and NoC prototyping in DARE180

- DARE+
  - Rad.-hard prototyping of MPPB elements in DARE180
  - ESA TRP activity, 2011 – 2013

- ASIC Prototype
  - DARE180 CMOS technology
    - Available area: 5x10 mm^2
  - Architecture
    - 1 Xentium core @100MHz
    - Network-on-Chip
    - SpW-RMAP interface
    - Bridge interface to external ADC/DAC
    - Small memory tile

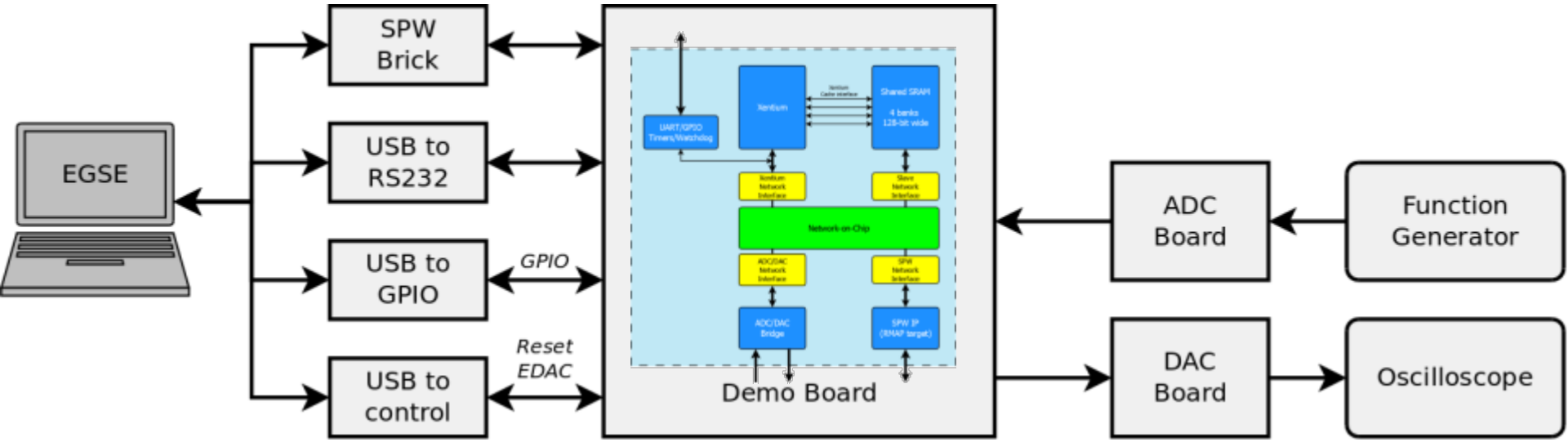


XentiumDARE Overview



XentiumDARE validation

- Functional testing
  - ESA NGDSP benchmarks
- Radiation testing
  - TID
  - SEE - SEU / SET



Benchmark Environment

XentiumDARE
Functional radiation tests

- Constraints:
  - Limited time for each ion
  - Functionality (no SPW)
- Self-checking Xentium programs:
  - Xentium + Memory Tile
  - Xentium + Data banks
  - Xentium + devices
  - Xentium + ADC/DAC
  - Xentium + SPW (front-end only)
- Xentium Binary uploaded to ASIC
- Results are output on the GPIOs

Benchmarks Introduction

- Subset of “Next Generation Space DSP Software benchmarks”
- Implemented 4 of 5 benchmarks
  - Benchmark 1: I/O Performance
  - Benchmark 2: Analog acquisition, processing and output
  - Benchmark 4: Onboard Data Processing Case 1
  - Benchmark 5: Onboard Data Processing Case 2
- Operating conditions
  - System frequency: 50 MHz*
  - SpaceWire frequency: 200 MHz (transmit clock)
  - Board power supply voltage: 1.95 V

* limited due to board issue; 100 MHz achievable

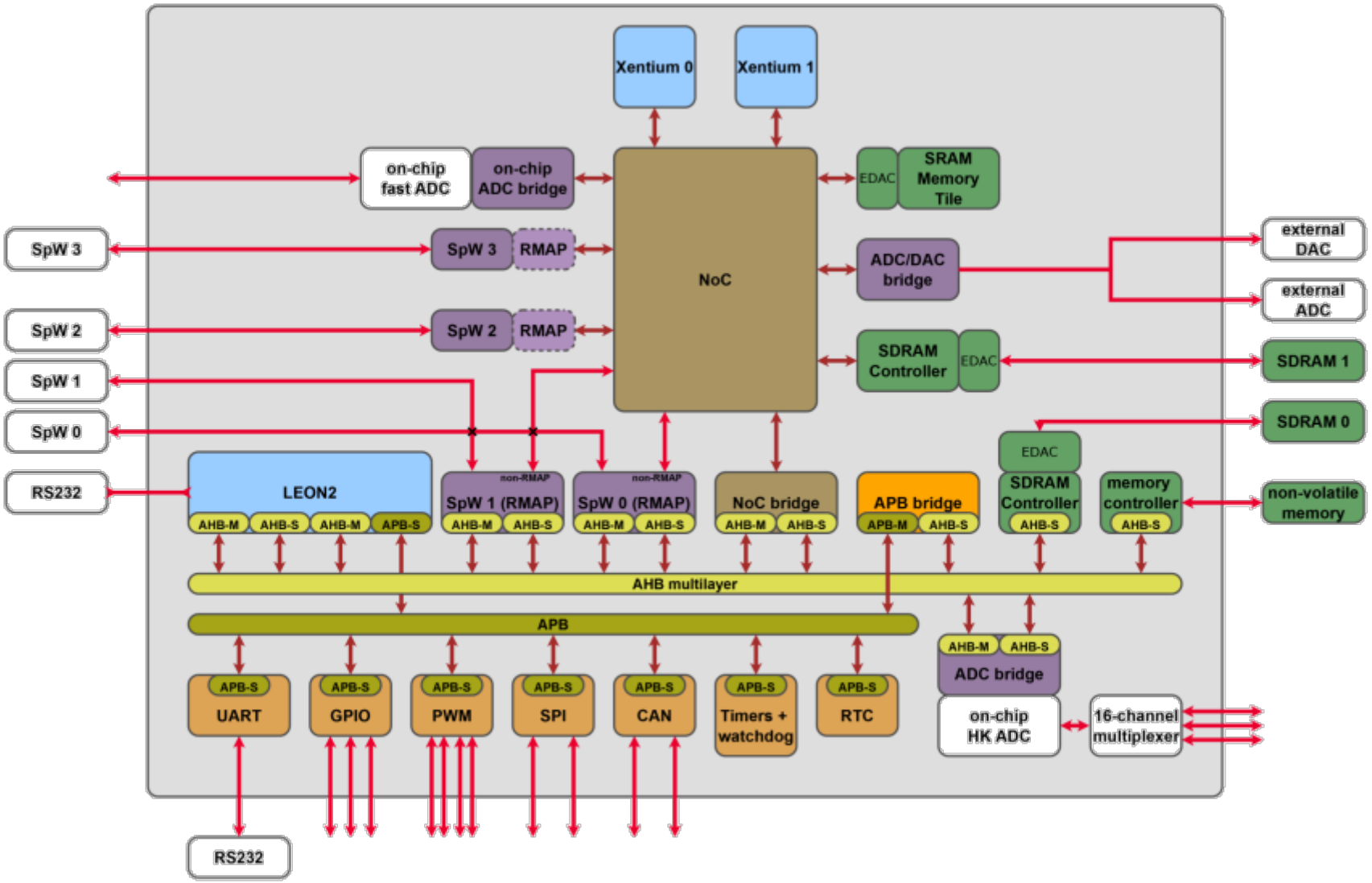
XentiumDARE Summary

- Final review & public presentation in December 2014
- XentiumDARE operational @100 MHz
- Power consumption: Core 1.8V; IO 3.3V
  - Dynamic <1.5W at full load
  - Static < 5mW
- Area
  - 5x10 mm^2
- Radiation hardened (1 Mrad, LET<70MeV/cm^2/mg)
- All benchmarks are functionally correct and pass
- Performance @ 100 MHz system clock
  - 400 MMAC/s (16-bit)
  - 16-taps FIR @20 MSPS
  - 1k-FFT @18 MSPS
  - ADC/DAC @50 MSPS max
  - SpaceWire @200 Mbit/s

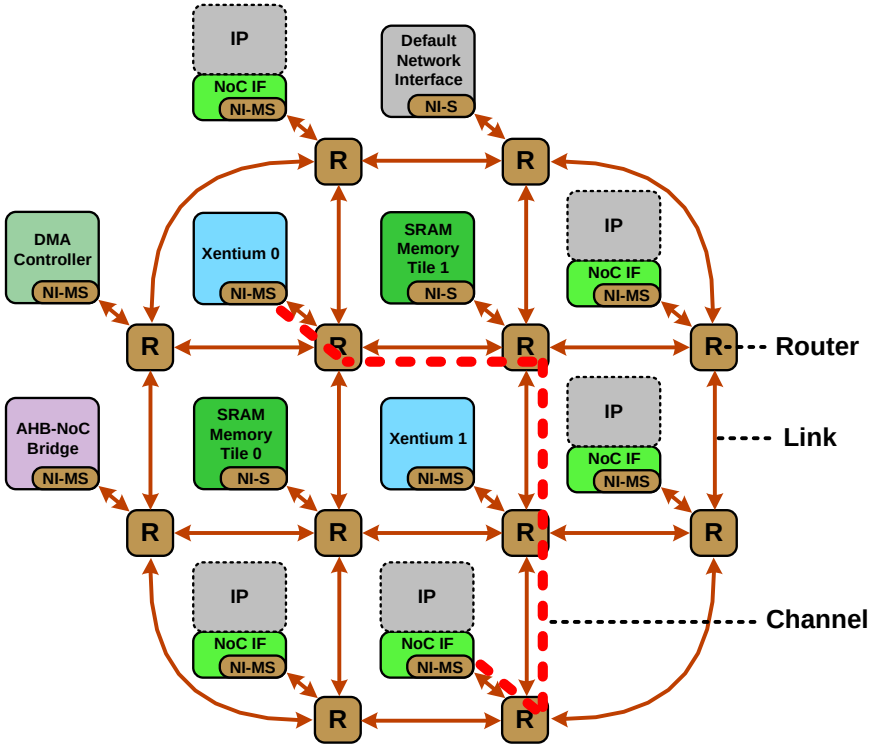
Step 3 – ASIC implementation

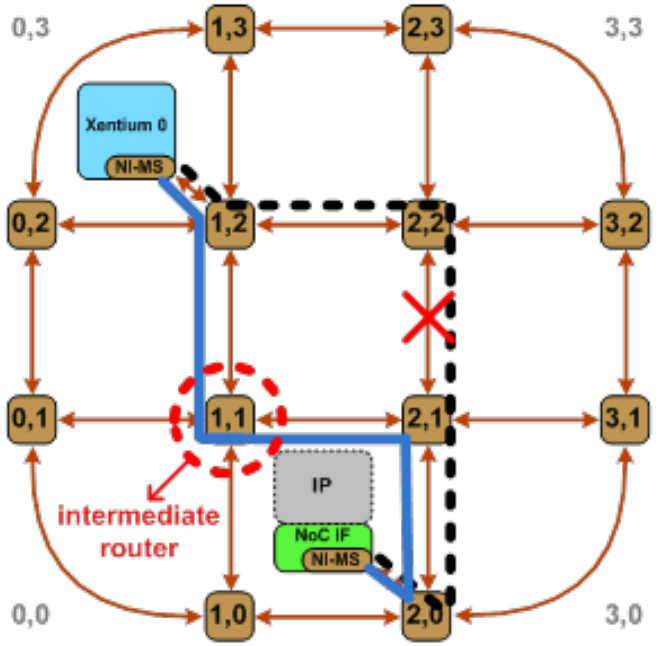
WHAT'S NEXT …

Scalable Sensor Data Processor (draft architecture)



Reconfigurable XY routing



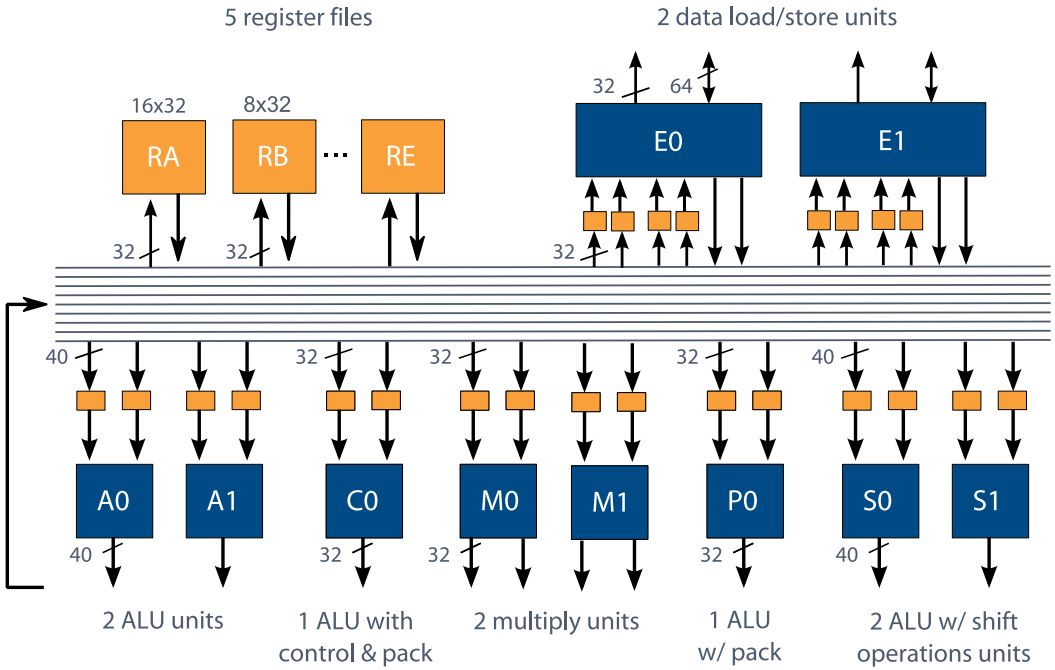


Work around (partly) faulty switches and links

DeSyRe
on-Demand System Reliability
www.desyre.eu

Xentium architecture hardware extensions

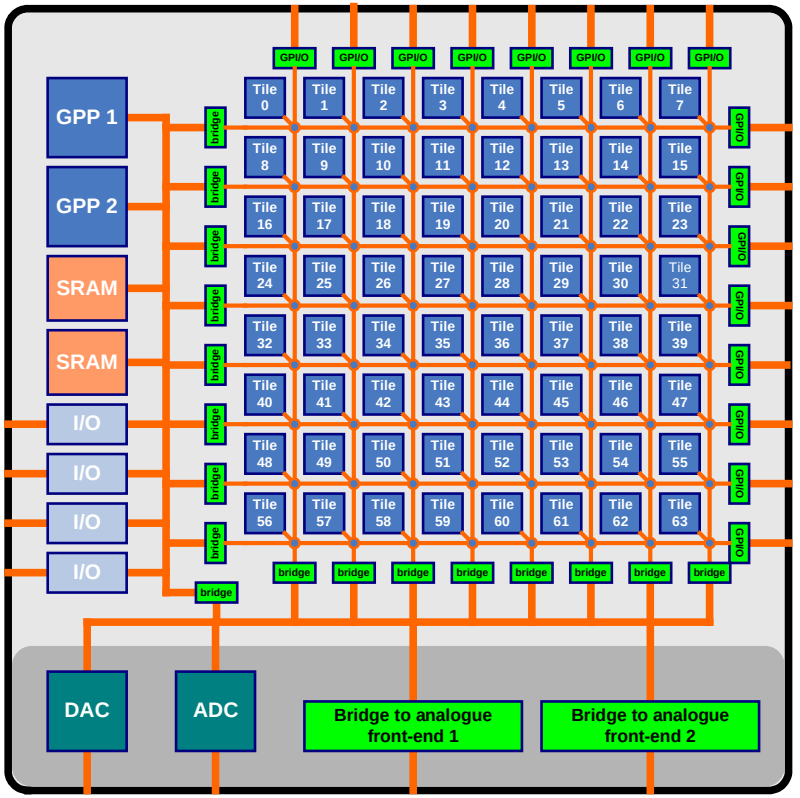
- Hardware floating-point support
- Bit manipulation instructions
- Hardware debug support



Many-Core DSP for Space 65nm - estimations

- Xentium VLIW DSP core in rad.-hard 65nm CMOS
  - Clock: 300 MHz
  - Performance: 1.2 GMACs/s
  - NoC per link: 9.6 Gbit/s
  - Area: 1.1 mm^2
    - 75% gates utilization
    - Including NoC interface
- Many-core SoC example
  - 48 Xentium processing tiles
  - 16 memory tiles
  - 60 NoC routers
    - 8×8 mesh

à **60 Giga MAC operations/s**



Summary

- Multi-core DSP architecture is
  - Heterogeneous and scalable
  - Functionally evaluated on FPGA in MPPB
  - Tested as rad.-hard ASIC prototype in XentiumDARE

- Multi-core Xentium DSP sub-system IP
  - Scalable processing power
  - Scalable NoC-based interconnect
  - Currently being integrated in Scalable Sensor Data Processor

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