ESA DSP Day 2014

September 19th, 2014

ESA/ESTEC

Overview / Logistics

ESA DSP Day 2014 Topics

- **Final presentations of <u>completed industrial activities</u>**

- **Status updates on <u>ongoing industrial work</u>**

- **ESA summary / roadmap update, discussions on future strategies, AOB**

Grouping of Topics

- **<u>AM</u>: Digital Signal Processor IP, DSP ASIC developments, related studies**

- **<u>PM</u>: COTS DSP based developments, summary / roadmap & discussions**

Other info

- **Presentations will be made available via DSP day website <u>after the event</u>**

- **<u>WiFi access</u> details => backside of your badge**

Development Routes for Payload Data Processors

The following development routes have been followed in recent years (since ADCSS2007)

Hardening of a <u>COTS DSP</u> against radiation effects on board / software level
- Does not depend on other technologies such as ASIC DSM
- Potentially fast route to performant processor boards
- Problem areas: Reliability, radiation hardness, complexity, mass and power

Hardening of a proven COTS DSP <u>architecture</u> by using a <u>space qualified ASIC</u> platform and transparent modifications
- Re-use of Software Development Environment (SDE), commercial chips saves cost
- High maturity IP, SDE
- IP hardening and -cost are potential issues

Development of a <u>multi-core DSP</u> / massively parallel IP based processor
- High performance feasible,
- IP hardening, SDE maturity, programming are potential issues

Reconfigurable <u>FPGA based</u> solutions
- Interesting for specific solutions, potentially fast route to flight hardware
- Problem areas: Reliability, radiation hardness, power consumption, ITAR

European Space Agency

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COTS DSP

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Development of a multi-core DSP / massively parallel IP based processor
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DSP ASIC

Reconfigurable FPGA based solutions
- Interesting for specific solutions, potentially fast route to flight hardware
- Problem areas: Reliability, radiation hardness, power consumption, ITAR

ESA DSP Day 2014 – Agenda

Time	Agenda Item	Presenter
09:00 - 09:15	ESA introduction	ESA
09:15 - 10:00	**DARE+ Application ASIC / Hardened DSP IP and Tools**	Recore Systems b.v.
10:00 - 10:20	**Scalable Sensor Data Processor Development Status**	TASE
10:20 - 10:30	Parallel SSDP / DSP related ESA activities	ESA
10:30 - 10:50	*Coffee break*	-
10:50 - 12:20	**NGAPP final presentation**	RSA / UVIE
12:20 - 12:40	**HPDP development status**	ISD /Airbus D&S
12:40 - 14:00	*Lunch break*	-
14:00 - 16:00	**HiP COTS based computer final presentation**	Airbus D&S / CGS
16:00 - 16:20	*Coffee break*	-
16:20 - 16:50	**HPPDSP Development Status**	Airbus D&S / UoD
16:50 - 17:20	ESA summary / DSP roadmap update	ESA
17:20 - 18:00	Public discussion	ESA

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