Scalable Sensor Data Processor Development Status
DSP Day - September 2014

25/09/2014

THALES ALENIA SPACE INTERNAL

ThalesAlenia Space
A Thales / Finmeccanica Company

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Presentation of the SSDP ASIC Program & Context

- SSDP will be the first Space Qualified European multi-core Digital Signal Processor (DSP) devoted for future space missions.
- This mixed signal SoC (System-On-Chip) ASIC implementing a multi-core payload data processor is developed in the frame of an ESA's CTP contract.
- This chip will merge 2 Recore's Xentium VLIW DSPs with existing, proven space technologies such as Leon2-FT and data interfaces, as SpaceWire, CAN, SPI, etc.. to create a payload processor capable of managing the wealth of data collected in future space missions.
- The internal blocks and associated memories are interconnected with a powerful Recore's Network-on-Chip grid on the Xentium subsystem and an AMBA bus on the Leon Subsystem. Both subsystems are interconnected by a bridge.
- Firstly foreseen target missions: JUICE & Lunar or Mars landers
- SSDP also planned to be generic DSP component for Subsystems, Payloads, etc..

Teams Presentation: Consortium organization

The Industrial Consortium comprises the following members:

- **TAS España** (Spain): Prime Contractor and in charge of:
  - MPPB evaluation
  - ASIC Specification, Architectural, Detailed design, and Verification and Validation activities.
  - Design and manufacturing of the Evaluation Boards
  - EGSE responsible

- **Imec vzw** (Belgium): in charge of:
  - Provider of UMC-DARE technology and libraries
  - Support to TAS España on technology, IPs & Package selection
  - ASIC layout
  - ASIC samples manufacturing, packaging, and electrical testing.

- **Recore Systems BV** (The Netherlands): in charge of:
  - Support to TAS España on MPPB evaluation,
  - Xentium, NoC, DMA,etc.. IPs enhancements development
  - Support to TAS España on ASIC/EGSE SSDP HW & Software
  - SDE responsible

- **Arquimea Ingeniería** (Spain): in charge of:
  - provider of the Fast ADC IP and related engineering support

Presentation of the SSDP Program & Context

- JUICE is a mission to the Jupiter system and its moons Callixto, Ganymede and Europa. Specific requirements of this mission include, in addition to the strong need for efficient power consumption and mass, high radiation tolerance (in the order of hundreds of krad) due to the specific challenges of the Jupiter system.

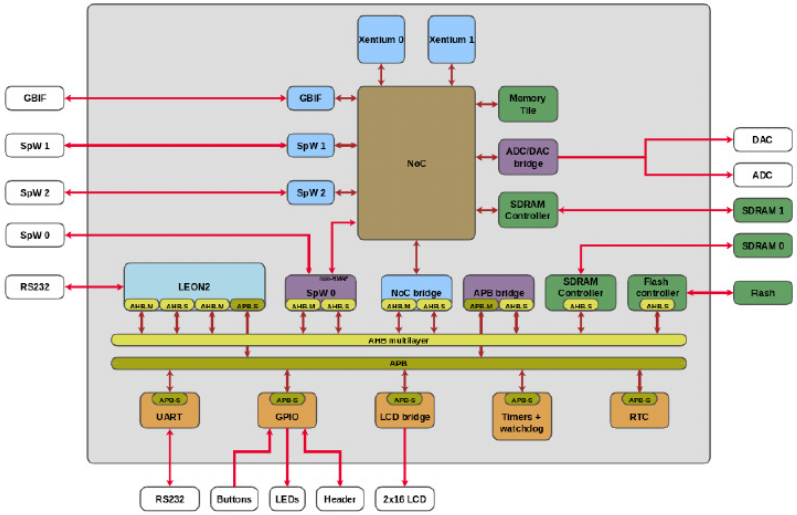
- Lunar or Mars landers are foreseen to exploit optical navigation methods for controlled entry, descent and landing, creating a need for high processing power, predictable and combined with efficient interfaces to next generation imaging sensors, with low mass and low power consumption.

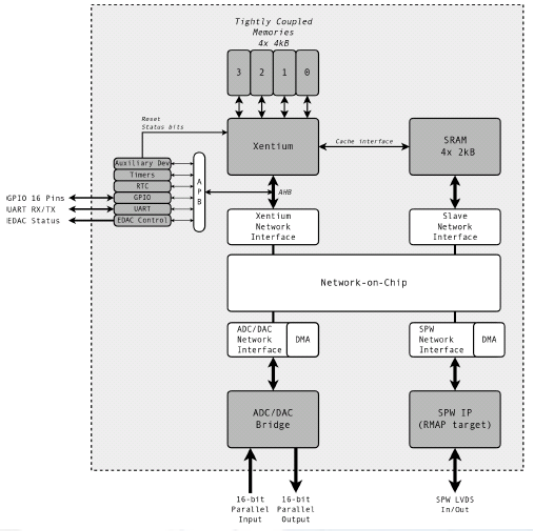
- SSDP Program is conceived to ensure the general availability of high tech processor with the highest degree of flexibility, configurability, connectivity, scalable processing power, highly rad-tolerant, low power consumption, low mass, low volume to cover needs for future missions like Juice, and Lunar and Mars Landers.

- IMEC DARE-UMC 180 nm Technology Selected:
  - Outstanding Radiation Performances
  - Mixed Signal Capabilities
  - Availability of Analog IP Blocks.

Previous projects heritage

- MPPB: Massively Parallel Processing Breadboard:
  - EM with 2 Xentium & 1 Leon on a XILINX FPGA.
- DARE+ Application ASIC
  - Xentium & NoC Grid implemented on 180 nm DARE UMC ASIC
- NGDSP: European DSP Trade-off & Definition Study
  - Evaluation of Different DSP Processors including MPPB
- NGAPP: Next Generation Processing Platform.
  - Evaluation of MPPB

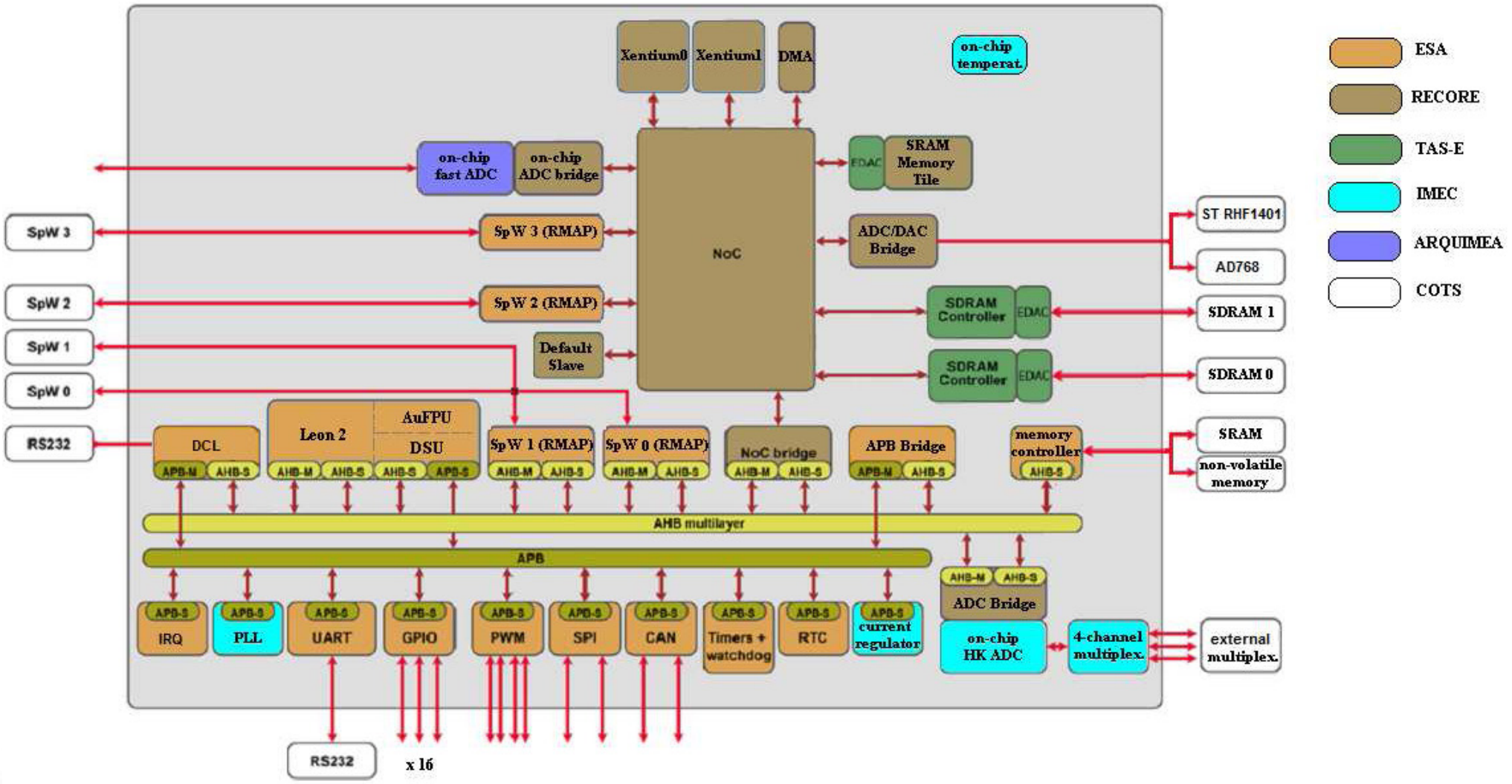




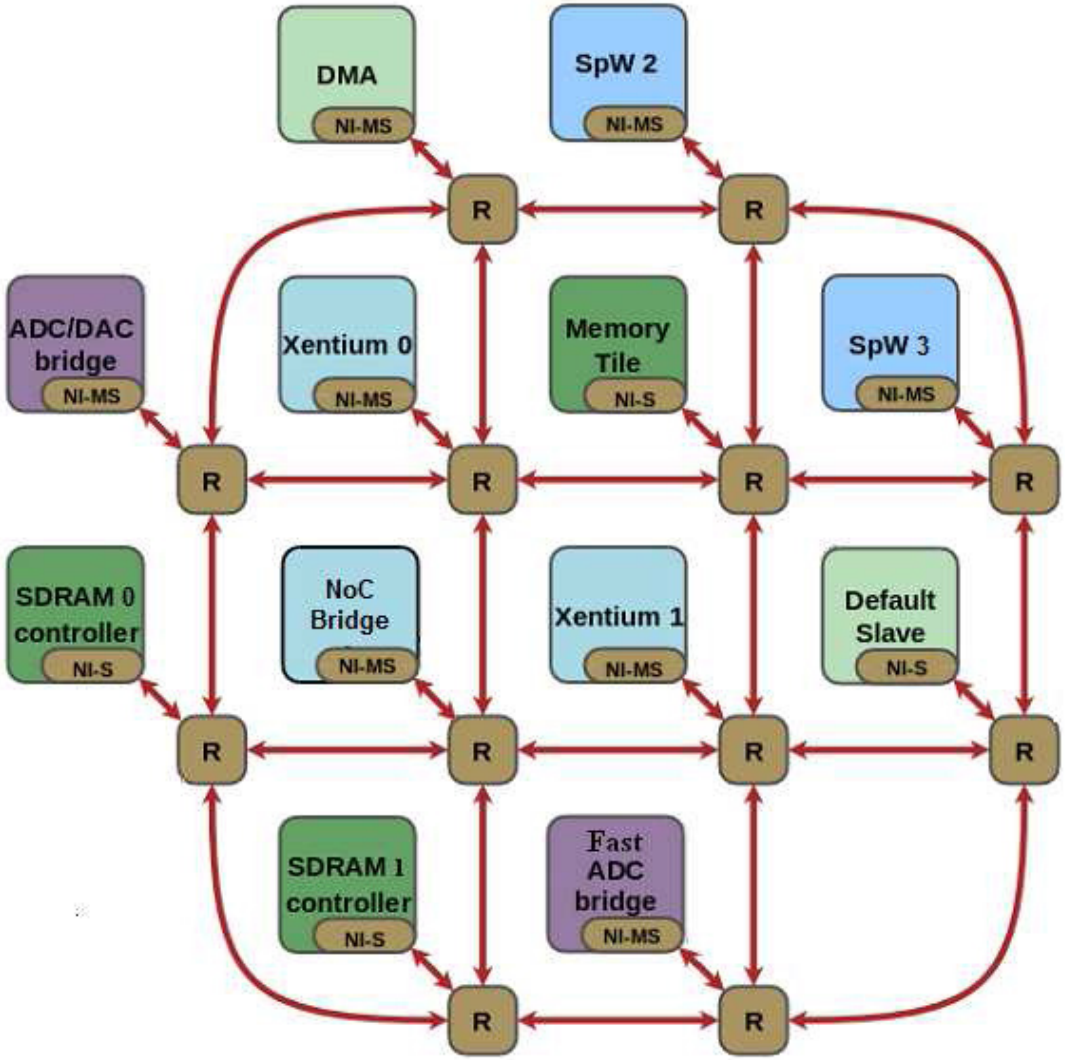
SSDP & SDE enhancements

- Evaluations identified architecture improvements.
- But such a complex design requires also a complex SDE toolset
- Improvement areas identified during MMPB evaluations
  - Compiler improvements
  - Simulation support enhancements
  - On target debugging Hw Support
  - Traffic Profiling monitoring
  - Optimised DSP libraries
  - SW Low Level Drivers
  - Board Support Routines

Preliminary SSDP Block Diagram

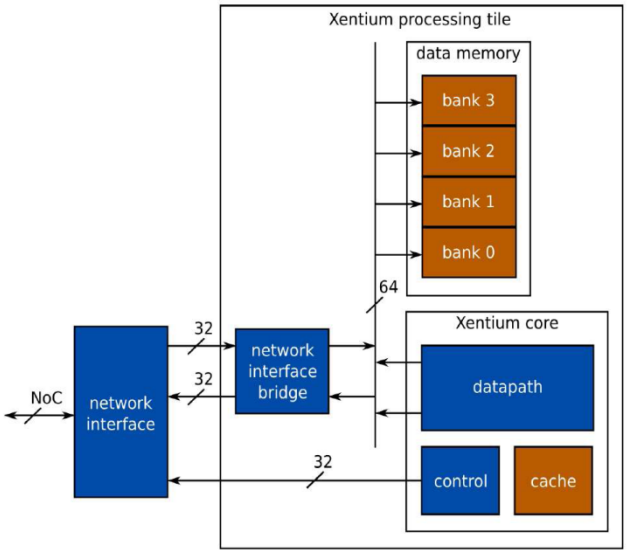


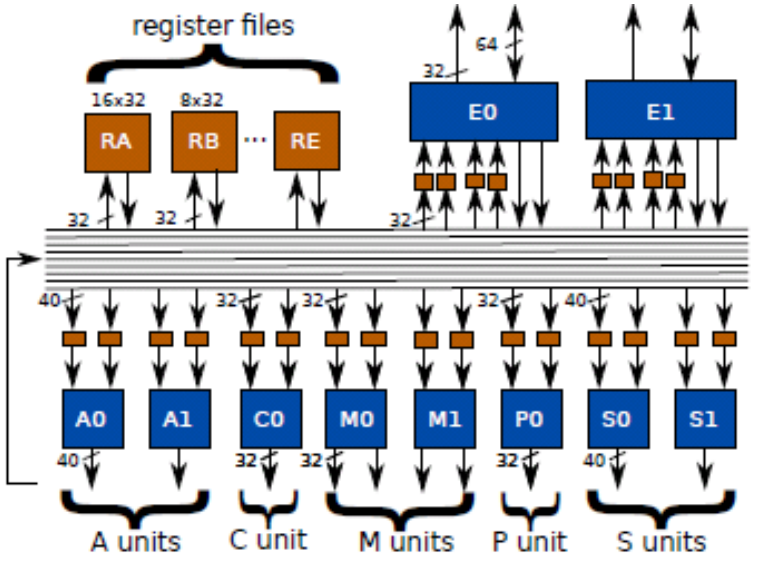
SSDP NoC Grid



Xentium Processor

- Programmable high-performance fixed-point DSP processor
- VLIW architecture with
  - 10 parallel execution units
    - 4 16-bit MACs per cycle
    - 2 32-bit MACs per cycle
    - 2 16-bit complex MACs per cycle
- Data precision
  - 32/40-bit datapath

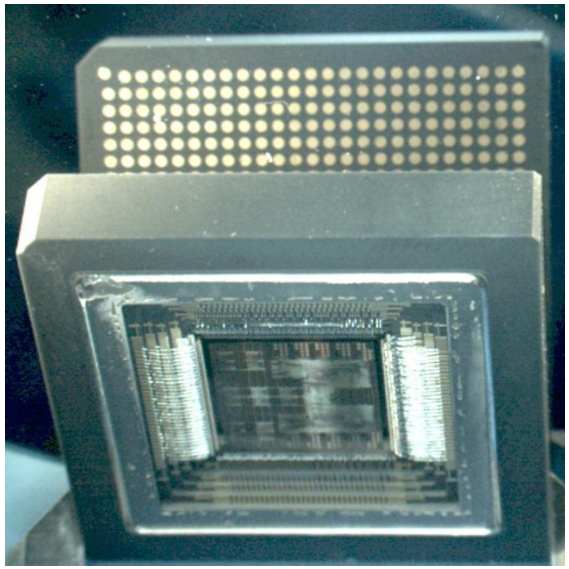




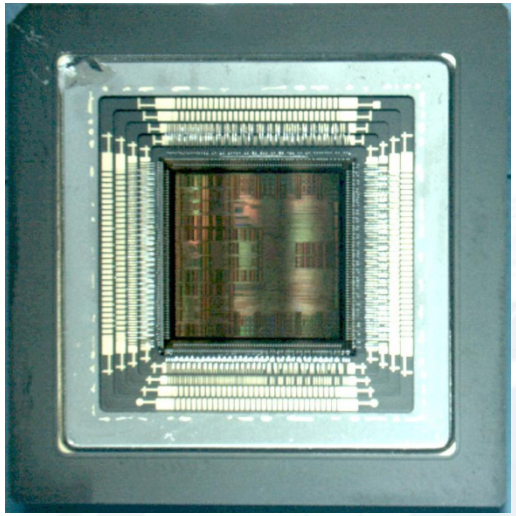
SSDP ASIC Budgets (I)

- 100 MHz System Clock.
- 2 Xentium tiles (@ 100MHz)
  - 2×400 16-bit MMAC/s
  - 2×200 32-bit MMAC/s
  - 2×200 16-bit complex MMAC/s
  - 2×32 KB data memory
  - 2×16 KB instruction cache
- 1 Leon2-FT processor (@ 100MHz)
  - 16 Kbytes I & D Caches
  - FPU: 60 Mflops target.
- Network-on-Chip (@ 100MHz)
  - 32-bit packet-switched
  - 3.2 Gbps per link bidirectional
- Internal Memory
  - 64 KB memory tile on NoC
- SpaceWire (200 Mbps link)
  - 2 SpW-NoC RMAP interfaces
  - 2 SpW-AHB RMAP interfaces
- 16-bit Fast ADC-NoC interface
  - Configurable sampling rate
  - 10-bit ENOB, 100 MS/s
  - 12-bit ENOB, 20 MS/s

SSDP ASIC Budgets (II)



- Complexity Estimation:
  - Random Gates: 1,5 M Gates
  - Memory: 2 Mbits
- 6 Watts Maximum Power
- Package Baseline: CGA-625 (CQFP-352 option with reduced capability)



- 300 Krad Target (1 MRad desired)
  - DARE-UMC: Tested up to 1 Mrad.
- LET Threshold for SEU > 50 MeV*cm2/mg
  - DARE-UMC: SEU > 67 MeV*cm2/mg
- LET Threshold for SEL > 70 MeV*cm2/mg
  - DARE-UMC: SEL > 111,4 MeV*cm2/mg

3rd party IP Blocks to be included (TBC)

Exact name of BIPR Item	Owner	Description	Patent # or Ref./Issue /Revision/ Version #	Contract /Funding Details under which the IPR was created	Date of creation of the version of the BIPR listed here	Affected deliverable with comments
Xentium IP	Recore Systems	High-performance fixed-point VLIW DSP core	V 1.0	Recore funded	2012-05	SSDP chip
Xentium Studio SDE	Recore Systems	Software development tools for Xentium DSP core (compiler, assembler, linker, simulator, debugger)	V 1.0	Recore funded	2012-03	SSDP SDE
Network-on-Chip IP	Recore Systems	Packet-switched on-chip interconnect technology, consisting of NoC router, NoC interfaces, and DMA	V 1.0	Recore funded	2012-10	SSDP chips
IEEE 754 FPU	AED	High Performance FPU	Version 1.0	AED Funded	Feb 2013	SSDP chip
ADC 13 bit 1MS/s	IC-SENSE	The available ADC has ~11.5 ENOB (depends on S&H), 1.5b INL, 0.5b DNL. Speed can be scaled. Imax = 10mA. In addition the number of bits can be scaled by digital control to 8 bits. Highly flexible input structures for all applications, offset compensation, diff or SE, common mode independent…		ESA funded		SSDP chip
16 channel MUX	IC-SENSE	Analogue 16 channel multiplexer		ESA funded		SSDP chip
120MHz PLL	IC-SENSE	Fully integrated. SET hardened. 120 MHz		ESA funded		SSDP chip
		+/- 10% (wider range or centre frequency tuning possible), 100kHz resolution,				
Temperature reference on chip	IC-SENSE			ESA funded		SSDP chip
Low dropout regulator	IC-SENSE	Available for 460mA and 30mA load current Can be adapted to other current levels. High efficiency: consumption only 0.3% respectively 0.5% of full load current.		ESA funded		SSDP chip
HF COSMIC VISION ADC IP	Arquimea	ADC 10 to 100MHZ	Version 1.0	ESA funded ESA Contract 4000101621	Feb 2013	SSDP chip

ESA IP Blocks to be included (Preliminary)

- ESA/Gaisler Leon2-FT, including peripherals
- ESA/Astrium SpW RMAP
- ESA HurriCANe
- ESA RTC/CUC-CTM
- ESA PWM
- ESA EDAC

Status of the SSDP

- TASE has performed MPPB evaluation
- Requirements Specification under consolidation.
  - MPPB suggestions from Airbus D&S, RUAG, and GMV MPPB evaluation.
- RECORE: analysing and implementing Xentium & NoC enhancements.
  - Functional Changes, Optimisations, Hw debug support, Profiling
- IMEC & TASE working on the package definition.
  - IMEC providing DARE-UMC technical support.
- IP Selection consolidation: All partners.

Main milestones – Foreseen Planning

Basic Development Activities:

- ***SRR: requirements definition consolidation and final IP selection***
  - ***Q4-2014***
- ***CDR: Design Review***
  - ***H2-2015***
- ***Electrical, Functional Tests and Validation***
  - ***H1-2016***

Conclusion

Questions & Suggestions