HPDP Development Status and Experiences

ESA DSP Day 2014

Laurent Hili (ESA) / Constantin Papadas (ISD) / Mohsin Syed (Airbus DS)

19-Sep-2014

AIRBUS DEFENCE & SPACE

Contents

- Introduction
- Details of HPDP Demo Chip
- Overview of STM65 Technology
- Current Results and Experiences
  - Synthesis (commercial STM65)
  - Scan-insertion (commercial STM65)
  - Formal Equivalence (commercial STM65)
  - Netlist update for Rad-hard technology
  - Synthesis (rad-hard STM65)
- Next Steps

Motivation

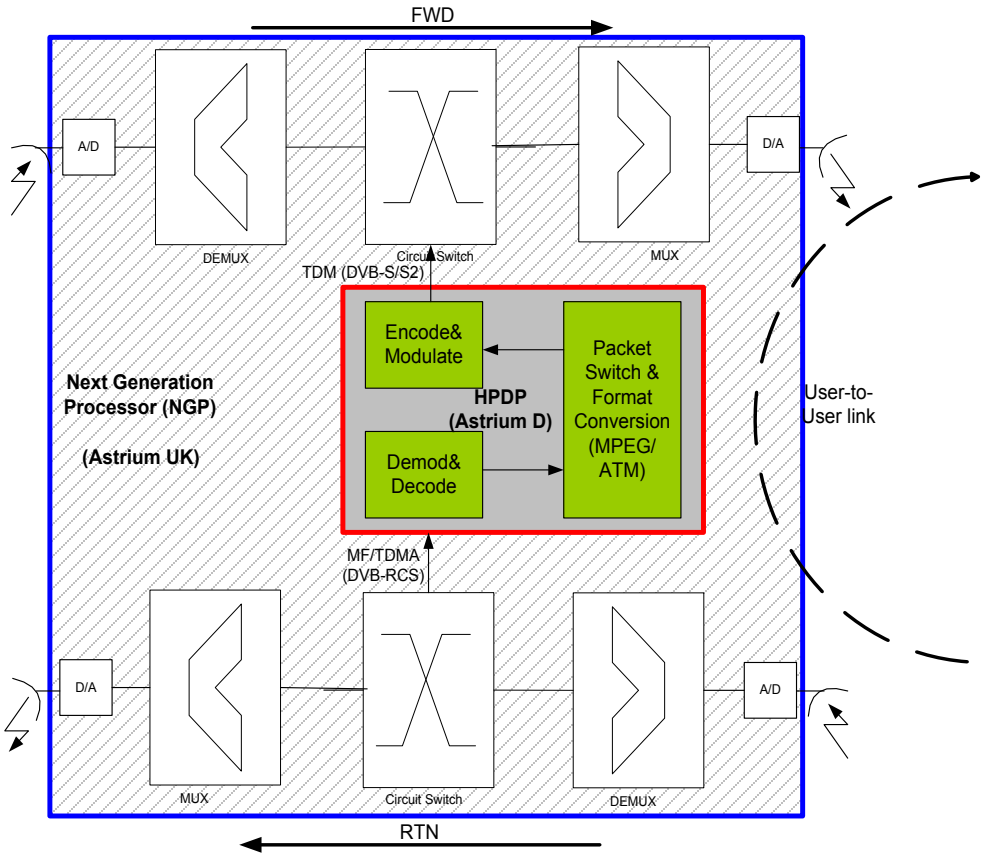
- Implementation of the High Performance Data Processor (HPDP) Demo Chip
  - Verify the functionality of the HPDP chip design
  - Get accustomed to the chip development flow of the future European deep sub-micron process

- The prototyping is carried out within the ESA Greek Industry Incentive Scheme:
  - ISD as prime is responsible for the backend design
  - Airbus DS responsible for the frontend design

Demands of Future Telecom Missions

- Flexible processing platform
- In-orbit reprogrammable
- High processing power
- High data throughput
- Fast time to market
- Lower development costs

E.g., Mesh Processor providing connectivity between users.



AIRBUS DEFENCE & SPACE

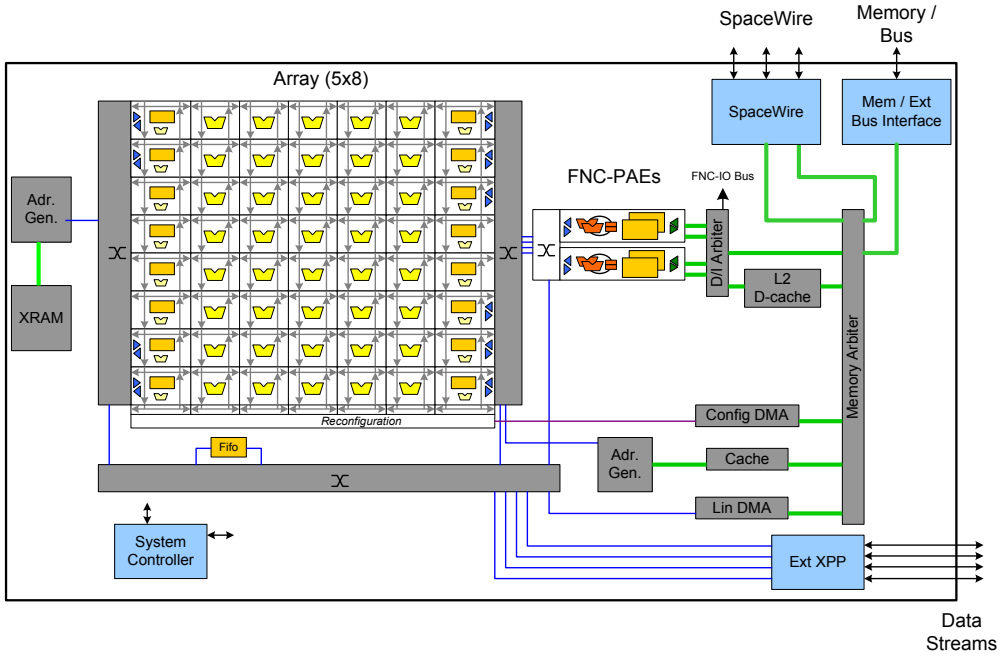
Typical Applications

- Regenerative Telecom Function
  - Requires reprogrammable hardware – ability to update/modify the processing algorithms.
  - Reconfigurable/ Adaptable MODEMs (DVB-RCS2, DVB-S2, etc.).
  - Software Radio and User-to-User applications.
  - Datapath processing (Cryption, Data-stream manipulation).

- High-end Data Processing (>1 GOps)
  - On-board Processing applications in ENS domain.
  - Data processing for high resolution sensors generating large quantities of data (e.g. HRWS-SAR).
  - Quick-look functionality
  - Applications requiring floating point support

Overview of HPDP Demo Chip

- Based on reprogrammable Array Processor IP.
- 40 PAEs and 2 FNCs.
- Floating point can be emulated.
- Provides >15 Gops at 300 MHz.
- High bandwidth IOs (4 channel with 1.6 Gbps each).
- High speed memory interface (~ 200 MByte/s).
- Control interface is SpW based (~ 200 Mbit/s)
- ~ 550 pads
- 5 clock domains in design
- Includes space relevant hardening at design level:
  - EDAC in the external memory interfaces
  - Scrubbing function for external memory
  - EDAC protection in on-chip memory
  - TMR-ed reset and clock logic
- Software Development Environment available and used extensively for algorithm evaluations (e.g., DVB-S TX and RX chains, Wavelet transformation).



AIRBUS DEFENCE & SPACE

Software Development Tools

For Array Programming
- Native Mapping Language Compiler (“NML”)
- Integrated placer & router (“XMAP”)
- Vectorizing C-Compiler

For FNC-PAE Programming
- GNU based C, C++ compiler
- Optimisation with Assembler

Simulation and Debugging
- Cycle accurate fast software simulator (“XSIM”)
- Supports multi-chip simulation
- Graphical visualiser and debugger (“XDBG/XVIS”)

Support Tools
- APIs for the specific SoC design and peripherals
- High and low level function libraries

Example Implementation: DVB-S Modulation

Modulator contains:

- Pseudo-Random-Scrambling
- Reed-Solomon Encoding RS(204,188)
- Time interleaving
- Convolutional coding
- Puncturing
- QPSK symbol mapping
- 4x oversampling and complex 36-tap roll-off filter
-

Performance meets typical requirements

- 25 MSyms/s output @ 100MHz [36 MHz Bandwidth]
- Fits in one HPDP

Similar results with much more complex DVB-S2 modulator

Overview of STM 65 Technology (1/2)

Manufacturing Point	Crolles 2 (F)
Wafer Size	12"
Technology Node	65nm
Gate oxide thickness	Double
Threshold Voltage	Triple
Metal Layers	Up to 7
Metallization Scheme	Cu Dual Damascene with Low K Integration
Lateral Isolation scheme	Shallow Trench

Technology Lifetime	> 10 years (target is 20years)
Digital Core Supply	1.2V
I/O Supply	1.8V, 2.5V, 3.3V
Density (High Speed Libraries)	640 Kgates/mm2
Density (High Density Libraries)	800 Kgates/mm2
Consumption	5.7 nW/MHz/Gate
Options	Analog, RF, eDRAM, Fuses
Radiation Endurance	Yes

Overview of STM 65 Technology (2/2)

Commercial	
Standard Cell	46
Memory Compilers	15
IO	50
PLLs	12
OTP/MTP/Fuse	10
eDRAM	2

Hardened	
Standard Cell	5
Memory Compilers	4 (Requests for memory cuts have to be made to ST Microelectronics)
IO	5
PLLs	1
OTP/MTP/Fuse	NA
eDRAM	NA

Synthesis & ATPG Results

- Airbus DS performed the Synthesis using commercial STM 65nm library (provided via CMP) resulting in 300 MHz (XPP) // 150 MHz (FNCs)

- Demo Chip top-level (including pads)
  - Area: 18.6 mm²
  - Gate Equiv: 8.9 M
  - Number of Instances: 2.16 M
  - Number of registers: 322670

- Demo Chip Core
  - Area: 12.2 mm²
  - Gate Equiv: 5.9 M
  - Number of Instances: 2.13 M
  - Number of registers: 320006

- Test-patter Generation
  - Number of scan-chains: ~ 210
  - Stuck-at Faults: 95.2 %
  - TDF Faults: 80 %
  - Number of Test-vectors: 11500

Formal Equivalence Results

- RTL vs Netlist (pre scan-insertion) :
  - Result : NO DIFFERENCES FOUND
  - Coverage: 94.5 %
  - Total Targets: 291731
  - Unsolved : 16146
  - Blackboxes: 1092

- Netlist (pre scan-insertion) vs Netlist (post scan-insertion)
  - Result : Designs are EQUIVALENT
  - Coverage: 100 %
  - Total Targets: 312353
  - Unsolved : 0
  - Blackboxes: 901

- Blackboxes include:
  - Pad cells (544)
  - Memories (353)
  - PLLs (4)
  - Designware components (e.g. Multipliers/FIFO-controller are not understood by the FormalPro)

Experiences with commercial STM 65nm library

- STM65nm commercial library is provided via CMP – No direct contact with STM

- Long latency until a complete library is delivered
  - Standard cell June 2012
  - Memories August 2012
  - PLL Spring 2013
  - ➢ Recommendation: PLL has to be part of the design kit in the final library. [Confirmed to be the case for the rad-hard STM65 library]

- Memories have to be explicitly requested from STM // Memory compiler is not provided.

- STM library supports only Synopsys flow // Mentor Graphics is not supported.

Experiences at Airbus DS

Scan-Insertion

- Large run-time in the default configuration. Can be significantly reduced only when relaxed SDC is used.
- The Runtime Debug system complicated the scan-insertion step:
  – Multiple scan enables in design.
  – Complex scan stitching due to the special scan-connections required. The tool (Synopsys DFT Compiler) did not produce warnings or error, log file was clean.

Equivalence Check

- Mentor FormalPro was used
- Insufficient support for SystemVerilog constructs and Synopsys DesignWare macros
- Sufficient schedule delay due to tool problem corrections (leading to wait for new tool version)

Experiences at ISD – Synthesis using Rad-hard STM65 (1/2)

Hardening Approach

- Replace all the FFs with hardened FFs
- Replace all the clock drivers with hardened clock drivers
- Use a hardened PLL
- Use hardened memory cuts
- Other hardening techniques to be used in the next phases of the flow

The slowest libraries have been used just to be in the safe side

- Worst case devices
- Vdd 1.1V
- Junction temperature 125C
- Device performances like after 20 yrs of operation

Timing constraints

- The device has been successfully synthesized on the rad-hard STM65 for a 200 MHz system clock
- Attempts to synthesize at 250 MHz system clock will be also performed

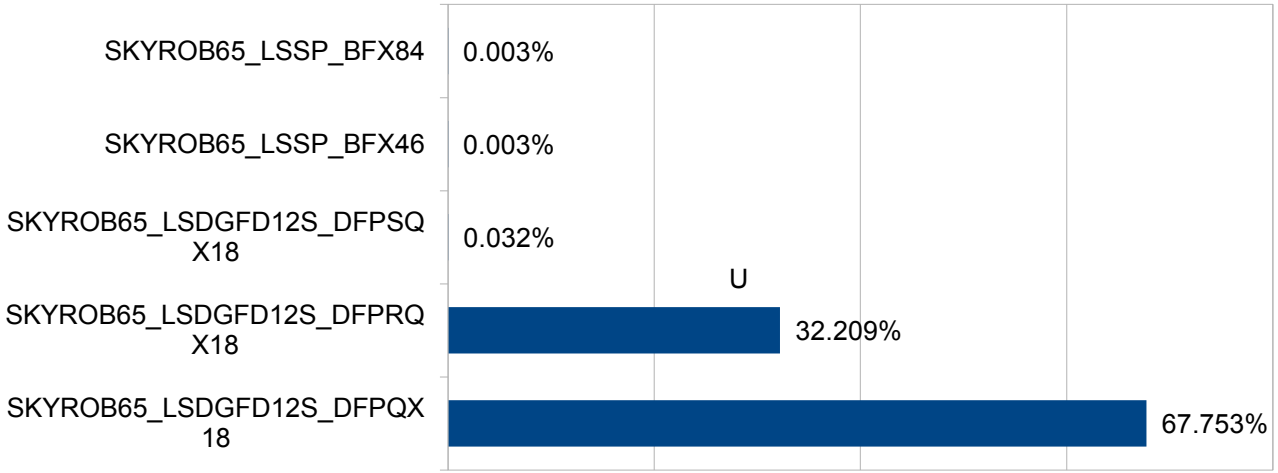
ISD has full access to the design environment via Atmel and STM

AIRBUS DEFENCE & SPACE

Experiences at ISD – Synthesis using Rad-hard STM65 (2/2)

Some results

- # cells in the design: ~2M
- # FF in the design: ~ 320K
- Total area (with memories and PLLs, without Pads) ~22 mm^2
- Hardened FF usage



Open issues

- At this stage it is not clear if the demo chip will use classical wire bonding pads (double raw) or bumps. Obviously this decision influences the final size of the demonstrator.

AIRBUS DEFENCE & SPACE

Next-Steps

Next Steps
- Layout completion (ISD)
- ATPG (ISD)
- Post-layout Verification (Airbus)
- ASIC tape out (Airbus/ISD)
- Samples manufacturing (ST) & Packaging

Schedule
- The target is to be ready for tape-out late 2014 – early 2015.