ESA Summary / DSP Roadmap Update

R. Trautner, TEC-EDP

ESA Summary & DSP Roadmap Update

- Summary: Ongoing ASIC and IP developments
- Summary: Status of COTS DSP based computers
- NGDSP: Recovery options based on new IP
- Complementarity & Updated ESA DSP Roadmap
- Discussion & AOB

Summary: Ongoing ASIC and IP Developments

Scalable Sensor Data Processor, DSP and NoC IP

- SSDP prototypes expected to be available in late 2015
- SSDP evaluation boards expected to be available around the same time
  - commercially from TASE
  - for specific work, on loan from ESA
  - SDE licensable from RECORE Systems b.v.
- SSDP FM contract: funding approved, proposal expected soon, contract start expected Q4 2014 (in parallel to prototype development contract) pending successful negotiations. If all goes well FMs might be available end 2016.
- Radiation hardened fixed point DSP IP, NoC IP, bridges & interfaces as well as SDE are commercially available from RECORE Systems b.v.
- ESA making efforts for developing a floating point version of Xentium together with RECORE Systems b.v.

Summary: Status of COTS DSP based computers

COTS DSP based computers

- 2 designs have been elaborated by industry: Scalable Hi-P design, dual processor HPPDSP design
- Feasibility, high performance and scalable reliability / availability have been demonstrated
- Demonstrator with TRL 4/5 available; TRL ~6 in key areas (radiation hardness of DSP, error mitigation tested and characterized)
- Technology is considered mature to be adopted by projects. Key problem to overcome is now conservatism of project teams / advantage of flight heritage of PowerPC based hardware. However, the power efficiency, scalability and growth potential of the concept are considered key advantages vis-à-vis competition.
- ESA making efforts to find opportunities for in-flight demonstration to ease project adoption

Summary: Status of COTS DSP based computers

COTS DSP based computers

- **Hi-P deliverables include SmartIO / EGSE rack, 3 Hi-P processing modules (PMs)**
- It is currently intended to provide the Hi-P SmartIO/EGSE rack back to AB D&S on loan, to support their own development work
- Part of the PMs may also be provided back to CGS / AB D&S on loan basis

- **However, some HW & SW will be kept at ESTEC and provided to potential future users on temporal loan basis for assessment and evaluation:**
  - **Hi-P Processing module (PM) – from ESA**
  - **Hi-P Documentation (API, programming, etc) from ESA (deliverables from contract)**
  - **TI 6727 SDE to be licensed from commercial sources**
  - **User support from CGS (details TBD)**

- **Interested projects / parties shall contact R. Trautner, ESA/TEC-EDP**

NGDSP: Recovery options based on new IP - 1

Next Generation DSP (NGDSP): sudden death, re-animation ongoing …

- NGDSP history: 7 years in 5 bullets
  - Requirements for new floating point DSP ASIC have been consolidated from 2007
  - Tradeoff study performed: Atmel Diopsis ruled out, TI6727 IP not licensable, ADI21469 selected
  - ADI/ESA/Atmel licensing talks failed: IP license is (and remains) unaffordable
  - Previously already approved 600k ECI4 funding for DSM feasibility study then re-allocated for DDR2/3 IP development - ☹ ☺
  - Due to delays some requirements from 2007 outdated: ESA now assumes 1 GFLOP (in 2020 ?) theor. peak performance insufficient, should be at least > 3..4 GFLOP (TBC); requirements review needed.

- In parallel 2008-2013: MPPB development successful, DARE+ Application ASIC OK, SSDP funded and kicked off, SSDP FM funding ready, NGAPP performed, positive assessments

=> Re-orientation of development plans for future European floating point DSP was required: feasible, affordable, higher performance, good user acceptance, non-ITAR.

NGDSP: Recovery options based on new IP - 2

Next Generation DSP: A new feasible approach

- In parallel 2008-2013: MPPB successful, DARE+ Application ASIC OK, SSDP funded and kicked off, SSDP FM funding ready, NGAPP performed, positive assessments
- 2012/2013: PhD work at TU Twente, prototype of IEEE754 compliant floating point Xentium DSP version demonstrated (RECORE involved, ESA observer)
- 2014: IP licensing discussions with RECORE, license proposal was received, acceptable and affordable licensing scheme is within reach
- 2014: TRP proposal for CCN to RECORE contract on **floating point Xentium development and incorporation of IP in ESA IP portfolio** compiled; early in 2014 not yet accepted due to NL geo-return issues, but will be presented to AC again in Oct or Dec 2014 for implementation in 2015 => **needs delegation (and your !) support**
- With the envisaged new IP, scalable multi-GFLOP DSP is feasible, LEONx/SSDP/NGDSP family approach (IP + software) appears attractive => merging of previously separated development routes (NGDSP/massively parallel processor development).

=> one of the points for open discussion later today

Other activities – early preparations

In addition to presented efforts, a number of potential future activities are being proposed, including

- Discussions on floating point DSP core development by NXP (if funded, architecture will be complementary to any potential RECORE developments)
- Austrian ASAP programme: activity proposal for DSP software developments (decisions late 2014, TBC)
- ESA – Bulgaria programme 2015-2018: DSP-related topics have been proposed, for selection in 2015, TBC.
- Next TRP cycle will see several DSP based proposals: new NGDSP, hardware, software
- Other opportunities as they come along

⇒ **Continued effort to put activities in place that cover identified needs and address expected future opportunities**

⇒ **Support by industry via national delegations is key for funding becoming available**

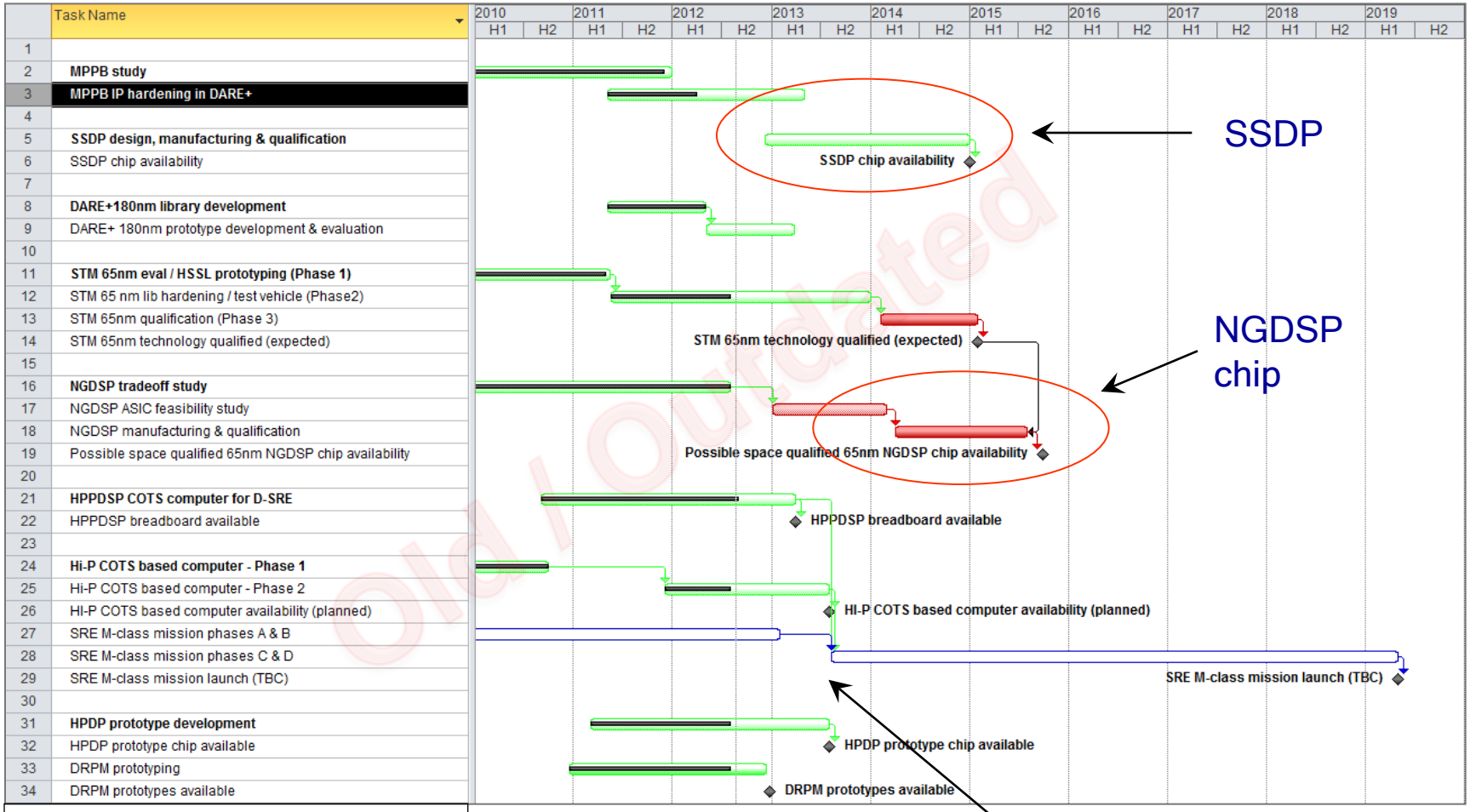
Complementarity of activities

Application / Activity	Telecom Data Streaming Fixed-point	Small DPUs and Instruments Fixed-point	High Performance DPUs Floating point	
	HI-REL	HI-REL	COTS	HI-REL
HPDP ASIC	X			
SSDP ASIC		X		
Hi-P HPPDSP			X	
NGDSP ASIC*				X

* includes related IP developments

Green = development ongoing; red = need identified

Previous ESA DSP Roadmap - 2012



Updated ESA DSP Roadmap - 2014

	Task Name
1	**MPPB study**
2	**MPPB IP hardening in DARE+**
3	Floating point Xentium DSP development
4	Floating point Xentium DSP IP available
5	
6	**SSDP design, manufacturing & qualification**
7	SSDP prototype chip availability
8	SSDP qualification
9	SSDP FM availability
10	
11	**MPPB/SSDP architecture & SW eval**
12	SSDP IP assessment complete
13	
14	**NGAPP**
15	DPU architectural design based on SSDP available
16	SSDP DPU board development
17	SSDP Software (library / OS) developments
18	SSDP DPU board and SW available
19	
20	**DARE+180nm library development**
21	DARE+ 180nm XD prototype development & evaluation
22	
23	**HPDP**
24	HPDP prototype chip available
25	
26	**DSM 65nm technology development**
27	DSM Phase2.0 / CNES (ESCC eval of lib)
28	DSM Phase2.1 / ESA (incl. initial deployment)
29	DSM Phase2.2 / ESA contract (HSSL IP+char+CAD)
30	DSM Phase3.0 / ESA (submission of C65SPACE to EPPL)
31	DSM Flip Chip / ESA
32	
33	**NGDSP tradeoff study**
34	Manycore NGDSP ASIC pre-development (IP)
35	Manycore NGDSP prototyping
36	Manycore NGDSP qualification
37	Possible space qualified 65nm NGDSP chip availability
38	
39	**HPPDSP COTS computer for D-SRE**
40	HPPDSP breadboard available
41	
42	**Hi-P COTS based computer - Phase 1**
43	Hi-P COTS based computer - Phase 2
44	HI-P COTS based computer availability
45	

New FIP IP development

SSDP HW/ SW devel.

Funding allocated

No funding allocated yet

New NGDSP attempt with new IP:
- ECI
- TRP
- GSTP