ESA Workshop on Avionics Data, Control and Software Systems (ADCSS)

Multi-Core Processors for Space Applications (MCPSA)

25-27 October 2011, ESTEC

Evaluation of the Multi-Core Technology for Demanding Space Applications

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MUSE – Evaluation of the MULti-Core Architecture for tracking SEnsor in Space

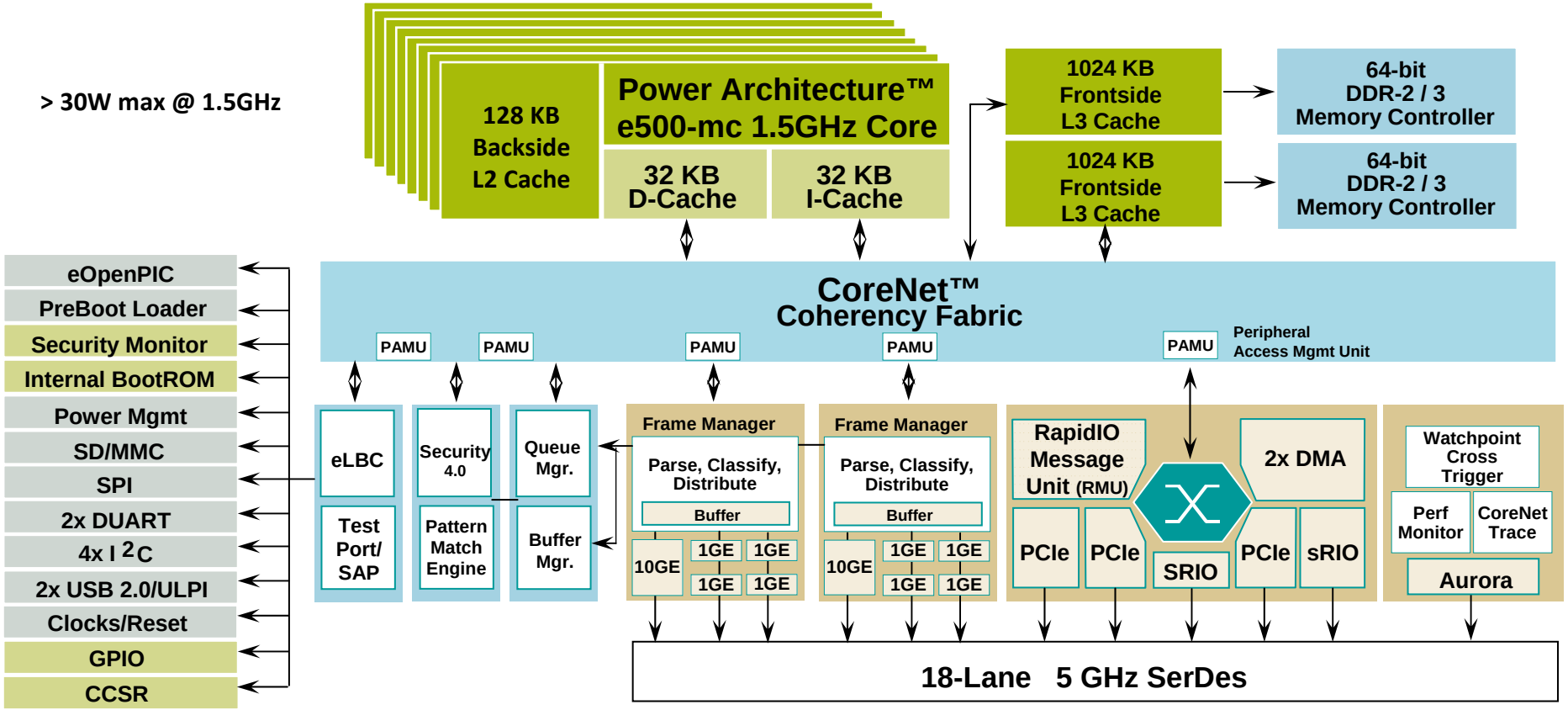
Objectives of the project:

- target technology evaluation
- requirement definition
- specification of system architecture (incl. FDIR)
- software architecture and algorithms
- hardware implementation and system integration
- setup of demonstration and evaluation scenario
- system evaluation

Criteria for Processor Selection:

- ✓ multi-core (8-16 cores)
- ✓ embedded design (SoC)
- ✓ performance (on-chip interconnect, FPU)
- ✓ memory interface
- ✓ I/O interfaces (standard, high speed)
- ✓ SOI technology
- ✓ power dissipation (mW/MIPS)
- ✓ power save functions
- ✓ availability (long term, ITAR free)

➢ **PowerPC Multi-Core Processor QorIQ P4080**



Block diagram of P4080

freescale™

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Technology	**8 core multi-core processor, 45nm SOI process clock frequency 1,5 GHz, 1295-pin FBGA**
Cache	**1st Level: 32 Kbyte code, 32 Kbyte data 2nd Level: 2 x 128 Kbyte back side 3rd Level: 2 x 1 Mbyte with ECC front side**
CoreNet Switch Fabric	**cache-coherent crossbar interconnect**
Memory Management	**MMU for each core PAMU for the I/O channels**
Main Memory	**2 separate memory controllers for DDR2/3 SDRAM 32/64 bit data bus with ECC, up to 1.6 GHz clock**
High Speed Interconnect	**3 PCI express® 2.0 controller 2 serial RapidIO controller**
Ethernet	**8 x 10/100/1000 Ethernet controller 2 x 10GE controller classification/policing H/W queuing, policing, buffer management, checksum offload, QoS, lossless flow control, IEEE® 1588, SGMII/XAUI**
Data Path Acceleration	**10Gb/s IP forwarding, 64B packets SEC 4.0: 10Gb/s IPSec, 1456B packets PME 2.0: 10Gb/s IDS, 1456B packets**

Main features of the P4080 Processor

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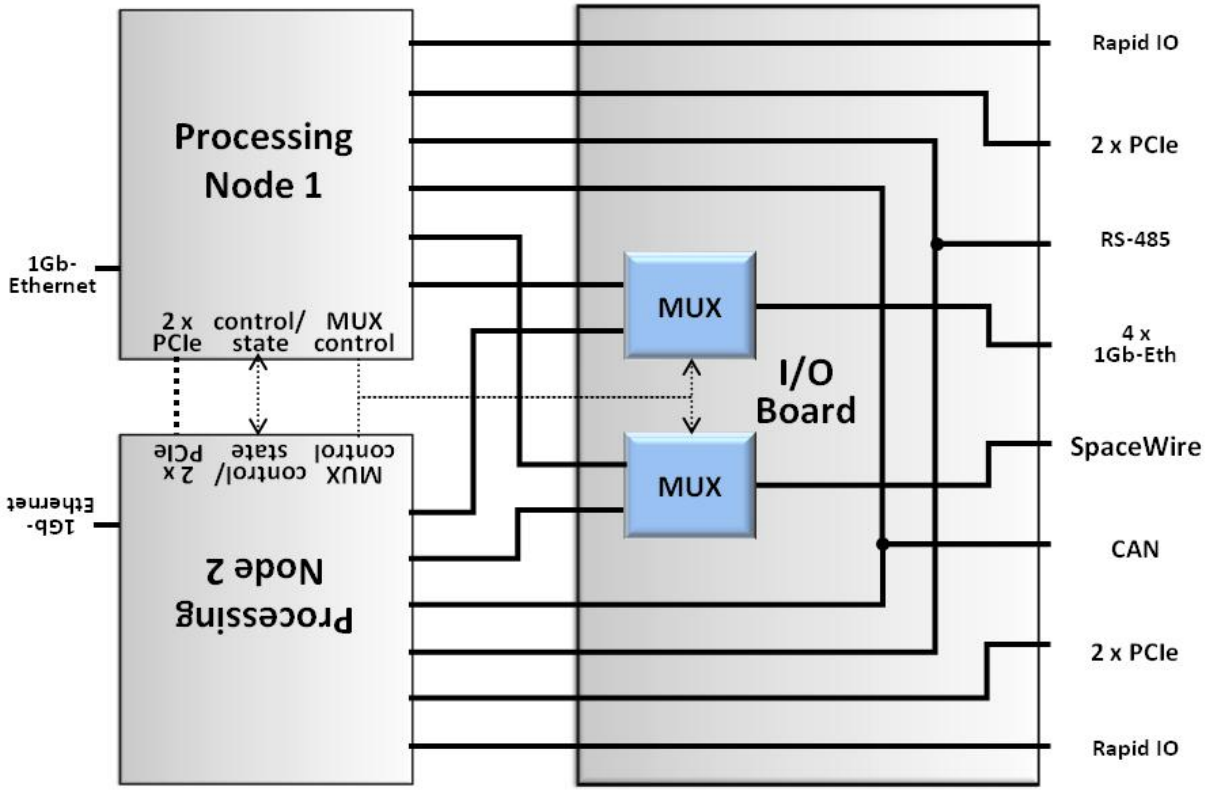

Redundancy and I/O Structure of the MUSE High Performance Processing Node (HPPN)

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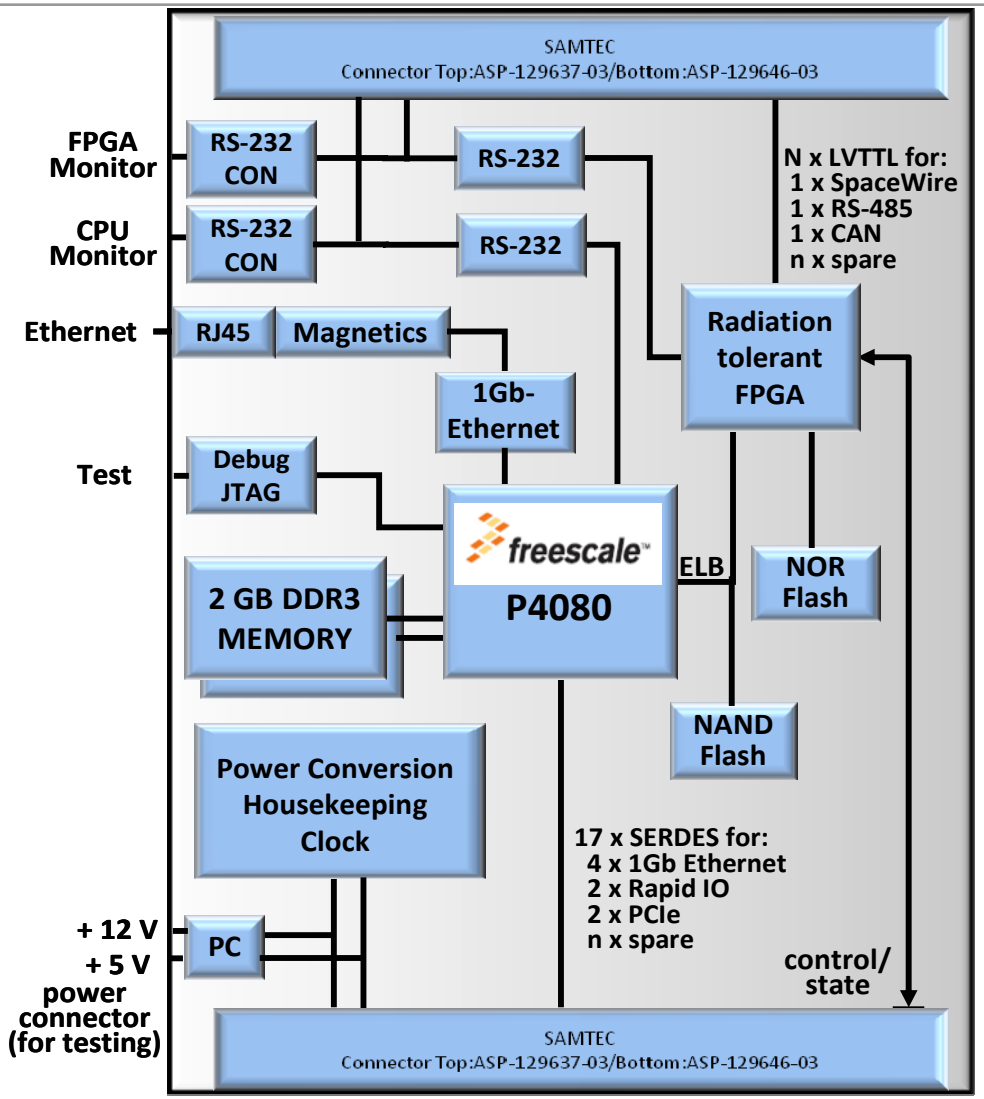
Hardware Structure



MUSE Processor Board

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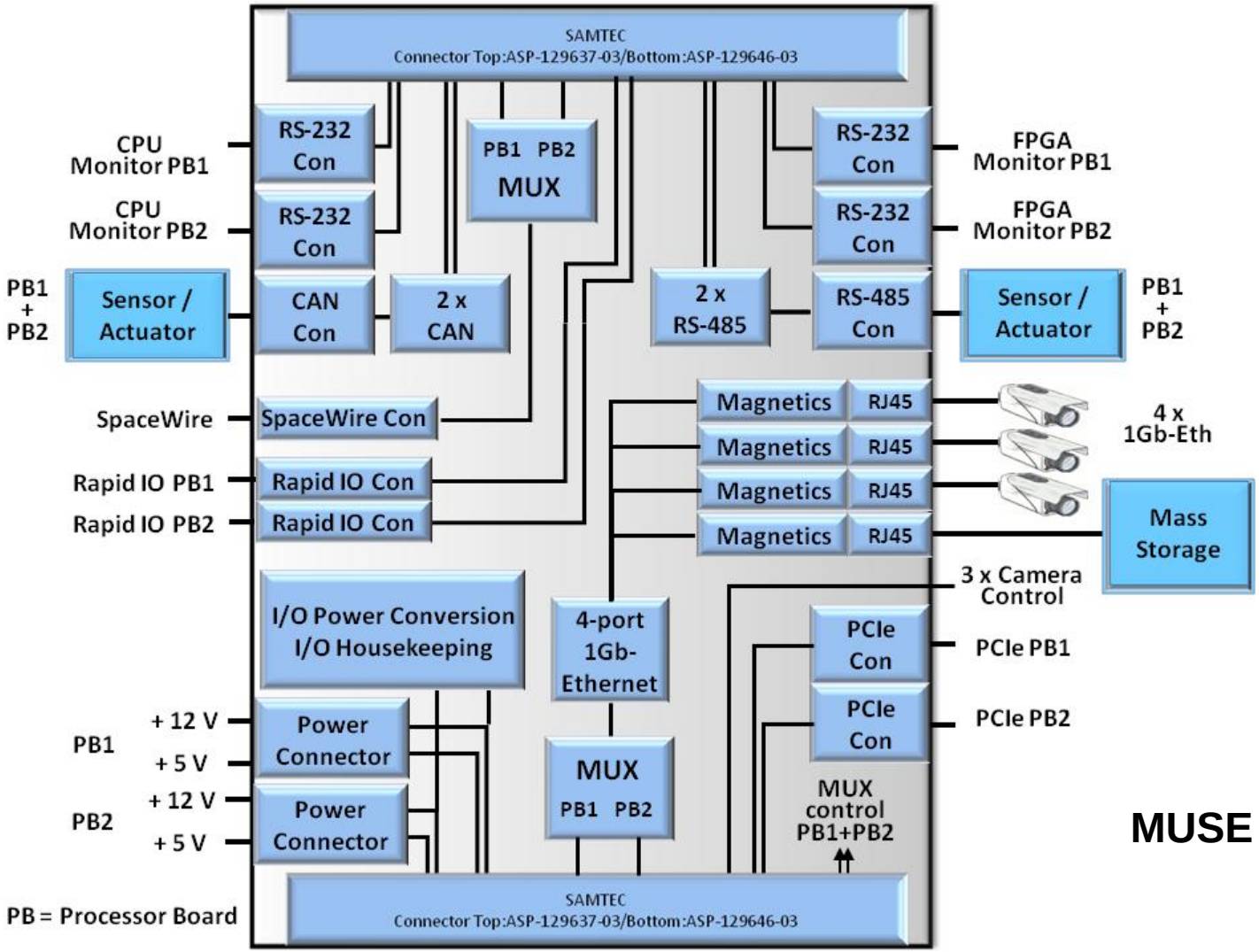
Hardware Structure



MUSE I/O Board

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Error Detection and Error Handling

- System level → 1oo2d system
- Multi-Core P4080 → redundant computations
- Caches → EDC (L3) and parity (L1, L2)
- Node memory → redundant memory banks with EDC
- Flash memory → RAD Hard, redundant copies with CRC
- FPGA → radiation tolerant (TMR)
- Control output → synchronizing voter (FPGA)
- Hardware watch-dog for unspecific errors in HW or SW
- Monitoring of all supply voltages, currents and temperatures
- Default error handling by node RESET and node-switch

FDIR Concept (Software)

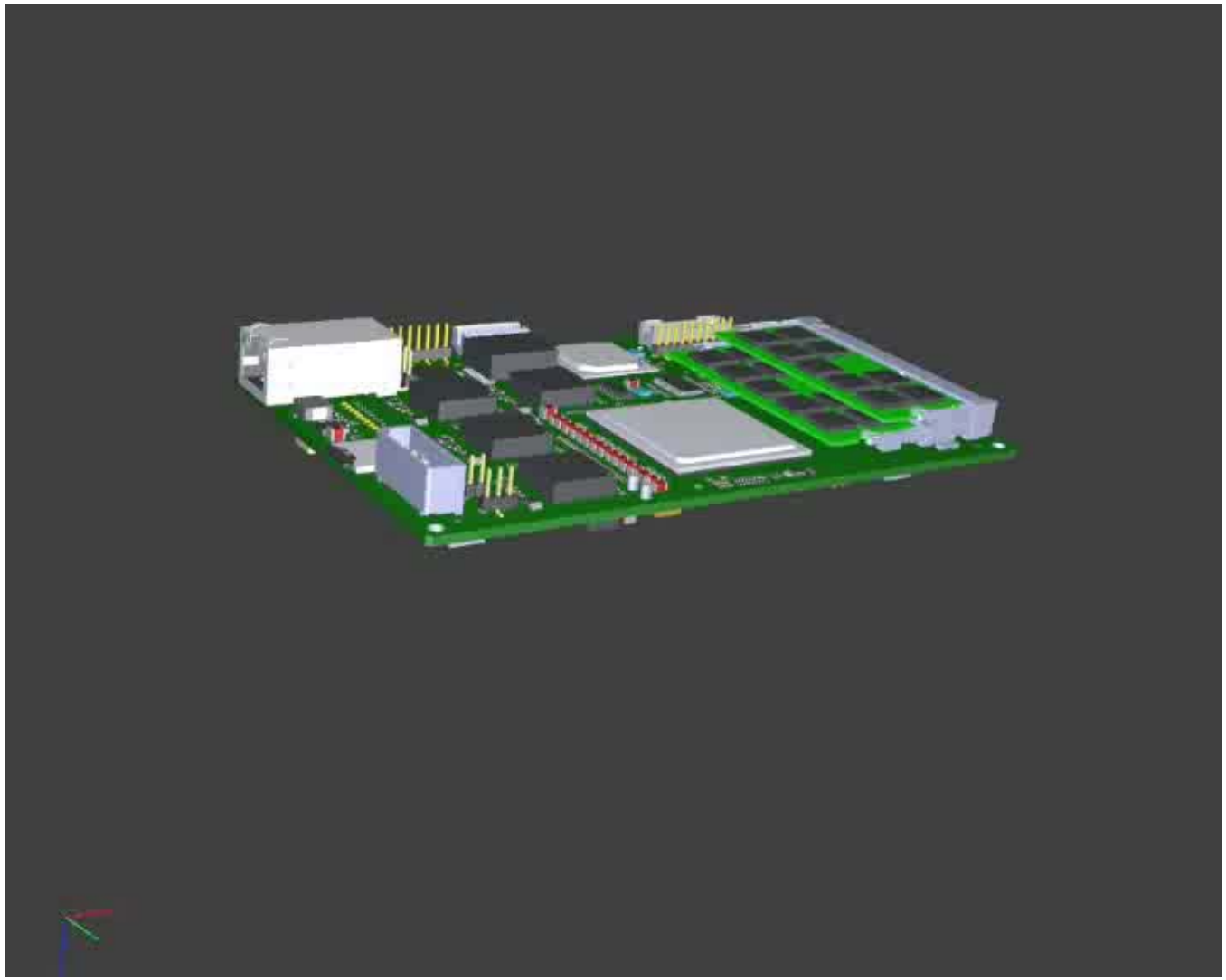
- Process- and task level redundancy:
  - Compute intensive: no redundancy (plausibility check)
  - Mission critical: dual mode redundancy (compare and restart)
  - Mission critical + real time: triple mode redundancy (synchronized voting)

- Diagnoses tasks for self checking of the nodes

- Hardware watchdog for heartbeat control:
  - Diagnoses- and application tasks → supervisor process (replicated)
  - Supervisor process → re-triggers hardware watchdog (TMR FPGA logic)

- Dual node concept (Worker/Monitor)
  - Software RESET and node-switch for all detected errors not handled locally
  - Outage time can be optimized by continuously sending actual state information to the monitor node (task-specific)

Assembly



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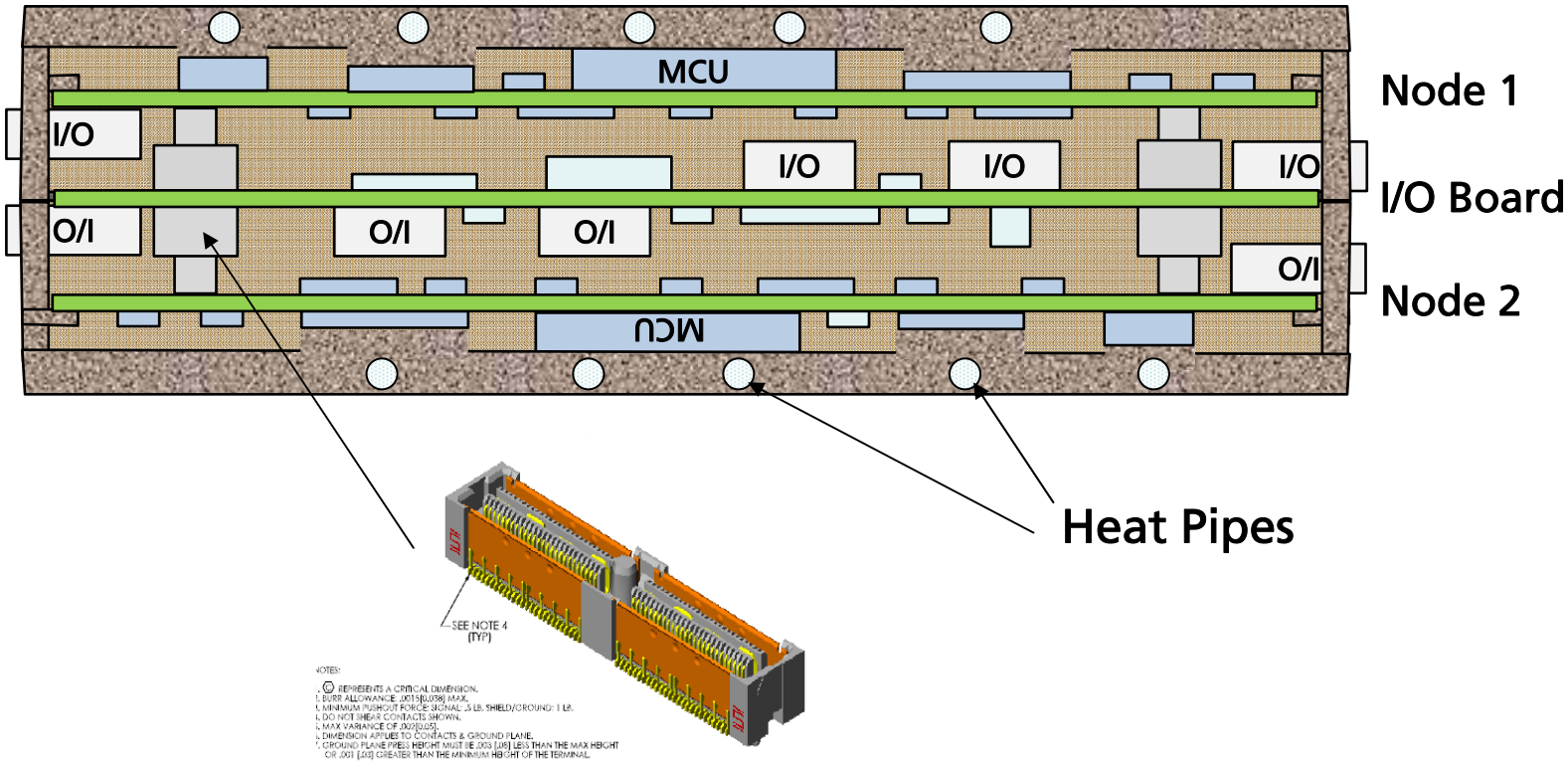
Assembly



Stack-Down Configuration

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Thank you for your attention!

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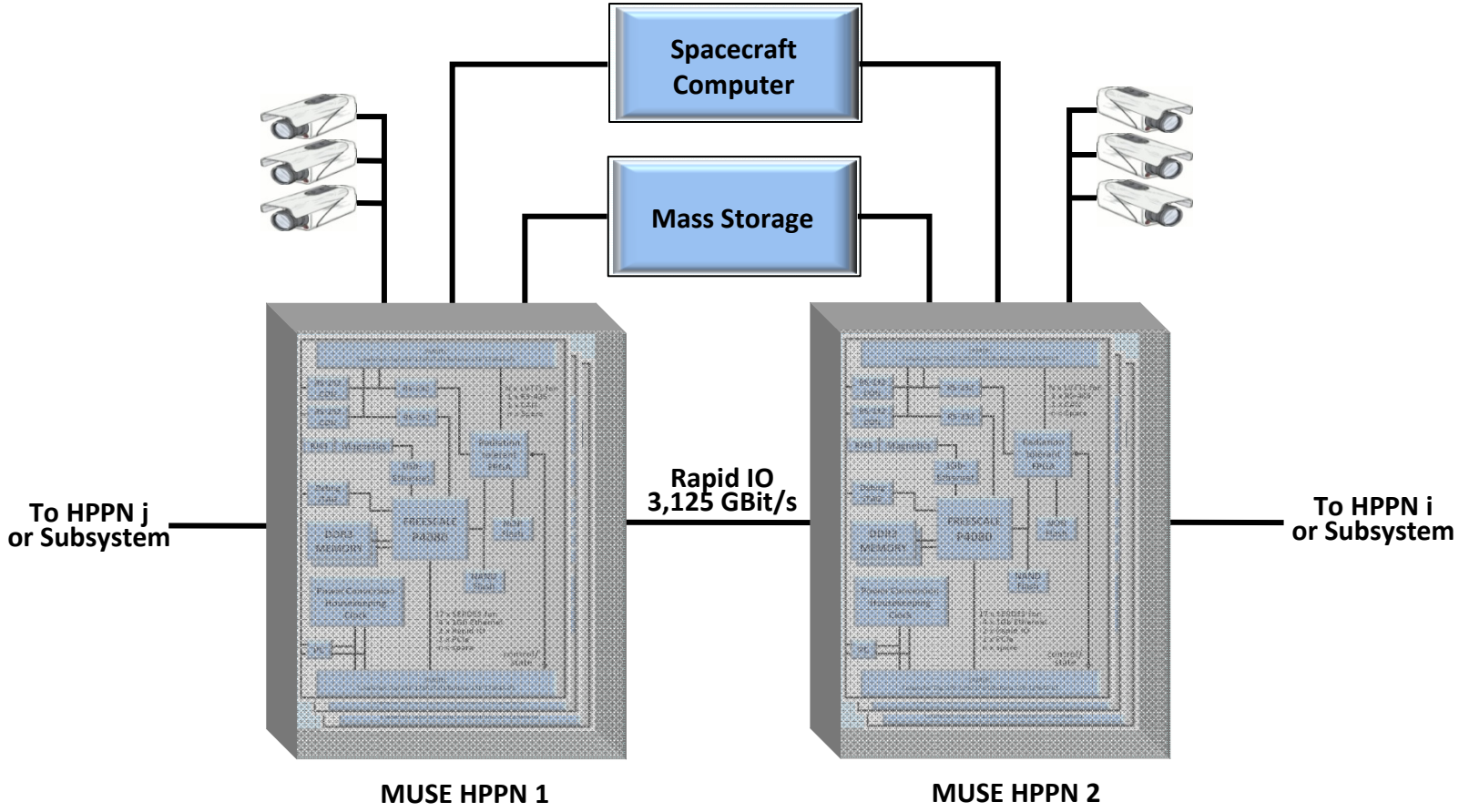
System Architecture



Scalability and Integration into the Communication Infrastructure of a Satellite

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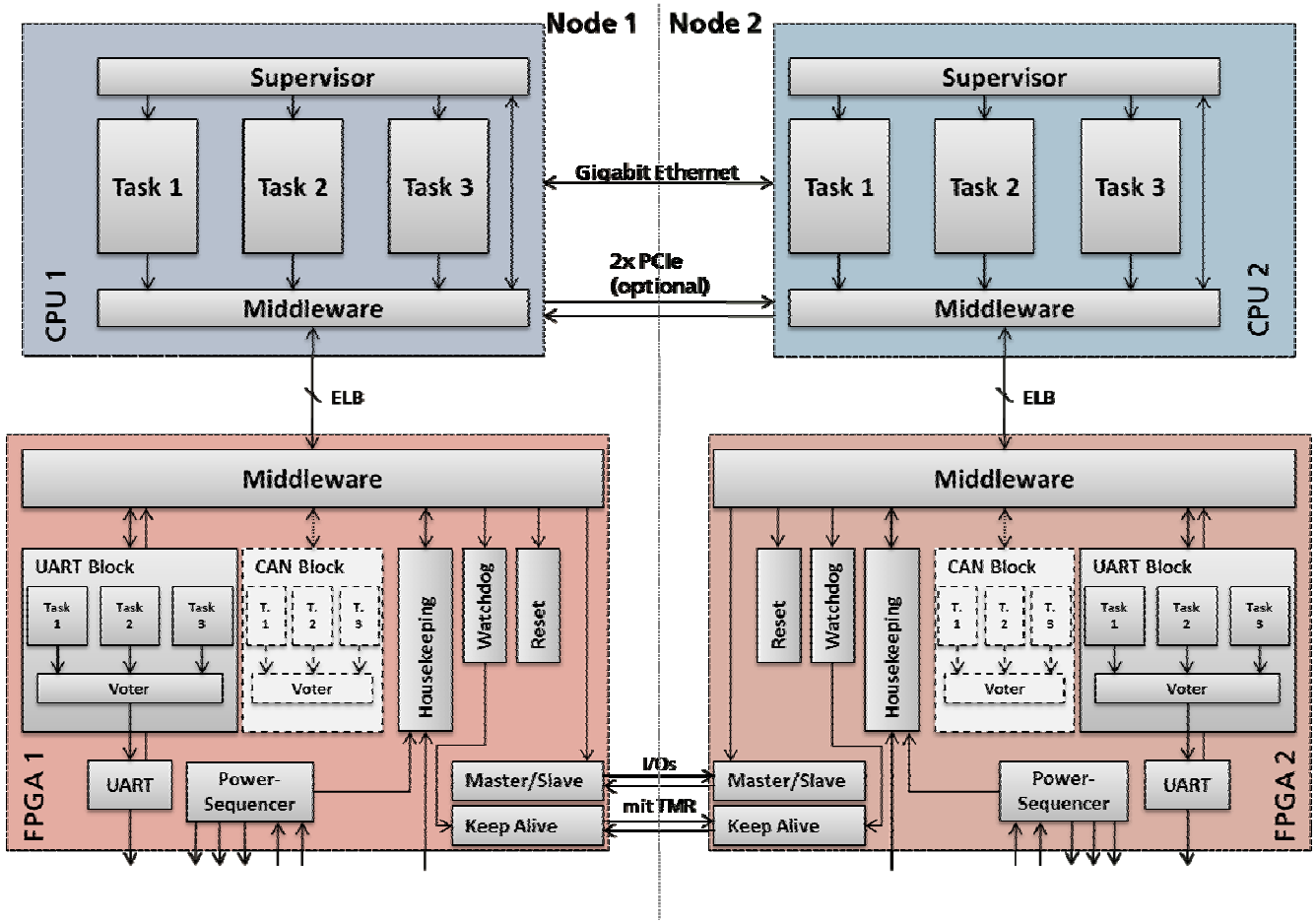
- Microsemi (Actel) A3PE3000L
  - 3 Mio. System gates in 75.264 VersaTiles
  - 341 single-ended I/Os / 168 differential I/Os
  - Flash-based configuration memory
  - Low power consumption
- Pin and design compatible space version available (RT3PE3000L)
- SEU immune Flash memory
- Radiation hard by design (TMR syntheses by design software)

FPGA Structure



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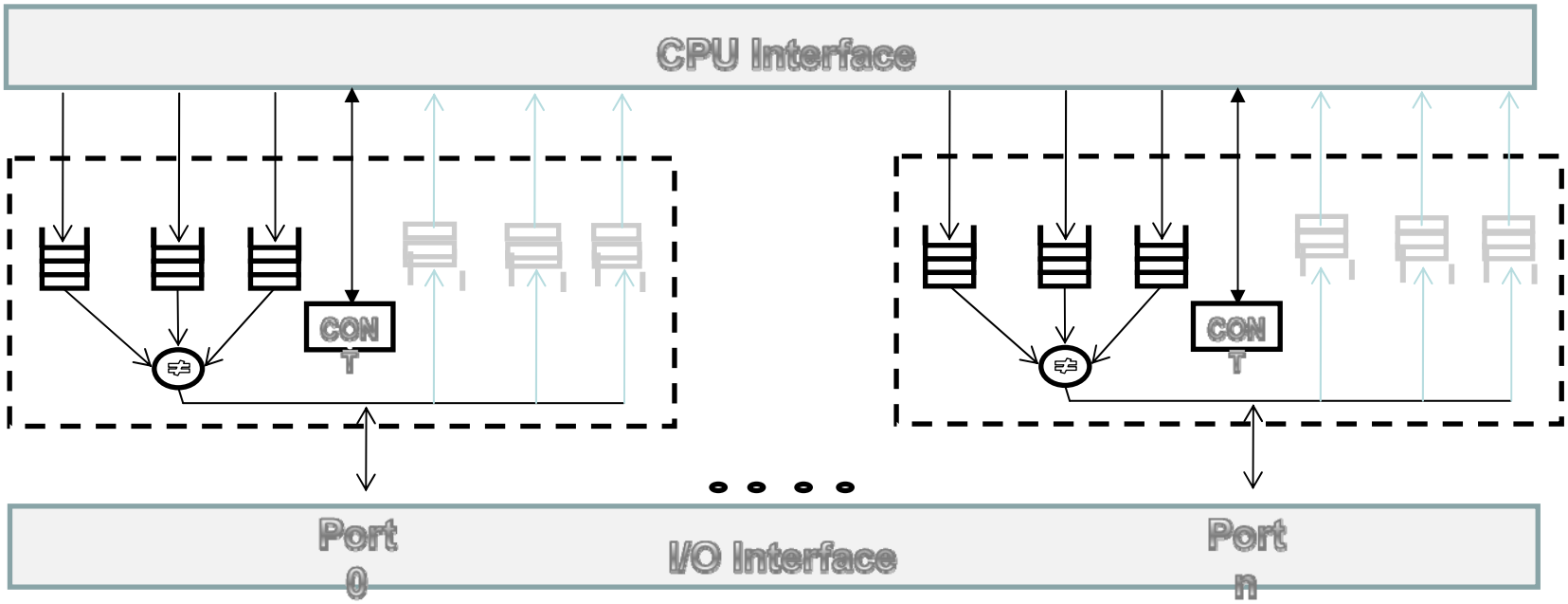

Synchronizing Voter (FPGA Hardware)

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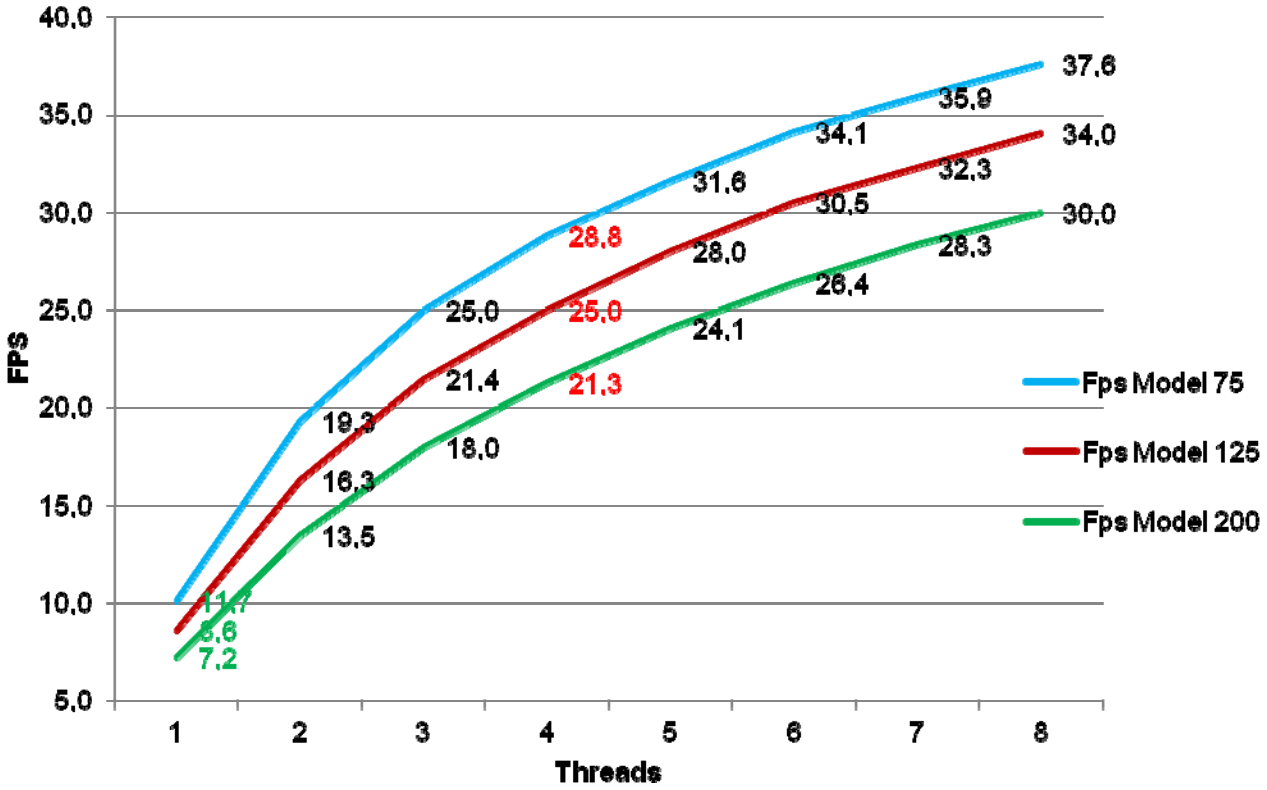

Scalability of Object Detection on P4080

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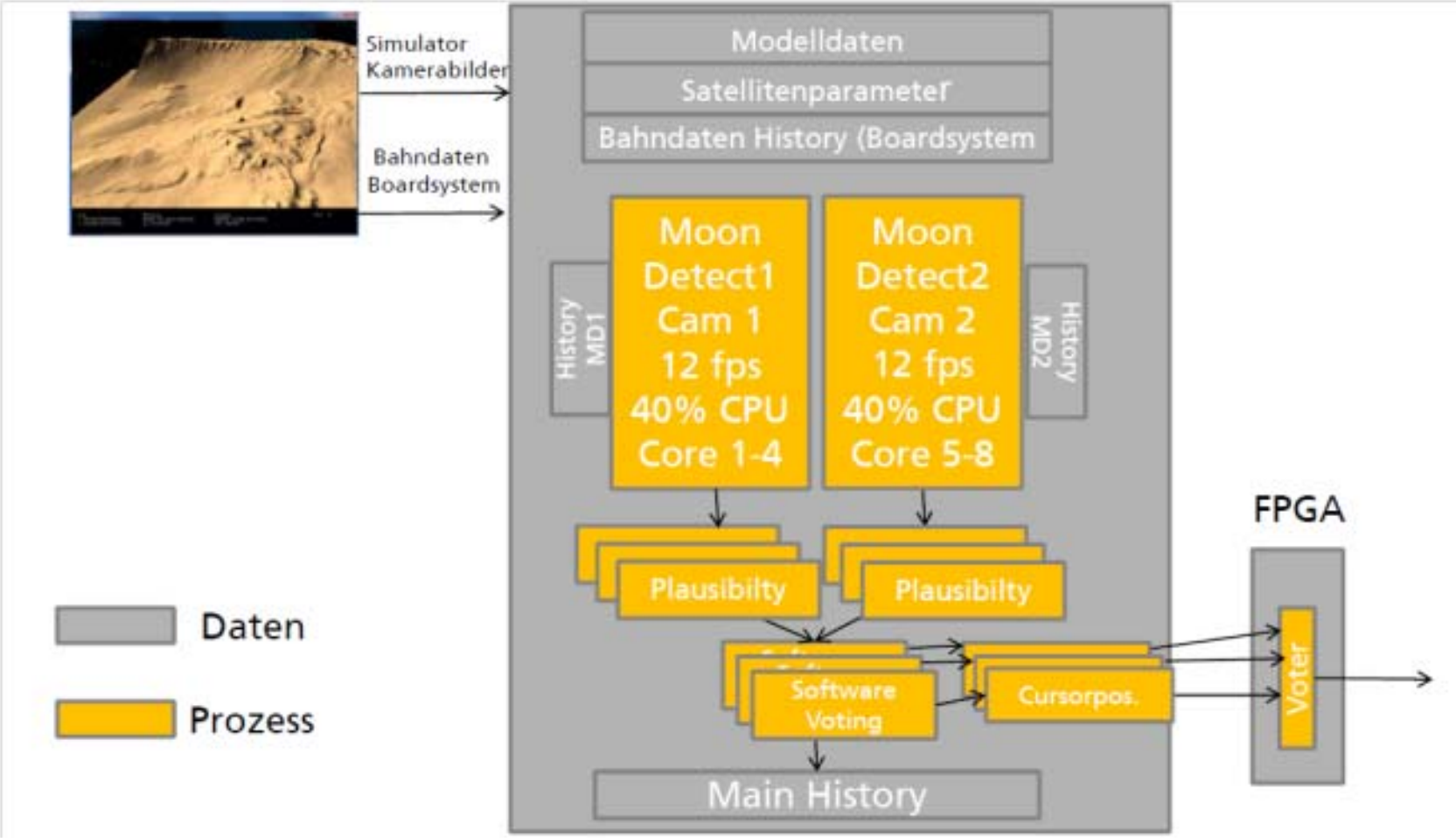
Software Structure



Software Block Diagram

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