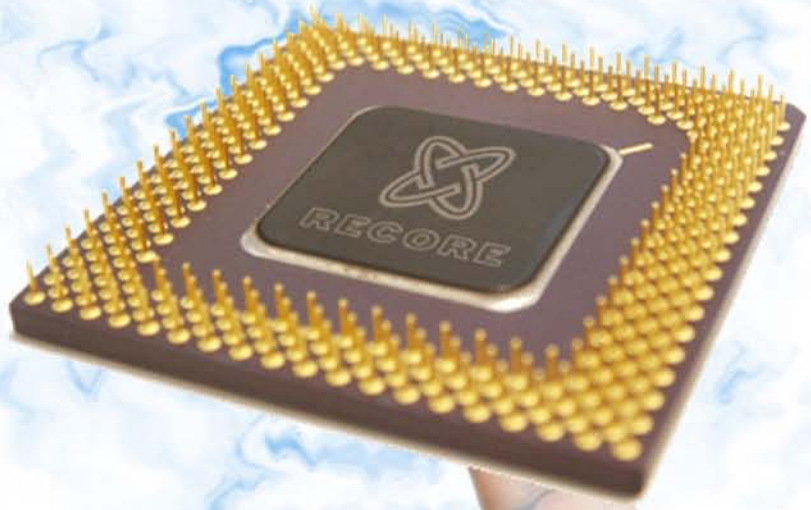
27 October 2011

Reconfigurable multi-core DSP architecture for Space Applications



Massively Parallel Processor Breadboarding

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Outline

- MPPB architecture
- Xentium® software development tools
- MPPB software and benchmarking
- MPPB ASIC migration

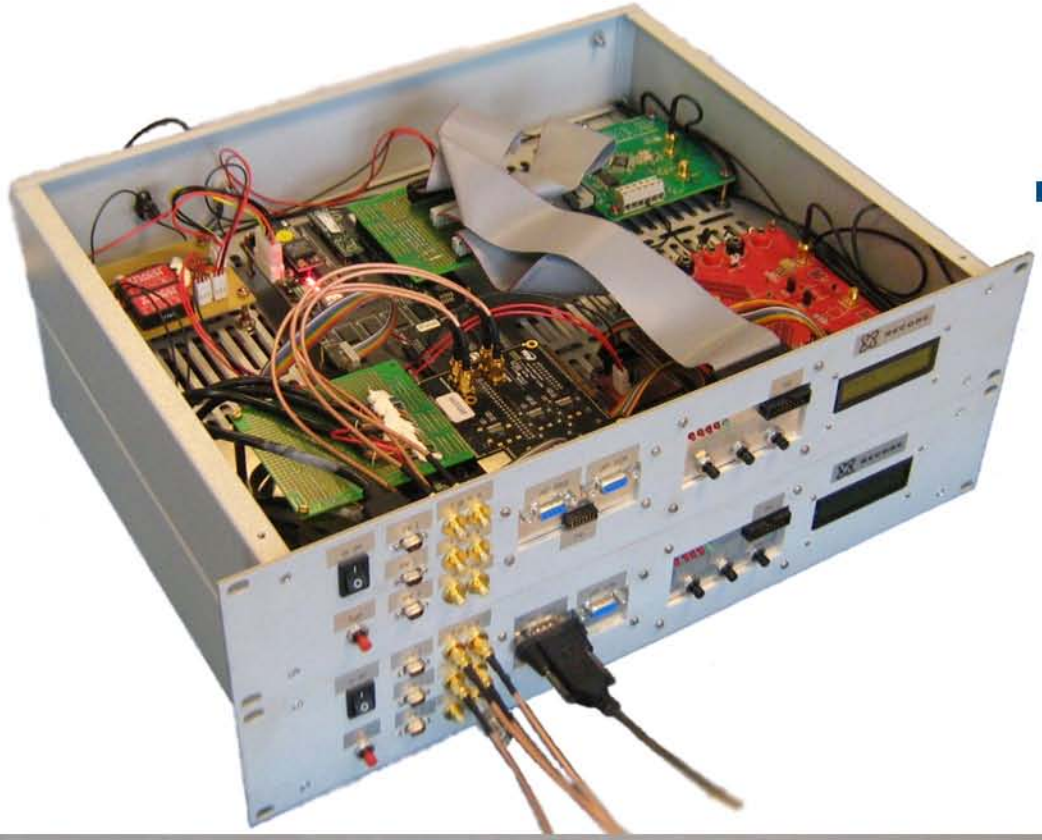
- R&D on multi-core DSP
- Next steps

Massively Parallel Processor Breadboarding

Multi-core SoC benchmarking of Recore's reconfigurable DSP technology in FPGA prototype for space applications

- ESA TRP activities
  - MPPB
    - Feasibility/benchmark study for next generation multi-core DSP for space applications (Jan '09 – Nov '11)
  - DARE+
    - Rad.-hard prototyping of MPPB elements in DARE180 (Jul '11 – Jun '13)
- ESA NPI activity
  - Development of methodologies and tools for predictable, real-time LEON/DSP-based embedded systems (2011 – 2013)
    - Performed by Politecnico di Milano (Polimi)
    - Supported by Recore Systems / MPPB

MPPB Box

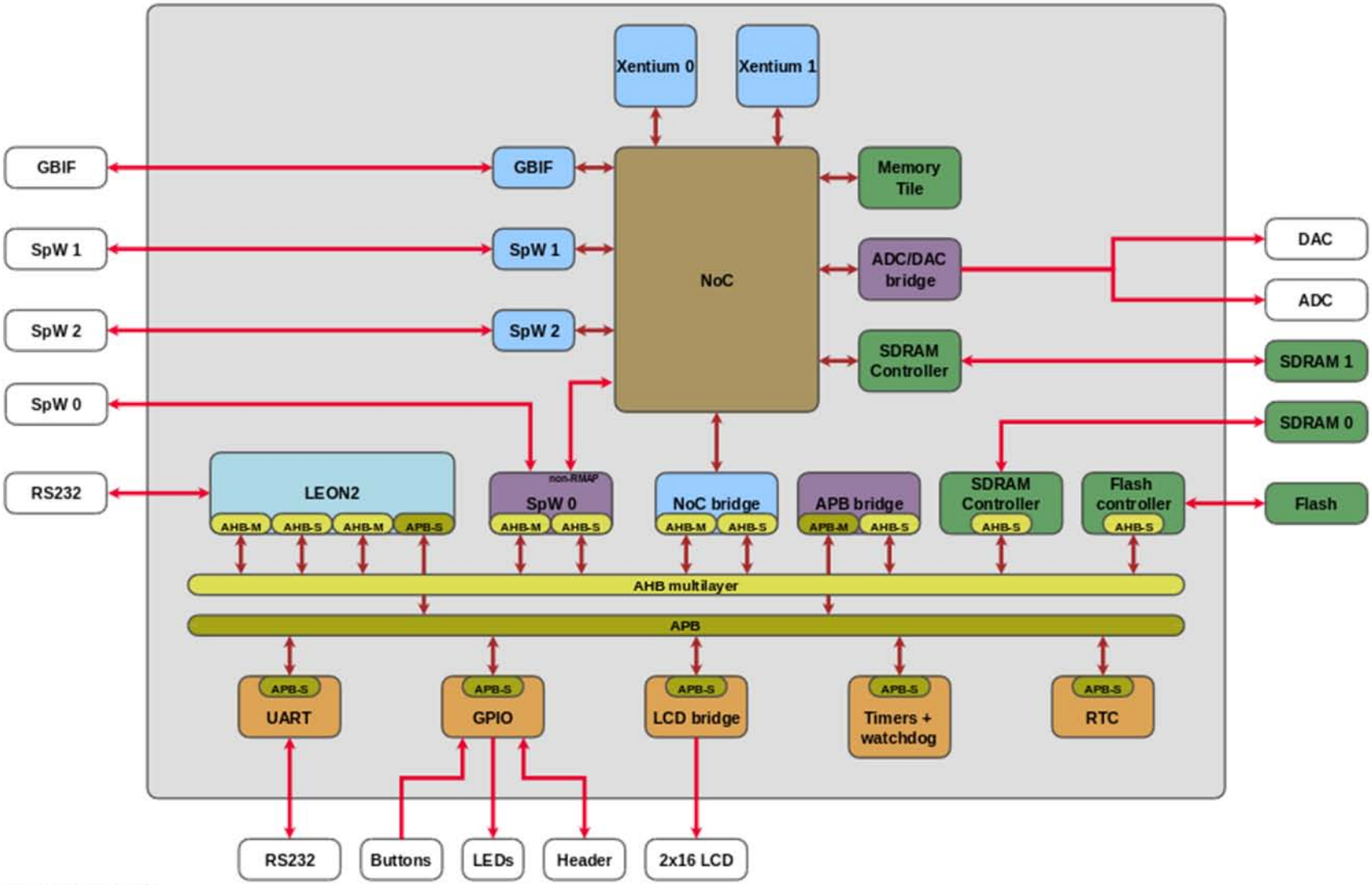


- 3 MPPB boxes delivered
  - ESA
  - ASTRIUM
    - NGDSP tradeoff study
  - Polimi
    - NPI activity

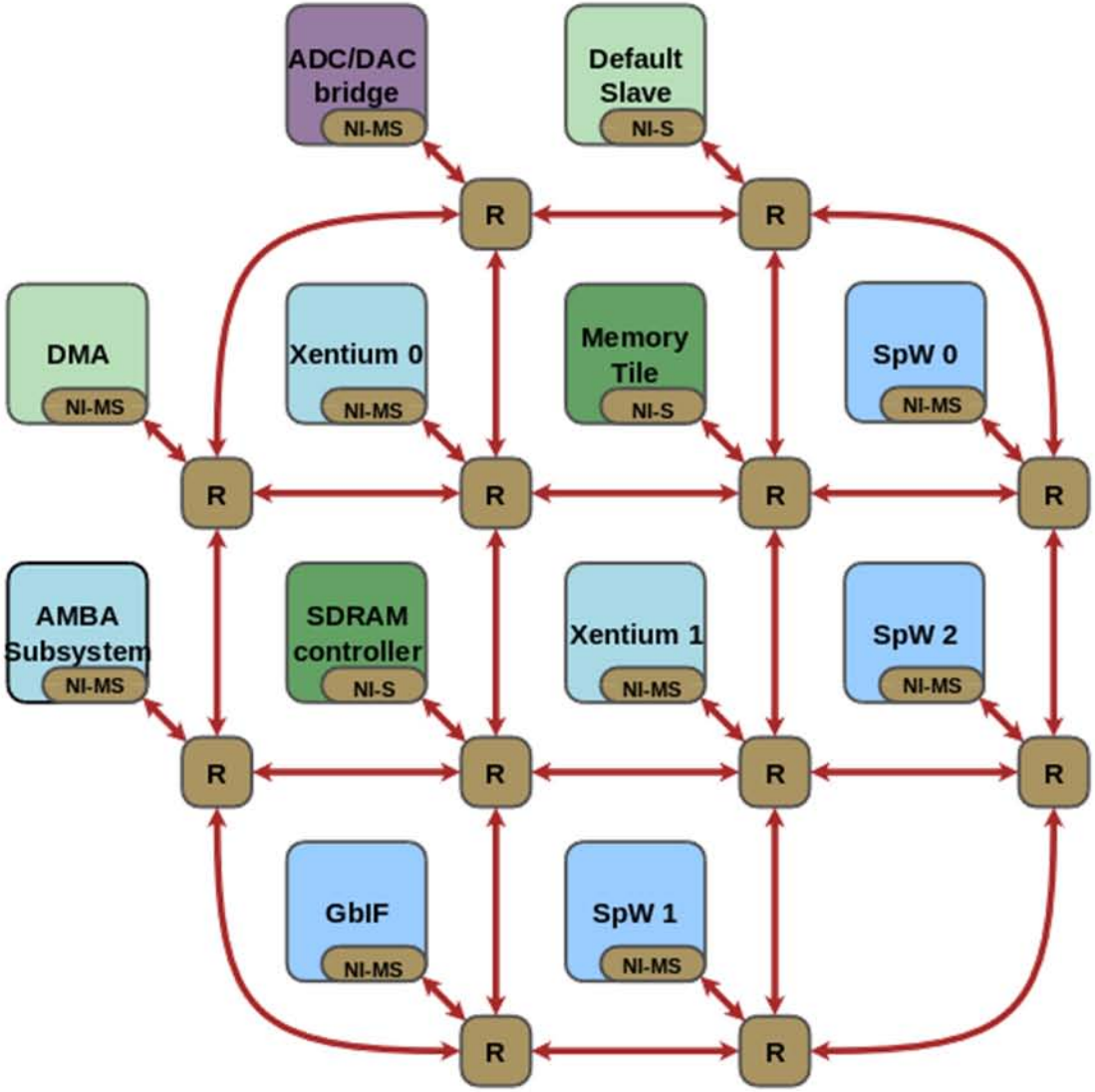
MPPB prototype on a Xilinx Virtex-5 FPGA

- 50 MHz system clock
- 2 Xentium tiles (@ 50MHz)
  - 400 16-bit MMAC/s
  - 200 32-bit MMAC/s
  - 200 16-bit complex MMAC/s
  - 64 KB data memory
  - 16 KB instruction cache
- 1 Leon2 processor (@ 50MHz)
  - 32-bit SPARC V8
  - Debug Support Unit / UART
- Network-on-Chip (@ 50MHz)
  - 32-bit packet-switched
  - 1.6 Gbps per link
    - In each direction
- Memories
  - 256 KB memory tile on NoC
  - 256 MB SDRAM on NoC
  - 256 MB SDRAM on AHB
  - 128 MB Flash on AHB
- SpaceWire (100 Mbps link)
  - 2 SpW-NoC interfaces
  - 1 RMAP-target interface
- Gigabit interface
  - 1.1 Gbps full-duplex
    - Aurora link layer protocol
- ADC/DAC-NoC interface
  - Configurable sampling rate
  - 14-bit, 40 MS/s AD6644
  - 12-bit, 40 MS/s DAC5662

MPPB architecture

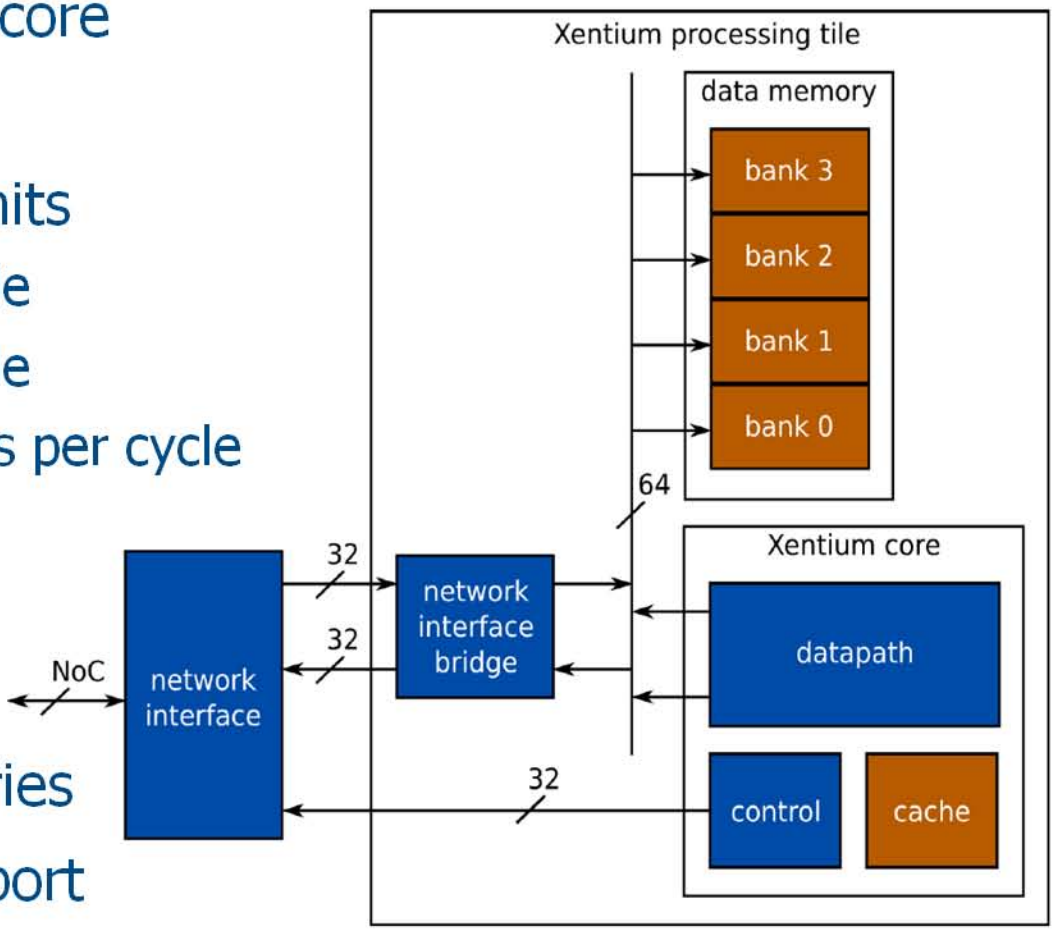


NoC subsystem



Xentium® Tile Processor core

- High-performance DSP core
- VLIW architecture
- 10 parallel execution units
  - 4 16-bit MACs per cycle
  - 2 32-bit MACs per cycle
  - 2 16-bit complex MACs per cycle
- 32/40-bit datapath
  - Fixed-point
  - Block floating-point
- Embedded local memories
- Stream processing support



MPPB interfaces bridges

- NoC interface bridges to connect external peripherals
  - Memory-mapped network interface
  - Packing/unpacking of data
  - Configuration of external peripherals
- SpaceWire link – NoC bridge
- Gigabit link – NoC bridge
- ADC / DAC – NoC bridge
  - Parallel input/output to/from ADC/DAC evaluation board
    - AD6644 – Analog Devices, ADC, 14-bits @ 40 MS/s
    - DAC5662 – Texas Instruments, DAC, 12-bits @ 40 MS/S
  - Packing/unpacking of samples in/from 32-bit NoC words
  - Configurable sampling rate of ADC and DAC

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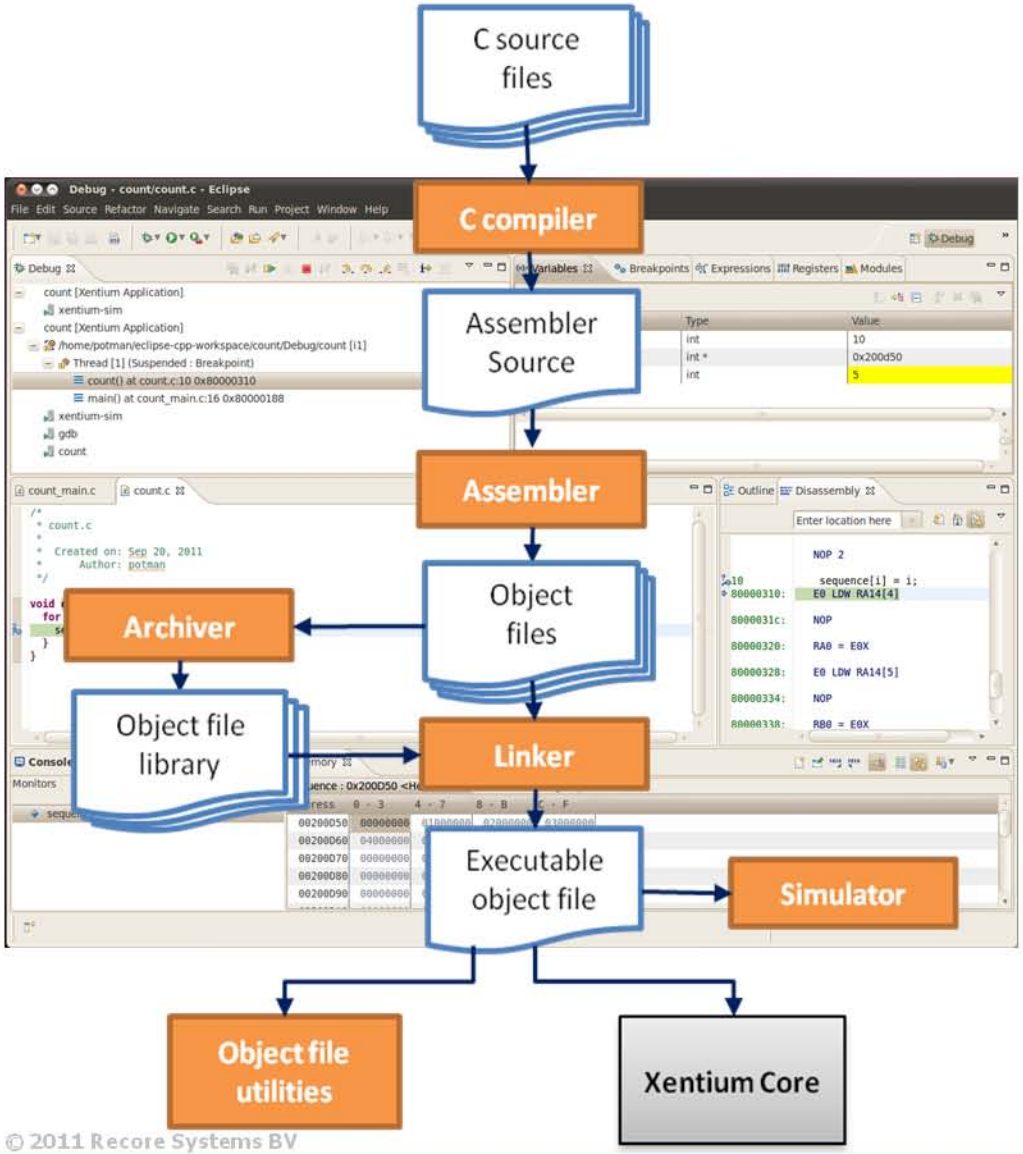
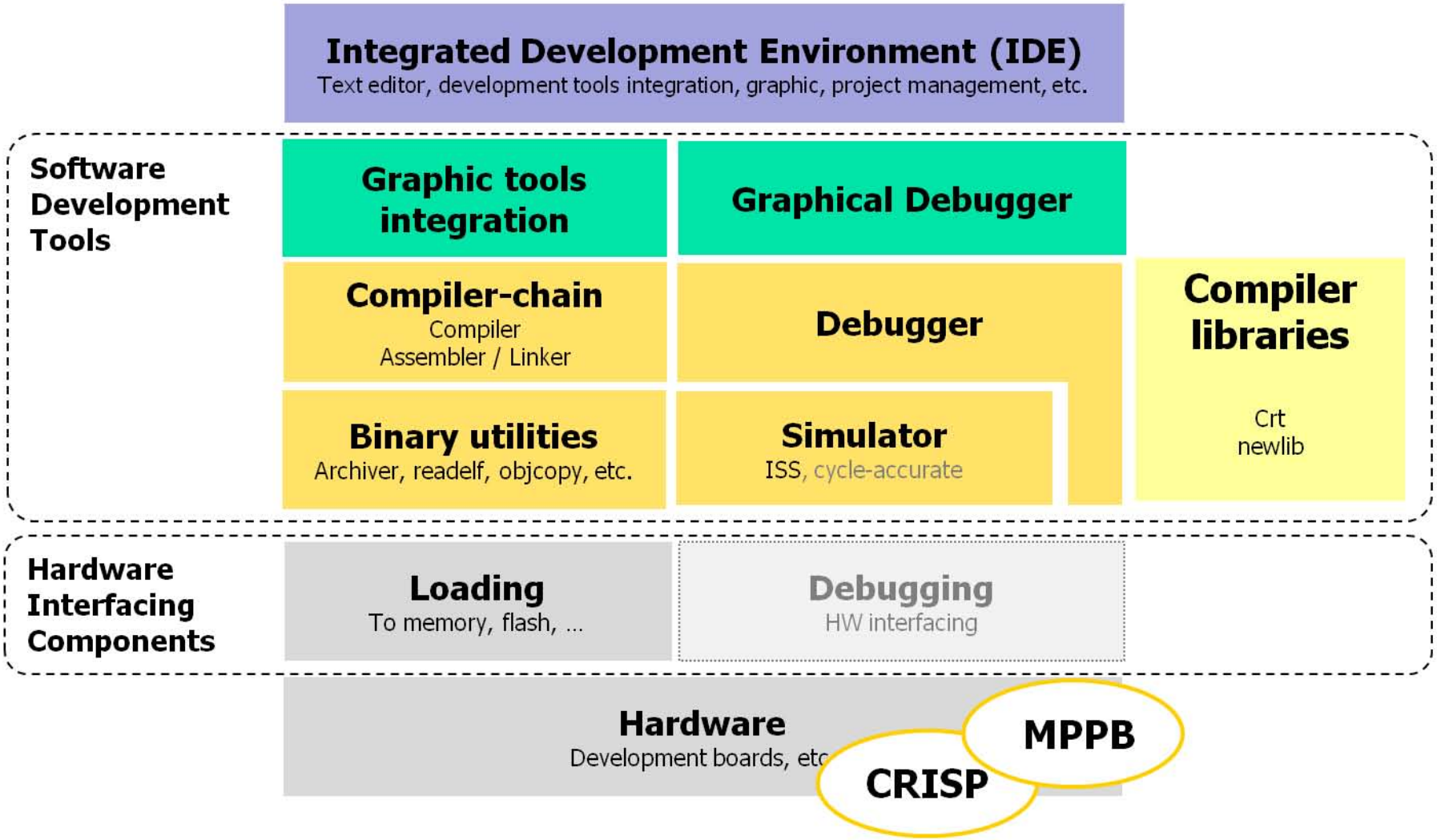
Xentium® software development flow



- Xentium C compiler
  - ANSI/ISO-standard C
  - Built-in functions for Xentium specific operations
  - Mix C and assembly functions calls
- Xentium assembler
  - Clean and readable
  - Extensive built-in preprocessor
  - Standard assembler directives
- Compile, assemble & link a program in a single step
- Xentium instruction set simulator
  - Trace program execution
  - Program execution cycle count
- Xentium Eclipse plug-in
  - Integrates command line Xentium tools into the Eclipse C/C++ IDE

Xentium Studio software development tools



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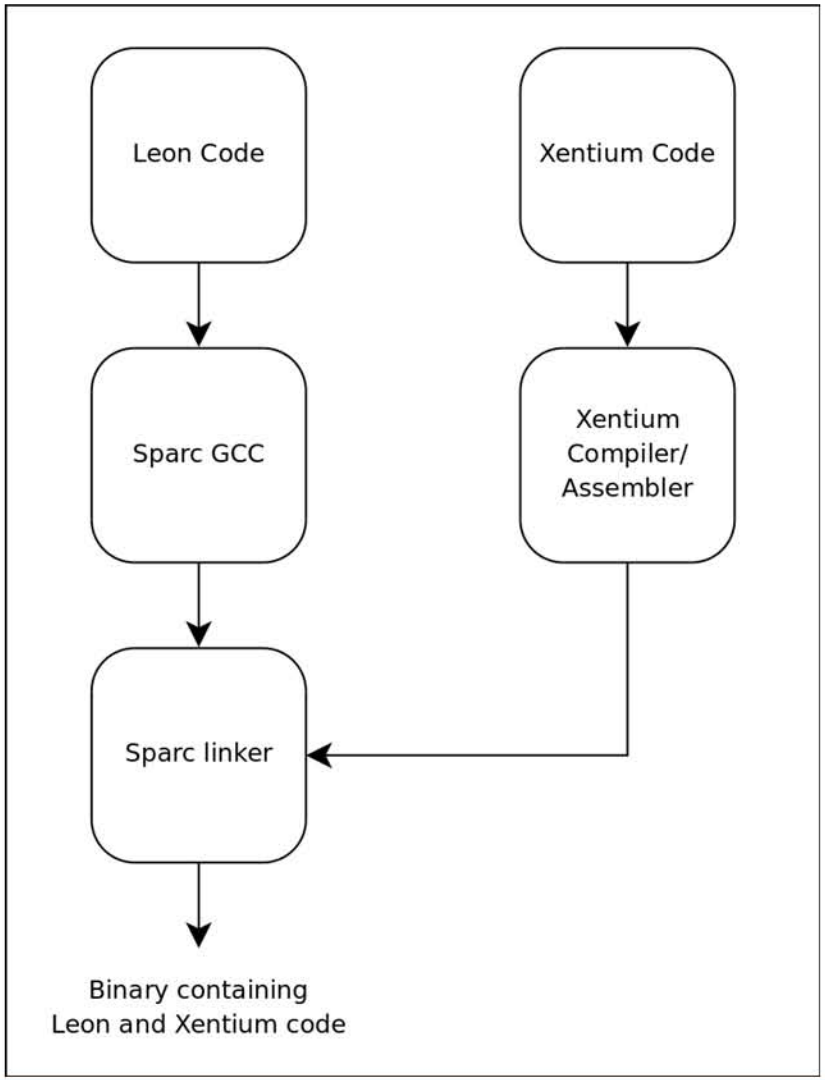
MPPB software development

- Writing code
  - Leon
    - C or SPARC assembly
  - Xentium
    - C or Xentium assembly
- Compiling code
  - Leon
    - sparc-elf-gcc
  - Xentium
    - Xentium C-Compiler or Xentium assembler
- Linking code
  - Xentium binaries are linked in the Leon binary



MPPB programming scheme

- Xentium applications
  - DSP Kernel accelerators
  - Seen as tasks, started from the LEON host processor
- Xentium API
  - Implements synchronization with Xentiums
    - Communication (interrupts/mailboxes)
    - Task queuing
  - Uses DMA to copy data to/from the Xentiums

MPPB I/O

- I/O performance
  - ADC-NoC 40 MS/s *Limited by ADC performance*
  - DAC-NoC 40 MS/s *Limited by DAC performance*
  - SpW-NoC 70 Mbit/s *SpW runs at 100Mbit/s (gross)*
  - SpW-RMAP 70 Mbit/s *SpW runs at 100Mbit/s (gross)*
  - Gigabit I/F 1.1 Gbit/s *Requirement; V-5 supports 6.5 Gbit/s*
- Running I/O concurrently at maximum speed can be achieved by using different memory resources
  - Xentium data memories
  - SRAM memory tile connected to NoC
  - SDRAM external memory connected to NoC
  - SDRAM external memory connected to AHB

MPPB performance
ESA NGDSP benchmarks (1)

- Analogue Data Acquisition Processing and Output
  - MPPB box specs
    - System clock (i.e. Xentium) runs at 50 MHz
    - The ADC and DAC run at 40 MS/s
  - Throughput from ADC to DAC (using a single Xentium)
    - Loopback @ 40 MS/s
    - FIR -16 @ 12 MS/s, FIR-64 @ 3 MS/s, FIR-256 @ 1 MS/s
    - FFT-1024 @ 20 MS/s, FFT-2048 @ 10MS/s, FFT-4096 @ 5 MS/s
    - FFT-1960 @ 1 MS/s
  - Measured overhead of LEON2, ADC, DAC and DMA interrupts
    - FIR-256: 1.5%
    - FFT-2048: 13%
      - Effective throughput 9 MS/s

MPPB performance
ESA NGDSP benchmarks (2)

- Image Data Compression and Packaging
  - Single Xentium
    - 2D Discrete Wavelet Transform (DWT)
  - LEON2 software
    - CCSDS Encoding / Packing
- Onboard Processing Case 1 / 2
  - Single Xentium
    - 128 points complex-FIR for demodulation
    - 80% Digital Down Conversion (DDC)
      - 4x upsampling and 5x downsampling
  - LEON2 software
    - CCSDS compressing (Consultative Committee for Space Data Systems)

Important observation

- The Xentium excels in number crunching
- The LEON is needed for control processing

ESA NGDSP benchmarks can be compared to NGDSP tradeoff study and COTS based computer benchmark results

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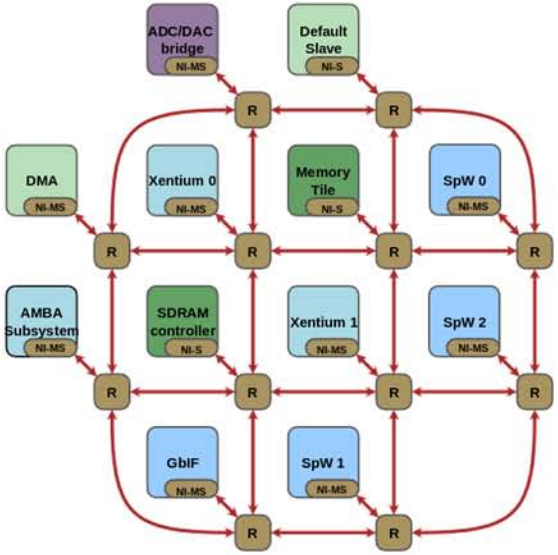
- Space-related activities & next steps

ASIC migration

- Synthesis of key components
  - Xentium, NoC router (4x4 grid), NoC interfaces (slave, master/slave, ADC, DAC)
- Analysis of Single Event Effects for fault-tolerant components
  - Rad.-hard CMOS library
  - EDAC integration
  - SEE sensitivity analysis of control logic



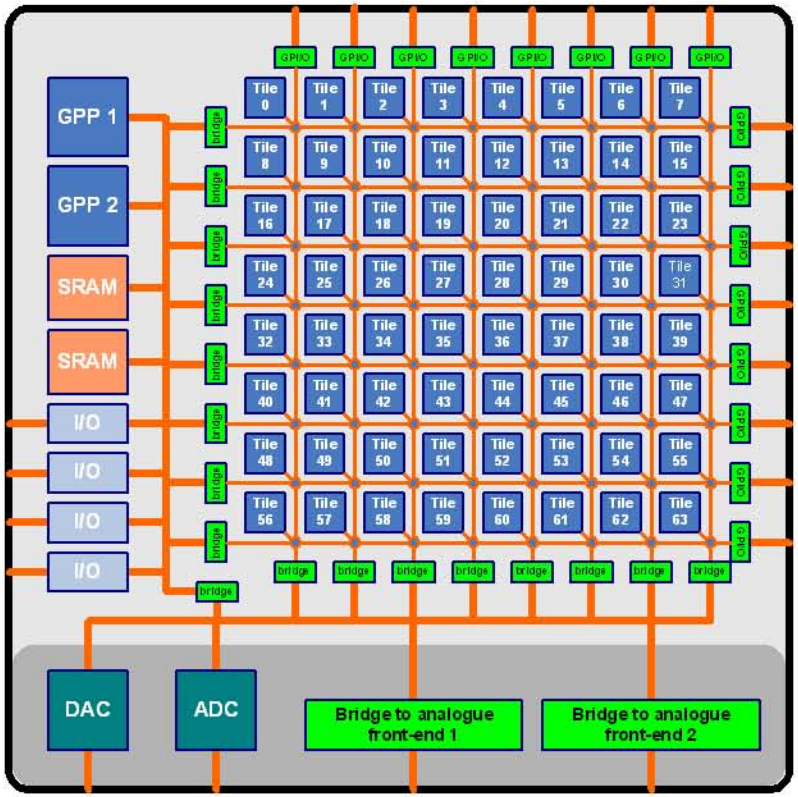
4x4 Network-on-Chip router mesh	UMC90	ST65LP	ST65GP
Total area (@200MHz)	0.788mm²	0.520mm²	0.504mm²
Non-combinatorial area	0.528mm²	0.286mm²	0.284mm²
Combinatorial area	0.260mm²	0.234mm²	0.220mm²
Max clock speed	550MHz	460MHz	870MHz
Scan-cell insertion (100%)	94.98%	94.98%	94.98%
Clock gated registers	87.61%	87.55%	87.55%

ASIC migration
rad.-hard 65nm CMOS estimations

- Xentium + NoC interface
  - Clock 300 MHz
  - Performance 1.2 GMACs/s
  - NoC per link 9.6 Gbit/s
  - Area 1.1 mm^2
    - Including NoC interface
    - 75% gates utilization
- Many-core SoC example
  - 48 Xentium processing tiles
    - Including NoC interfaces
  - 16 memory tiles
    - Including NoC interfaces
  - 64 NoC routers
    - 8×8 mesh

→ **60 Giga MAC operations/s**

→ **60 mm^2** (75% gates utilization)



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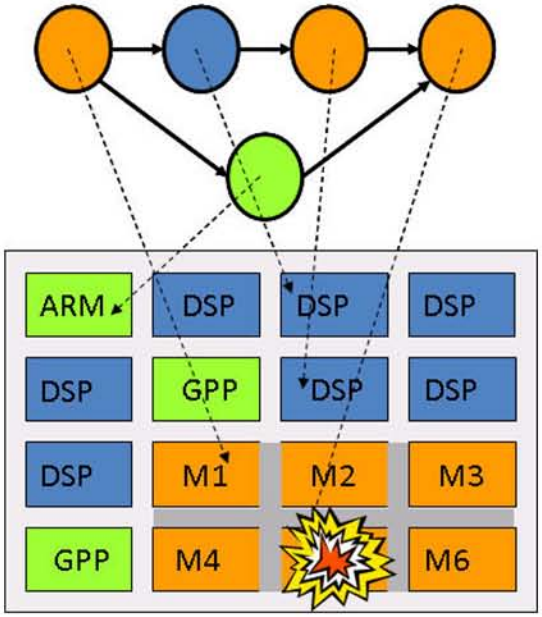
Related multi-core research at Recore

- **CRISP** (FP7)
  - *Dependable & Reconfigurable multi-core SoC*
  - 01-01-'08 / 30-04-'11
  - **www.crisp-project.eu**
- **3DIM3** (CATRENE)
  - *3D integration system architecture*
  - 01-07-'09 / 30-06-'12
- **ALMA** (FP7)
  - *High-level (reconfigurable) multi-core programming and simulation tools*
  - 01-09-'11 / 31-08-'14
- **DeSyRe** (FP7)
  - *Fault-tolerant & reliable SoC and NoC*
  - 01-10-'11 / 30-09-'14



- *Dynamically detect and circumvent faulty hardware*
- *Graceful degradation*
- *Fault-tolerant NoC*
- *Efficient multi-core programming*

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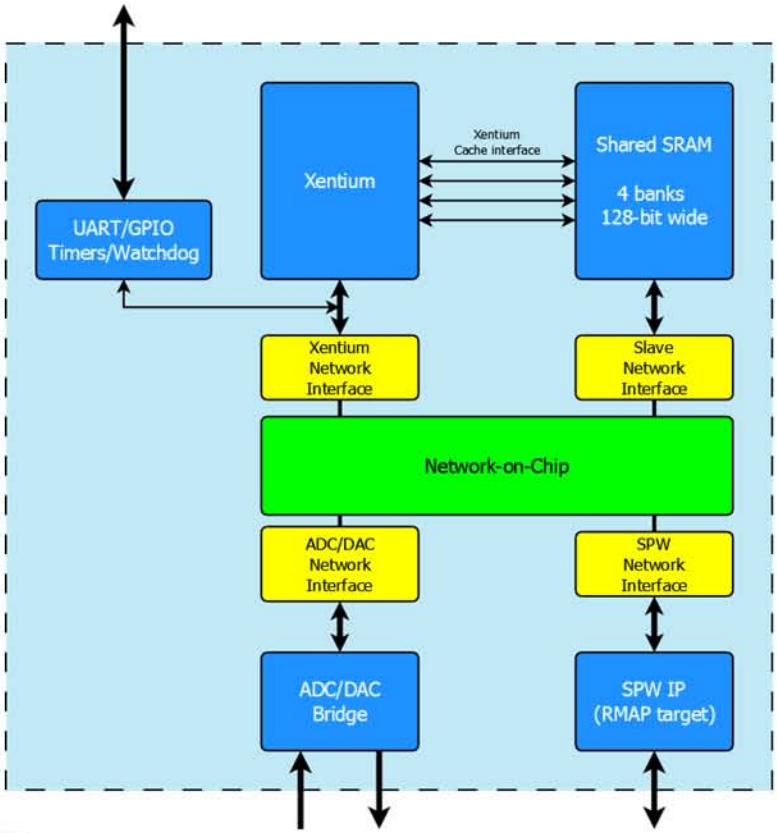
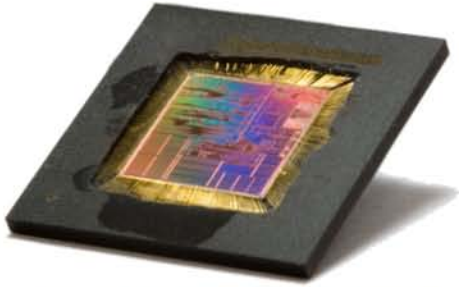
Rad.-hard DSP and NoC prototyping in DARE180

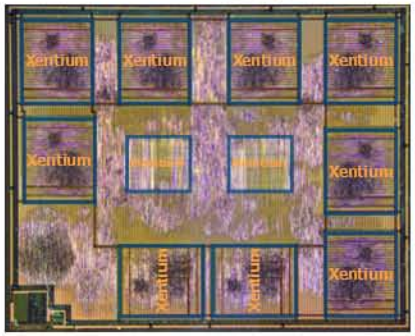
- DARE+
  - Rad.-hard prototyping of MPPB elements in DARE180
  - ESA TRP activity, 2011 – 2013
  - ESA Technical officer: B. Glass
- ASIC Prototype
  - DARE180 CMOS technology
    - Available area: 5x10 mm^2
  - Architecture
    - 1 Xentium core
    - SpW-RMAP interface
      - Connects to external host processor
    - Bridge interface to external ADC/DAC
    - Small memory tile



Technology maturity

- **2007** Reconfigurable Montium® system-on-chip
  - 4 Montiums, 1 ARM9 and other IPs
- **2010** Reconfigurable Xentium® many-core
  - General Stream Processor for digital signal processing
    - Radar digital beamforming (on 135-Xentium-cores!)
  - 9 Xentiums, 2 Memtiums and dependability manager
  - Dependable on-the-fly self-repairing chip
- **2013** Expected: rad.-hard prototype (TRL 5 or 6)
- **Xentium advantages**
  - Available as customizable IP
  - Software Development Environment
  - Small footprint and low-power
  - High performance DSP
    >20x speedup compared to GPP (@ same clock)





How can we help you?

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