Reconfigurable Multi-Core DSP Architecture for Space Applications

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Next generation digital signal processors for space applications have to be programmable, high performance and low power. Reconfigurability of digital signal processors for spacecrafts, such as instantly changing the payload processing functionality of spacecrafts while they are operational in space, becomes important. As an example, the functionality of a spacecraft can be updated in space to increase the operational lifetime of the spacecraft. Moreover, since cooling of devices in vacuum is expensive and hard to achieve, low power is key in space missions. We present a multi-core architecture for streaming DSP (space) applications comprising a conventional general purpose processor (LEON) subsystem, a reconfigurable subsystem of programmable and reconfigurable fixed point DSP cores, and multiple I/O interfaces which has been developed under the Massively Parallel Processor Breadboarding Study contract funded by the ESA TRP program. The LEON subsystem acts as the host processor, controlling all reconfiguration of the reconfigurable subsystem. The multi-core DSP subsystem comprises the following key building blocks:

- The Xentium® is a programmable high-performance DSP processor core that is efficient and offers high-precision;
- The Memtium™ is a reconfigurable memory tile that enables distributed local random access memory in a multi-core architecture;
- Network-on-Chip (NoC) technology provides sufficient bandwidth, flexibility and predictability which are required for interconnecting DSP cores and I/O interfaces in streaming DSP applications.

The Xentium is a programmable high-performance fixed-point digital signal processing (DSP) core for inclusion in multi-core systems-on-chip. High-performance is achieved by exploiting instruction level parallelism using parallel execution slots. The Xentium is designed to meet the following objectives: high-performance, optimized energy profile, easily programmable and memory mapped I/O.

The presented reconfigurable subsystem consists of programmable fixed-point digital signal processing cores that are connected by a NoC. The NoC provides the bandwidth and flexibility that is required for streaming DSP applications. The communication bandwidth in a NoC scales with the number of cores. In conventional bus architectures, additional processors share the original bandwidth and will eventually create a bottleneck. A NoC ensures predictable performance due to its point-to-point connections, in contrast to the unpredictability of a shared bus.

Several I/O interfaces are available on the multi-core DSP architecture; SpaceWire bridge-interfaces, Giga bit-link interfaces and bridges to external ADC and DAC devices are integrated in the architecture. All interfaces are connected the NoC of the multi-core DSP subsystem.

The presentation will highlight research activities focusing on multi-core DSP development, programming multi-core DSP, benchmarking, and migration to rad.-hard CMOS technologies as well as ASIC prototyping. The advantages of Recore's DSP and NoC technology over Mono- and Multicore General Purpose Processors in terms of performance, power consumption, and scalability are presented. Benchmark results for typical space based payload data processing algorithms are shown, and the software development tools and procedures are introduced.