From MERASA to parMERASA -

Multi-core Deployment in Hard Real-time Systems

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ESA Workshop on Avionics Data, Control and Software Systems (ADCSS)
Multi-Core Processors for Space Applications
Oct. 27, 2011

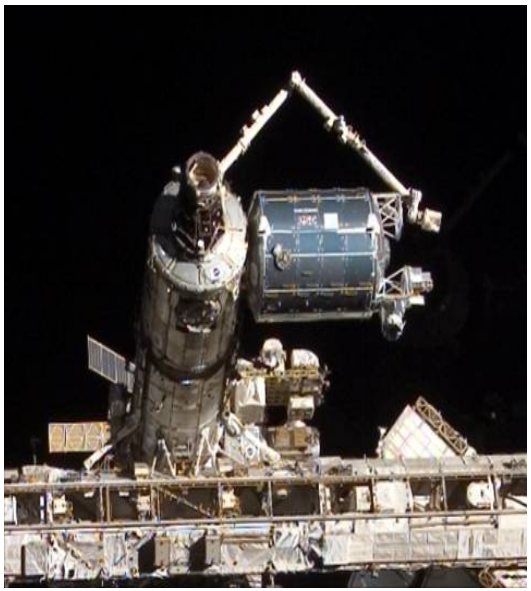
Overview

- **Motivation and demands** on embedded processors
- **MERASA project** overview, targets and achievements
- **parMERASA project** overview and targets
- **Conclusions and Vision**

Demands on Embedded Processors

- **Increasing demand** for functionality in current and future real-time embedded systems
- Often demand for **mixed criticality applications** execution

Increase of processor performance demanded



Demands on Embedded Processors

- **Time is critical** in embedded systems!

- Safety-related **hard real-time** embedded systems…
  - → require that a deadline must never be missed,
  - → need a prove of timing requirements by **WCET** (worst case execution time) **analysis**.

COTS (common of-the shelf) Processors

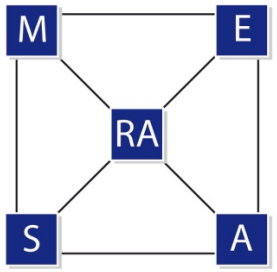
- **COTS processors** contain features that make a WCET analysis hard or even impossible, as e.g.
  - Complex branch prediction (near to impossible)
  - Out-of-order instruction queues (impractical)
  - Instruction caches (hard, but can be done)
  - Data caches (difficult)
  - Two level cache hierarchy (even more difficult)
  - Complex DRAM technologies (impractical)
  - Simultaneous multithreading (SMT), hyperthreading (impossible)
- COTS processors are designed for **high average performance, not for timing predictability**

COTS Multi-Cores

- **COTS multi-core processors** bring in additional handicaps for hard real-time tasks
  - Bus is shared among the cores, bus conflicts possible
  - Shared secondary cache
  - Access to memory must be arbitrated
  - I/O and interrupt handling
- Again, COTS multi-core processors are designed for **high average performance, not for timing predictability**

Demands on Embedded Processors

- Solution:
  Development of ...
  - **multi-core embedded processor** technology
  - in concert with **WCET** technology
  - and industrial **applications**
- Targets of **project MERASA** (2007-2011)
- Main target of **project parMERASA** (2011-2014):
  Parallelisation of Hard Real-time Applications for multi-cores



MERASA

Multi-Core Execution of Hard Real-Time Applications Supporting Analysability

EC FP-7 project 2007-2010

2.1 Mio EC contribution

Project webpage: http://merasa.org

MERASA Project Partners

- **University of Augsburg** (Project Coordinator)
  Germany
- **Barcelona Supercomputing Center**
  Spain
- **Université Paul Sabatier**
  Toulouse, France
- **Rapita Ltd.**
  York, UK
- **Honeywell international s.r.o.**
  Brno, Czech republic

Principal MERASA Research Focus

MERASA processor architecture

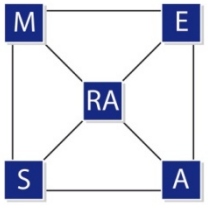
- **Embedded high-performance multi-core** processors
- Targeting **4 cores** (on FPGA) up to **16 cores** (on simulators)
- **Hard real-time** capable design

WCET analysis tools for multi-cores

- **Static** WCET analysis (OTAWA[1])
- **Measurement-based** WCET analysis (RapiTime[2])
- Interoperability of tools, coding guidelines

[1] OTAWA: a tool of University of Toulouse

[2] RapiTime: a tool of Rapita Systems Inc.



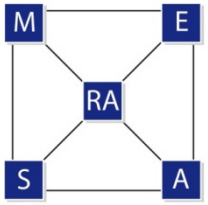
Principal MERASA Research Focus

System-level software for multi-cores

- **Isolation of hard real-time threads** running on different cores
- Time-bounded **thread synchronization** techniques

Embedded hard real-time applications

- **Honeywell International:** stereo navigation and collision avoidance
- **Industrial Advisory Board:** additional studies with ESA, Infineon, and BAUER Maschinen



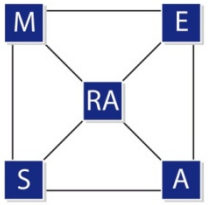
The MERASA Core

- **MERASA core architecture techniques**
  - Two-way in-order superscalar, 4-way simultaneous multithreaded (SMT) core
  - Internal **hard real-time scheduler** performs SMT execution
  - All pipelines are designed **non-blocking**
  - Long running instructions implemented by **preemptible microcode sequences**
  - Hard real-time tasks uses instruction and data **scratchpads** local to core (to limit interferences)

→ Each cycle an instruction of the highest prior task can be issued to each pipeline

→ **No blocking** by other task

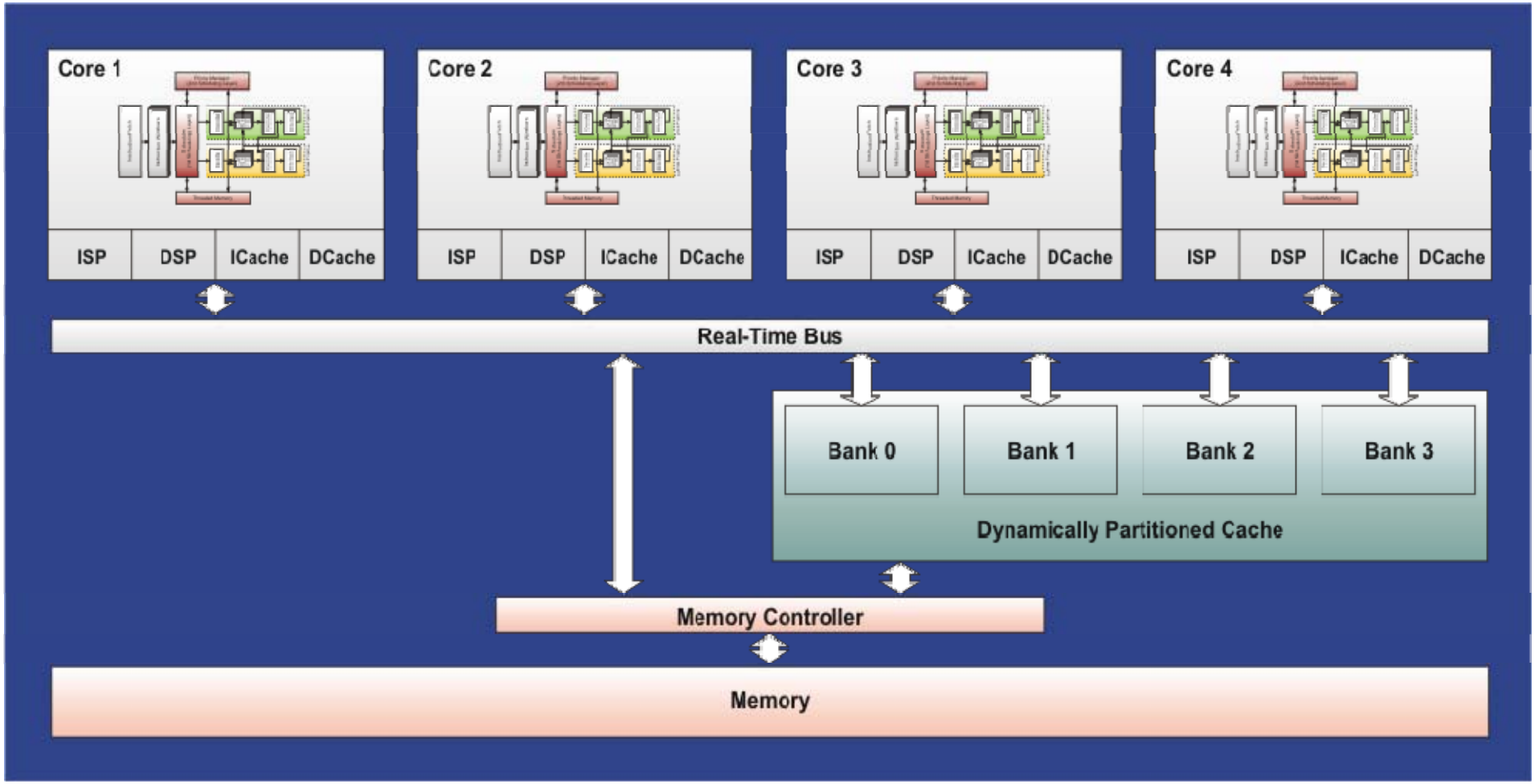
→ **Full isolation** of tasks reached for the MERASA core

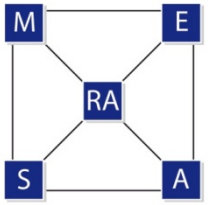


MERASA Multi-Core Processor

- **MERASA multi-core architecture** design targets:
  - Limitation of the number of shared resources
  - Bounding of interferences for inter-core features
- **MERASA multi-core architecture techniques:**
  - **Core-local scratchpads** combined with **Dynamically Partitioned Cache** decrease number of accesses to shared memory
  - Round-robin/time triggered (**TTA**) access to bus and memory bounds access times
  - Hard real-time capable **DDR2 SDRAM controller**
  - **Support for thread synchronisation** implemented in SDRAM controller to decrease WCET overestimation

General MERASA Architecture





MERASA Project Achievements
(Processor Architecture)

- **MERASA multi-core architecture**
  - Timing-predictable multi-core architecture based on in-order SMT cores
  - One hard real-time task per core in isolation
  - Capable of mixed execution of hard real-time and non real-time applications
  - N-core on simulator, quad-core as FPGA prototype

Hard real-time support by full **isolation of tasks** and **bounding of interferences**
Full partitioning at task level and **WCET analysability**

MERASA Project Achievements
(Tools and System Software)

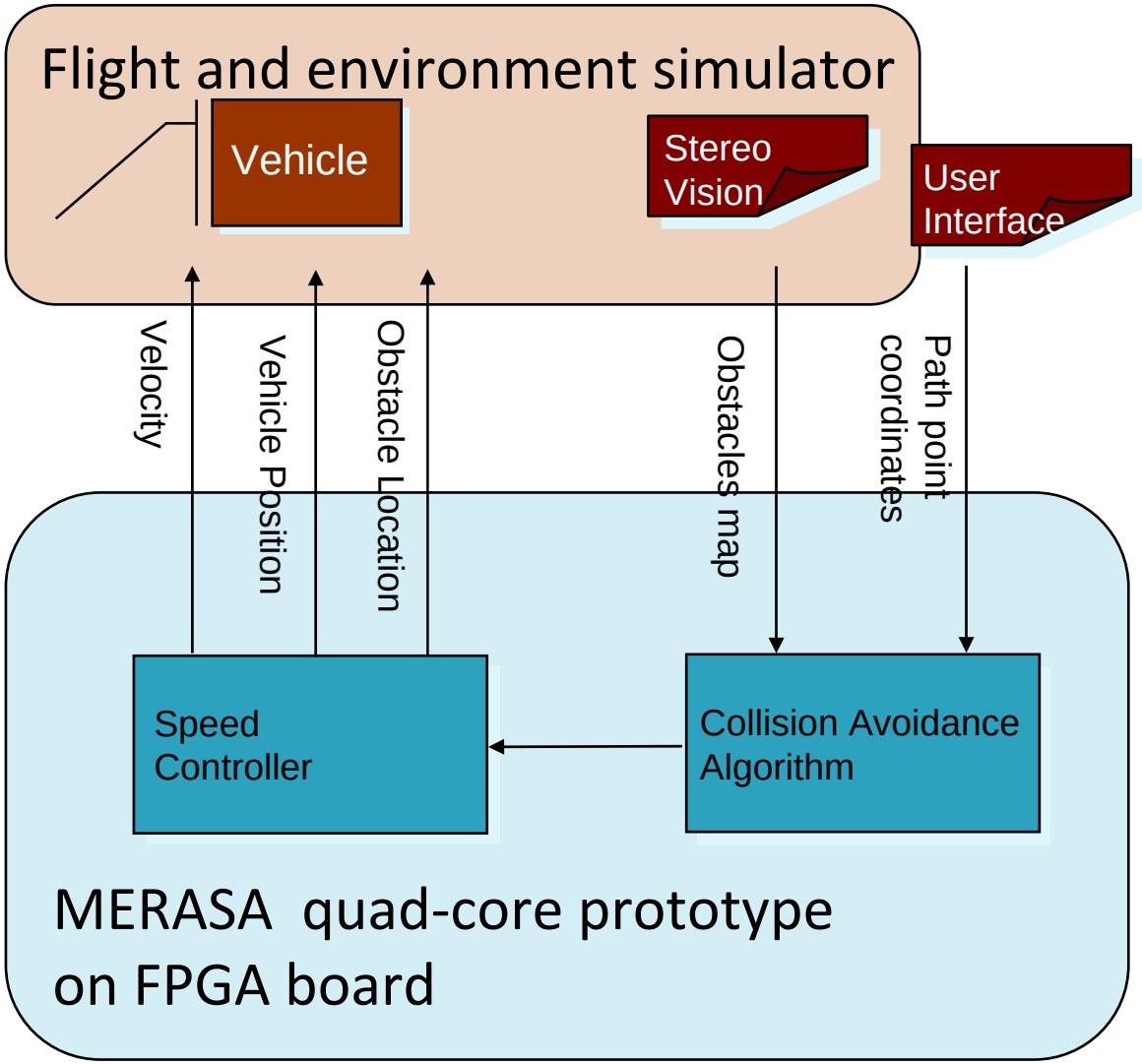
- **WCET tools**
  - **OTAWA** and **RapiTime** tools adapted to MERASA multi-core
  - FPGA prototype enhanced to send **traces of multi-core** execution to RapiTime Tracing Box (**RTBx**)
  - **Zero-overhead tracing** technique developed for RapiTime
  - **Interoperability** of WCET tools
  - **Coding guidelines** for sequential and parallel applications

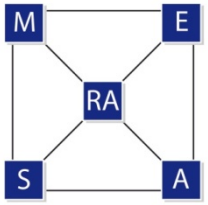
- POSIX compliant **system-level software**
  - **Isolation** of hard real-time threads
  - **Time-bounded** thread **synchronisation** techniques
  - **Drivers** for FPGA and pilot studies

MERASA Project Achievements
(Application Software)

- **Applications by Honeywell International**
  - **Parallelized collision avoidance** algorithm
    - runs on both simulators and FPGA prototype,
    - analyzed with both WCET tools,
    - used in demonstrator of “autonomously flying vehicle simulator”.
  - **Parallelized stereo navigation** algorithm
    - is too resource demanding for low-level simulator and FPGA,
    - runs in selected parts on high-level simulator,
    - analyzed with both WCET tools.

Pilot Study with Honeywell International: Autonomously Flying Vehicle





A Step Towards Time-Predictable Execution of Parallelized HRT Tasks

Combination of software and hardware techniques

- **For software**:
  Coding guidelines for parallelisation and WCET analysability
  - Time predictable system software required
  - Parallelisation is done based on parallel design patterns

- **For hardware**:
  Fully time-predictable multi-core processor design
  - isolation as far as possible or
  - bounding timing effects in case of shared resources

parMERASA

SEVENTH FRAMEWORK PROGRAMME

Multi-Core Execution of ***parallelised*** Hard Real-Time Applications Supporting Analysability

EC FP-7 project 2011-2014, start Oct. 1, 2011

3.3 Mio EC contribution

Project webpage: http://www.parmerasa.eu

parMERASA Motivation

- **Multi-core processors** provide a solution **higher levels of performance** of embedded hard real-time systems.
- T**iming behaviour of parallel applications is not analysable** with current analysis techniques.
- **New hardware and software design paradigms** together with **new analysis techniques** are required.

parMERASA Targets

- Find ways to **efficiently parallelise industrial applications** for embedded real-time systems.
- Provide **hard real-time support in system software, WCET analysis and verification tools for multi-cores**.
- Develop techniques for **time predictable multi-cores with 16 to 64 cores** which are commercially feasible.
- Contribute to **Standards** and **Open Source Software**.

parMERASA Project Partners

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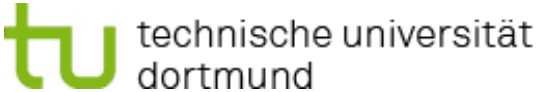
  Germany

- **Barcelona Supercomputing Center**
  Spain

- **Université Paul Sabatier**
  Toulouse, France



- **Technical University of Dortmund**
  Germany

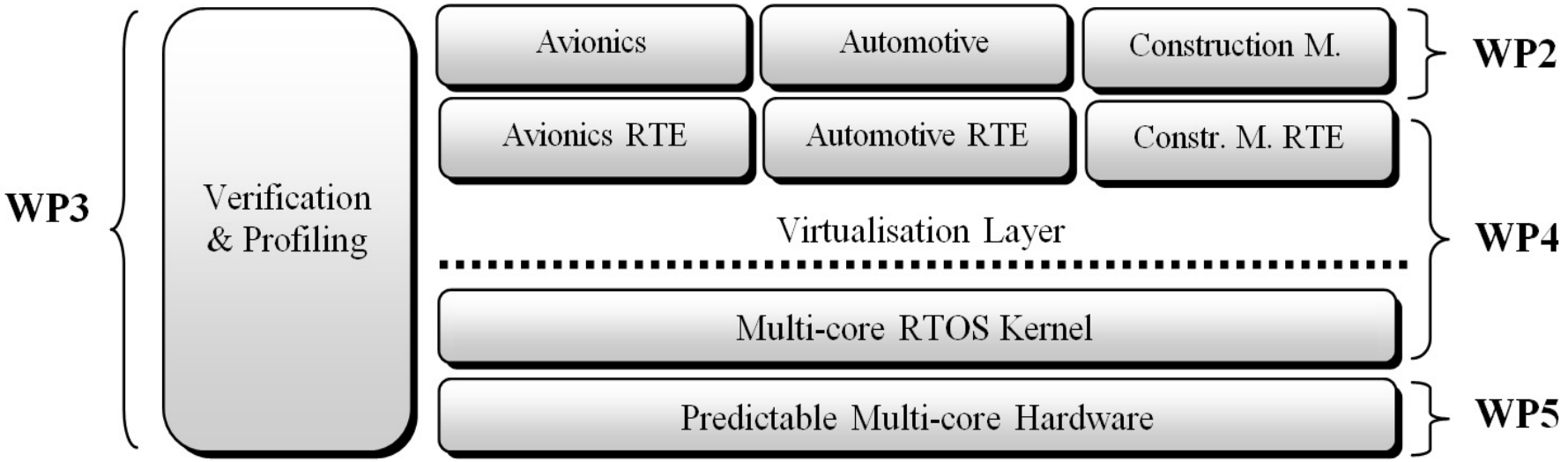
- **Rapita Systems Ltd.**
  York, UK

- **Honeywell international s.r.o.**
  Brno, Czech Republic

- **BAUER Maschinen GmbH**
  Schrobenhausen, Germany

- **DENSO Automotive Deutschland GmbH**
  Eching, Germany

parMERASA System Architecture Layers



parMERASA Industrial Advisory Board

- **Airbus,** Toulouse, France
- **European Space Agency ESA,** Noordwijk, Netherlands

- **Infineon Technologies UK Ltd**, Bristol, UK
- **Infineon Technologies AG**, Dept. Industrial & Automotive, Munich, Germany
- **BMW Group**, Munich, Germany
- **MECEL AB**, Sweden
- **Elektrobit Automotive GmbH**, Erlangen, Germany

Conclusions

- **Hard real-time demands** in safety critical areas require **timing predictable multi-cores**.
- **MERASA project** showed that **timing predictable multi-core design together with adapted WCET tools and system software** can be achieved
- **parMERASA project** targets **application parallelisation** such that timing predictability can still be guaranteed

MERASA and parMERASA Vision

- **Application companies** in safety critical areas should **demand timing predictable multi-cores**.
  - WCET analysis and verification instead of / additionally to testing.
- **Safety standards and certifications** will be **tightened to demand such processors in future**.
- **Automotive safety requirements** will develop to be **closer to the high safety standard in aerospace**.
  - Timing predictable processors can be foreseen in high volume market, also favorable for aerospace.
- **Higher performance demand** may – in future – be satisfied by **multi-cores with more than 16 cores**.

Our Vision

Make **timing predictable** techniques commercially feasible to **increase safety** in **aerospace**, **space** and **automotive** domains!