Multi-Core Processors for Space Applications
MCPSA- ADCSS 2011
Welcome

27 October 2011

European Space Agency

www.esa.int

Multicore

Multi-Core or Chip Multi-Processing (CMP), is a processor technology that provides parallel processing capabilities by containing multiple independent execution cores and instruction pipelines within one packaged processor assembly.

Applications across all the various categories of the embedded market as signal processing in aircraft avionics, multitask execution in automation, multimedia processing in consumer devices , are requiring higher performance.

A method of achieving higher performance is the increase of the processor clock frequency > increase of processor power dissipation figure.

Multi-core architecture is an alternative architectural solution has the main advantage to increase the platform performance without increasing the power consumption

	frequency	power dissipation increase	perfomance increase	remark
	1%	**3%**	**0.60%**	from Intel Corp. for <100nm (http://bcove.me/robm4kag)
example 1	15%	45%	9%	monocore
example 2	30%	90%	18%	monocore
example 3	**-15%**	~	**180%** Amdahl's Law $S_N = \frac{1}{(1-P) + \frac{P}{N}}$	Dual core

An example of Multi-core: Smarthphones & Tablets

Multi-Core technology allows simultaneously processing of multiple concurrent functions within one application, decomposing data and/or tasks to be distributed and simultaneously processed across all cores.

The list of smarthphones and tablets with dual-core processor (usually combined with a GPU) is continuously increasing:

The multi-core boom is the result of a marketing strategy, technology innovation but also thermal limitations: 1-1.5 GHz is the maximum achievable frequency on a smarthphone or tablet, exceeding this limit increases enormously the power dissipation…a hole in your pocket could be the consequence…

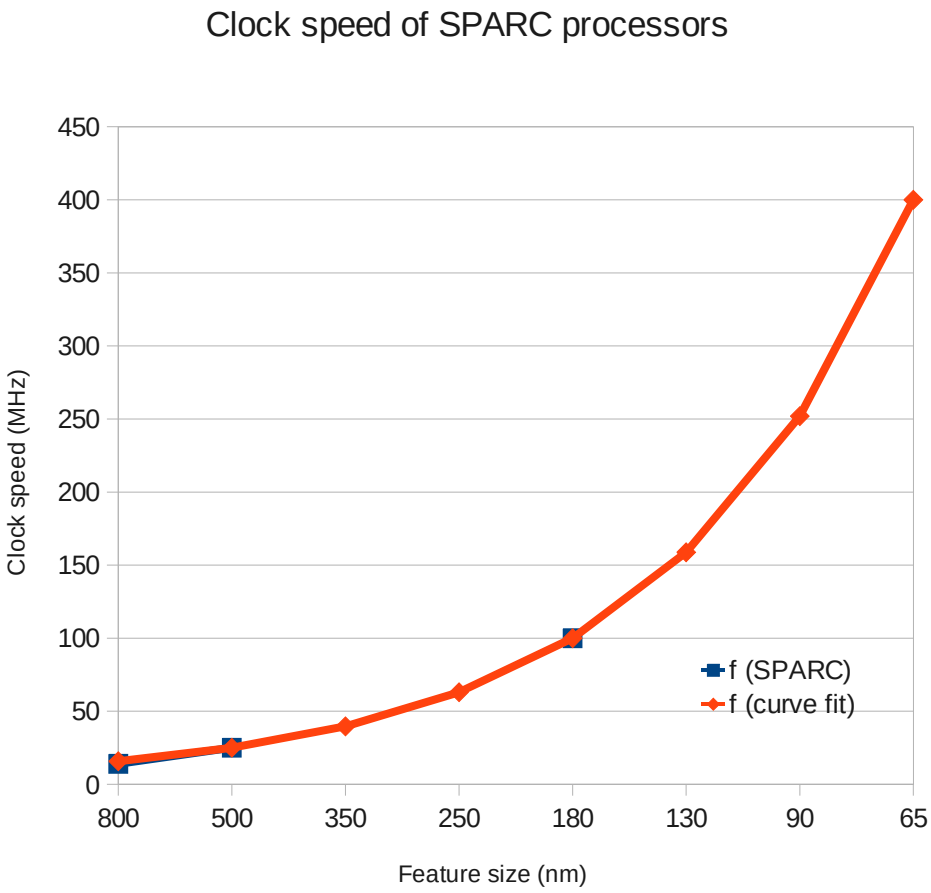
Strategy Analytics Inc recently forecast 15 % dual-core penetration in smartphones by the end of 2011, with an estimated 45 % penetration by 2015.

Clock frequencies of SPARC processors for Space

Clock Speed of SPARC Architectures*

mid 90's	end 90's	mid 00's
ERC32 3-Chip Set	ERC32 Single Chip	LEON2-FT AT697
ATMEL (TEMIC)	ATMEL (TEMIC)	ATMEL
0.8 mm	0.5 mm	0.18 mm
SPARC V7	SPARC V7	SPARC V8
10 MIPS 14 MHz	20 MIPS 25 MHz	85 MIPS 100 MHz

Extrapolating to 90 / 65 nm we obtain 250 / 400 MHz



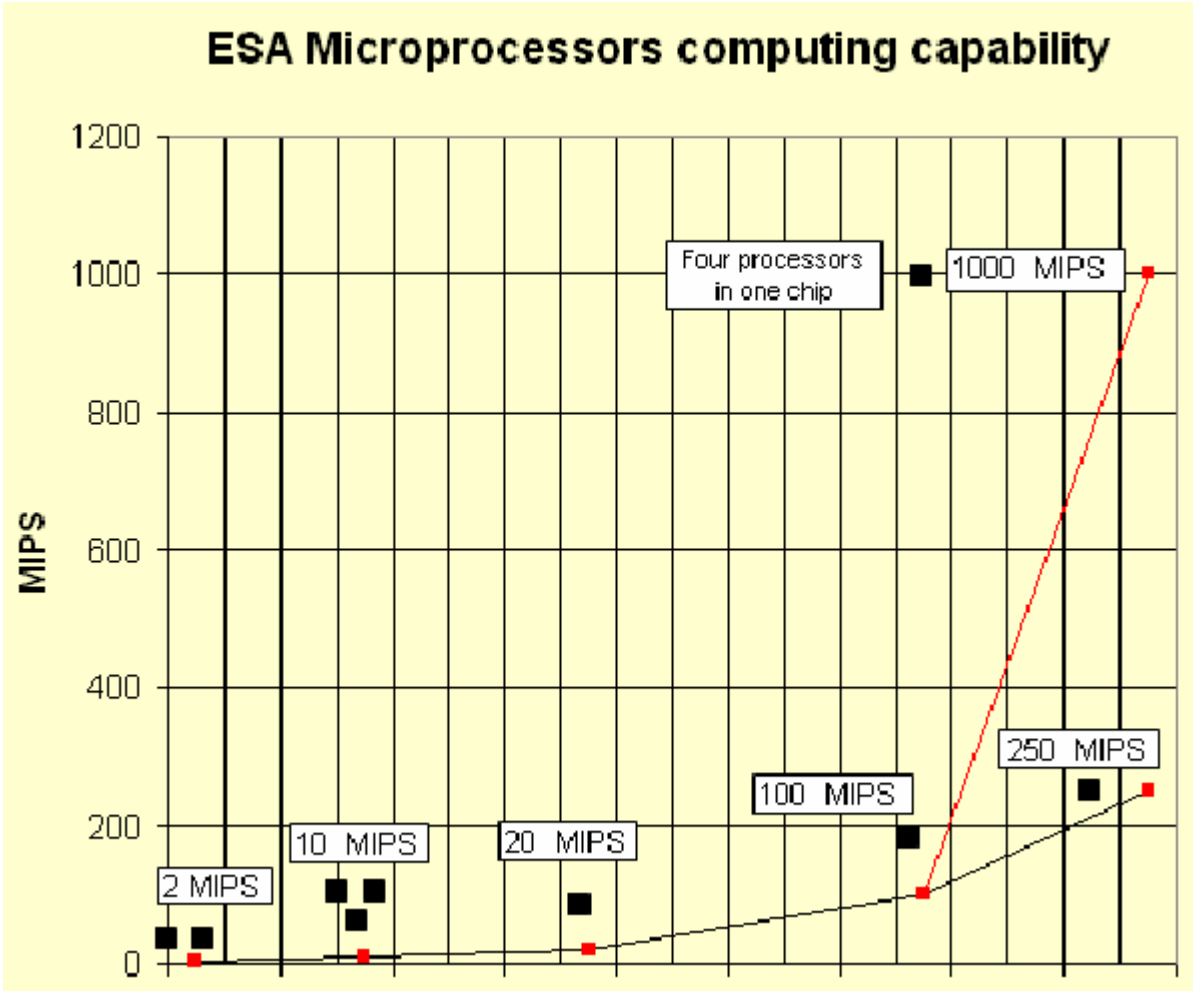
* See also the presentation "A Giga INstruction Architecture (GINA) for the future ESA microprocessor based on the LEON3-FT" *André L. R. Pouponnot TEC-ED DASIA 2006*

Multi-Core: enabling higher performance

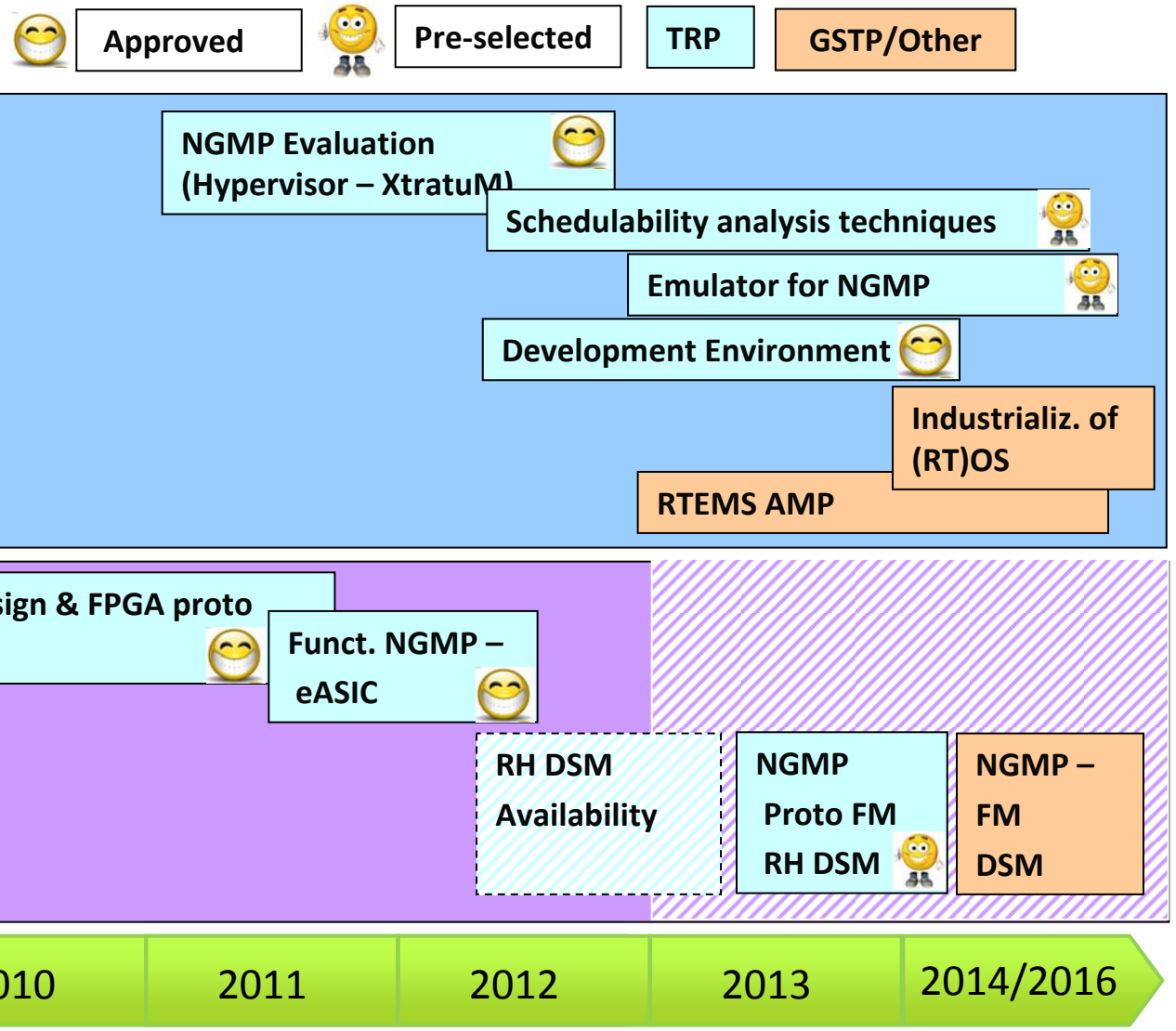
Even at 65 nm, we are limited to 400 MHz (~ 340 MIPS)

How further increase performance?

Multi-Core



ESA Roadmap for NGMP



Previous Events:
GINA study 2005-2006,
NGMP roundtable Sept 2006

Multi-core in space

Following the outcomes of the 2006 round table ESA has pursued the road of multi-core architectures: they enable the execution of more complex control algorithms and open the door to a higher degree of autonomy on-board,

But Multicore also shakes the foundations of the traditionally used programming models, introducing the notions of concurrency, resource sharing and synchronisation.

The introduction of multi-core technology in the future on-board computers requires new software solutions and software design methods.

The objective of this ADCSS2011 session is to present the current status of multi-core solutions for space applications, concerning both the hardware and software aspects and to present missions and applications for which multi-core platforms are needed

Advanced researches on the characterization of the worst case execution time (WCET) of hard-real time multi-core systems made in the frame of FP7 projects will also be presented

A final round table will discuss open points and should help to define intermediate steps to implement future platform and payload system based on multi-core architecture.

Agenda

Multi Core Processors for Space Applications			
09:00	Welcome	G. Magistrati	ESA/ESTEC
09:05	Next Generation multipurpose Processor – Status, Use Cases and Benchmarks	J. Anderson	Aeroflex Gaisler
09:35	Impact of Distributed Multiprocessor Systems and xTratum	M. Patte/ A. Crespo	Astrium / University Politecnica de Valencia
10:20	IMA and multi-core processors	Alain Rossignol (Astrium) / Peter Mendham SciSys	SciSys / Astrium
10:50	*Coffee Break*		
11:05	Measuring inter-task interferences in the NGMP	R. Gioiosa	Barcelona Supercomputing Center
11:35	Multi-core for payload processing: use case from the Euclid mission	P. Crouzet	ESA/ESTEC
11:55	GNC application cases needing multi-core processors	G. Ortega	ESA/ESTEC
12:20	Evaluation of the Multi-Core Technology for Demanding Space Applications	Peter Behr	Fraunhofer
12:40	*Lunch*		
13:40	Reconfigurable Multi-Core Dsp Architecture For Space Applications	P. Heysters	Recore
14:00	Results from MERASA and ParMERASA FP7 Projects	T. Ungerer	University of Augsburg
14:20	Results from PROARTIS FP7 Project	Jaume Abella	Barcelona Supercomputing Center
14:40	Multicore Systems -- Impact of the Programming Language	F. Siebert	AICAS
15:00	Round table		
16:00	WRAP-up		
16:10	*Workshop closure*		