ThalesAlenia Space
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Microcontrollers for Embedded Space Applications (MESA) Roundtable

Microcontrollers Applications within Thales Alenia Space products

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- An overview on previous applications
- Current developments
- Reference Applications
- Requirements

Some previous applications

- **Based on Atmel 82C32 device:**
  - experiments in microgravity (eg. MDS, PUE1 of PCDF facility)
  - plasma propulsion (Pleg-Pay, Lisa EPDP, SMART1)
  - Micro-propulsion control (eg PID control of array of thrusters)
  - Antenna Pointing Controller
  - RDIU Modules for TLC Spacecrafts
  - Generic equipment configuration set-up and monitor (e.g. MetOp FMU)

- **Based on UT69RH051 (Aeroflex UTMC)**
  - Various on TLC and Observation Payloads : MTSAT, ISRO, COF-PDU

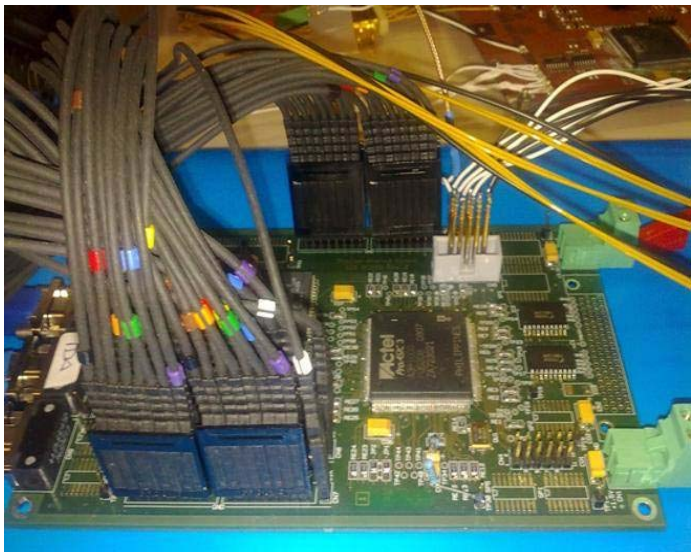
- **Customised version of Leon2:**
  - DST Control ASIC

Identified Limits of 80C32 component

- Architecture, based on the accumulator register, which dates back to the seventies.
- Poor addressing capability (64kx8 Data and 64kx8 Program Memories)
- No EDAC supported
- Limited set of instructions
- Lack of an ALU for, at least, for fixed point operations.
- 80C31 instruction usually takes 12 CPI (clock per instruction) with the inefficiency of an architecture base on a “accumulation register” continuously accessed to store the value of the operand
- Architecture was designed to be programmed in assembly code language (using a language like C, we pay in efficiency in term of compiled code size of 1,5 to 3 time w.r.t. an up to date core)

Bepi Colombo ISA Control Board

- Built around an “ad hoc SOC” implemented in AX2000 FPGA (the development board uses a ProAsic3):
  - Based on Actel IPcore 8051
    - Free License
    - Ability to execute an instruction every clock
    - Amba bus interface
  - On chip debug interface
  - 2 IP core Space Wire (supported by four DMA controller for data transfer)
  - EDAC
  - AMBA BUS APB3
  - Memory controller with paging register
  - Interrupts controller (8+8 channels)
  - 4 x 32 bits timers
  - Watchdog
  - 1 UART
  - GPIO General purpose IO interface
  - OBT based on SET format(SW time code)
  - Automatic switch on active SW bus (redundants interfaces)
  - HK multipexer management and ADC I/F
  - 1 PWM output.



- LVDS links for the 4 spacewires
- SRAM: 512kx16 (for data or code and check bits),
- EEPROM: 128kx8EEPROM,
- Boot PROM
- 20MHz oscillator
- KEIL SW Development Environment

We have to consider two, not exclusive, implementation options:

- Inclusion as an IP Core in ASIC or FPGA
- Stand-alone device

We also shall try to satisfy two performance classes:

- Very low performances, simple set-up and monitor
- Some processing performances (around 10/20 MIPS)

In both cases a true microprocessor (32 bits) is oversized

Some reference applications sizing

APPLICATION	MIPS	ALU	MEMORY RESOURCES (NET, NOT INCLUDING EDAC)	
			CODE	DATA
Micro Propulsion Control	6-10	Yes (at least Fixed Point)	PROM: 32 kBytes EEPROM: 128 kBytes RAM: 128 kBytes	EEPROM: 128 Kbytes RAM: 64kBytes
Mechanism and motors control	1-10	Yes (at least Fixed Point)	PROM: 32 kBytes EEPROM: 64-128 kBytes RAM: 64-128 kBytes	EEPROM: 64 Kbytes RAM: 64kBytes
Thermal control	1	Not mandatory	PROM: 32 kBytes EEPROM: 64 kBytes RAM: 64 kBytes	EEPROM: 64 Kbytes RAM: 64kBytes
Management of Life Experiment	1-3	Desired	PROM: 32 kBytes EEPROM: 64 kBytes RAM: 64 kBytes	EEPROM: 64 Kbytes RAM: 64kBytes
Plasma Monitors	1-3	Desired	PROM: 32 kBytes EEPROM: 64 kBytes RAM: 64 kBytes	EEPROM: 64 Kbytes RAM: 64kBytes

Some requirements

- Basic Core:
  1. Equipment configuration set-up and monitor
     - → Simple, 8051 like (ASEM51 Instruction set)
     - → IP for embedding into ASIC or FPGA
  2. Providing some processing performances
     - → Based on Von Neumann architecture (like ARM7DMI)
     - → Or Modified Harvard architecture (like ARM9)
     - → V8uC (SPARC) to be assessed
     - → Mainly for a stand alone component
     - → But also IP for embedding into ASIC or FPGA

- Word size: 8 / 16 bits selectable
- Processing Throughput (case 2.): ~ 1 MIPS/MHz – max 25 MHz clock
- Arithmetic Operations (case 2.): At least fixed point
- DMA channels (at least 2) to move data from / to peripherals and memories

Some requirements (cont.)

Memories interfaces:

- 1 Mbyte addressing space
- Controllers for PROM, EEPROM, Flash, SRAM, DRAM (tbc)
- EDAC
- Possibly some memory areas embedded in discrete component, both volatile and non volatile.

Communication Links:

- AMBA (APB3 preferred), for IP Core
- SpaceWire / RMAP (also for load and dump, test purposes) (*)
- CAN Controller (*)
- UARTs (*)
- I2C (tbc) (*)

(*) mainly relevant to discrete component; appreciated in conjunction to IP Core but not mandatory

Some requirements (cont.)

Miscellaneous:

- 4-8 32 bits general purpose Timers
- 8-16 Interrupts lines (e.g. 8 internal and 8 external)
- Watchdog
- On Board Time
- GPIO
- Embedded 16 bits ADC (or ADC I/F for IP Core) (*)
- Embedded DACs (TBC, at least 8 would be needed) (*)
- Embedded HK acquisition sequencer (*)
- Generation of std commands (M/L, O/O pulses).(*)

(*) mainly relevant to discrete component

Radiation Tolerance:

- TID ≥ 50 kRad
- SEU/SEL Protected design
- EDAC on external and internal memories
- Autonomous scrubbing (TBC).

Some requirements (cont.)

Test and Debug:

- Embedded Debug Serial Link / JTAG
- Availability of supported and mature SDE and debugging tools (e.g. KEIL)

Support to users:

- Comprehensive and exhaustive documentation
- Easy integration in customer design (IP Core)
- Test benches availability (IP Core)
- Effective Technical support